LSI403Z Digital Signal Processor

Preliminary Datasheet

The LSI403Z is a 16-bit, fixed-point digital signal processor (DSP) based on the LSI Logic ZSP400 DSP core. The LSI403Z contains an entire DSP system on a single chip, and is designed for applications requiring high throughput and flexibility coupled with high speed I/O, such as communications infrastructure equipment.

The LSI403Z operates at a clock rate of 150 MHz for a maximum effective throughput of 600 RISC-like MIPS. The LSI403Z RISC architecture is easy to program, and it uses a four-way superscalar pipeline with five stages to process up to 20 instructions at a time. The processor's execution unit contains two multiplier/accumulator (MAC) units and two arithmetic logic units (ALUs). The LSI403Z also supports single cycle add-compare-select, bit manipulation, and 32-bit arithmetic and logic operations.

The LSI403Z provides 16 Kwords of on-chip instruction memory and 16 Kwords of on-chip data memory supported by an 8-channel DMA controller, which can transfer instructions and data. For optimum I/O performance and flexibility, the LSI403Z contains two high-speed time-division multiplexing (TDM) serial ports, a single 8-bit host processor interface (HPI), an external memory interface unit (MXU), and a 4-pin programmable I/O (PIO) port. An IEEE 1149.1 Joint Test Activity Group (JTAG) port supports program download and debug.

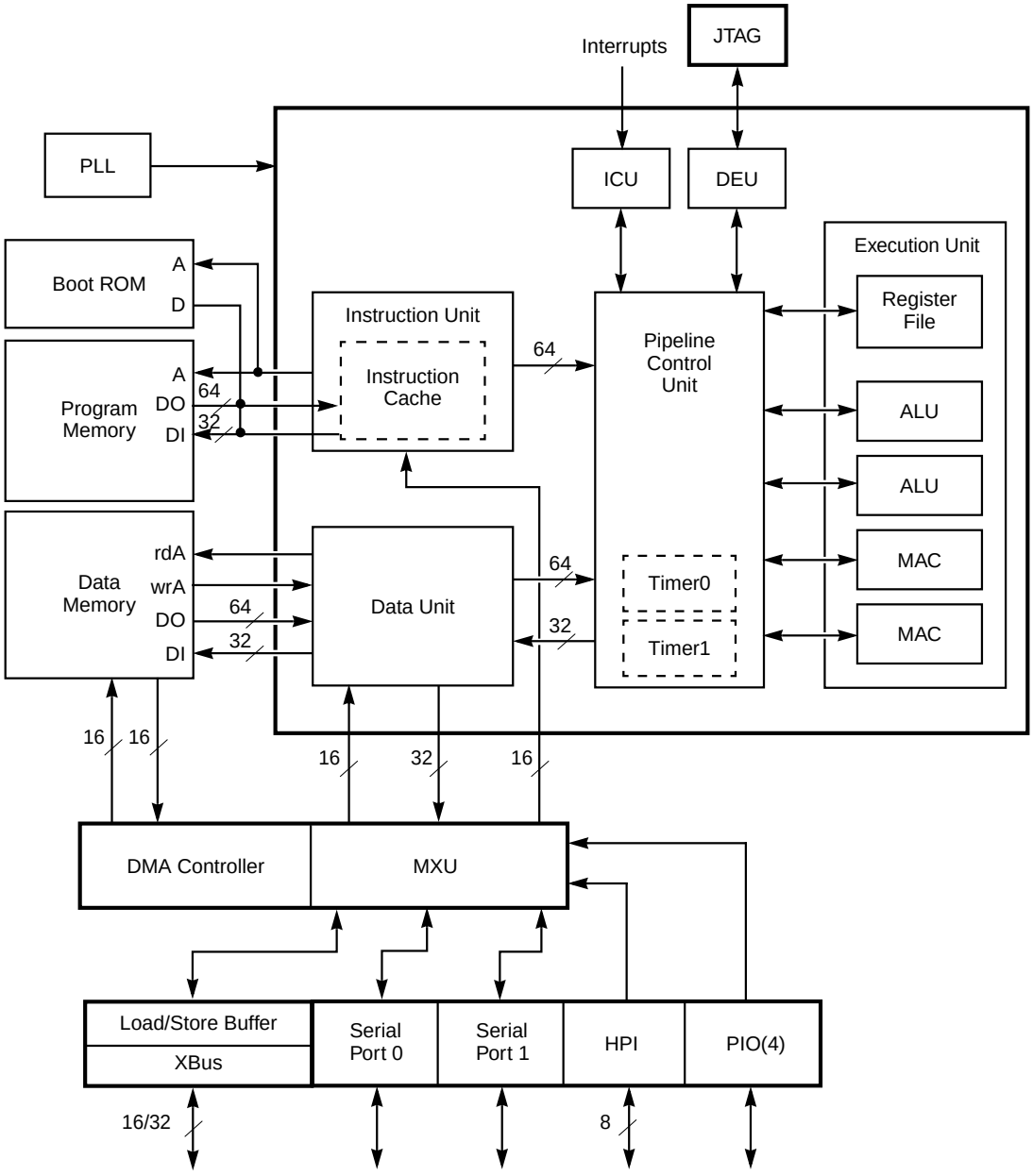
LSI Logic provides a software development kit containing an assembler, linker, GUI debugger, simulator, C compiler, and JTAG-based hardware emulator.

The LSI403Z is fabricated in the LSI Logic G12™-p technology. The LSI403Z is powered by a 1.8 V supply core and a 3.3 V I/O supply, and is packaged in a 208-pin plastic quad flat pack (PQFP) package.

Figure 1 shows a block diagram of the LSI403Z.

Copyright © 2000–2001 by LSI Logic Corporation. All rights reserved.

Figure 1 LSI403Z Block Diagram



DEU = Device Emulation Unit
HPI = Host Processor Interface
ICU = Interrupt Control Unit
PLL = Phase-Locked Loop
XBus = External Bus

Features and Benefits

Processor

- RISC architecture
  - Instruction grouping by hardware for parallel execution
- Four-way superscalar architecture
  - Two MACs
  - Two ALUs
- 600 RISC-like MIPS maximum throughput at a clock rate of 150 MHz
- Multitasking support
  - Low-latency interrupt structure with programmable priority levels
  - Efficient context switch support
- On-chip PLL for clock generation

Applications

- Optimized for communications infrastructure applications
  - Single-cycle, dual 16-bit MAC with 40-bit result
  - Single-cycle, high-precision (32-bit) MAC with 40-bit result
  - Two-cycle complex multiply
  - Single-cycle add-compare-select for Viterbi decoding

Technology

- 208-pin PQFP package

Memory

- 16 Kword internal instruction RAM
- 16 Kword internal data RAM
- 8-channel DMA controller
  - Supports fast I/O transfers
  - Transfers instructions/data to and from internal memory
- 32-bit MXU
  - Glueless interface to synchronous-burst SRAMs (SBSRAMs)
  - 18-bit address space (512 Kwords) for instruction and data memory
- Glueless interface to 16-bit SRAMs
- 2 Kword internal boot ROM

I/O

- Two high-speed TDM serial ports
  - H.100/H.110 bitstream-compatible
- 8-bit HPI
- 4-pin PIO port
- IEEE 1149.1-compliant JTAG port

Timers

- Two 16-bit timers with a 6-bit prescaler
- Single-shot and continuous mode

Functional Description

The LSI403Z contains an entire DSP system and allows the attachment of external memory and peripherals. See Figure 1 for a block diagram of the LSI403Z.

Core Modules

The pipeline control unit groups instructions, resolves dependencies, and schedules instructions for execution by the execution unit. The pipeline control unit also processes interrupt requests forwarded from the ICU.

The LSI403Z contains a four-way, superscalar, five-stage pipeline. At any time, up to 20 instructions may be in various stages of the pipeline. The five pipeline stages of this machine are: Fetch/Decode (F/D), Group (G), Read (R), Execute (E), and Write (W).

The pipeline control unit also contains two 16-bit timers for interrupt generation. Both timers are fully-programmable and have 6-bit prescalers. When enabled, the timers count down from the user-specified initial value to zero at a rate determined by the scaled output of the LSI403Z output clock. The timers generate an interrupt when zero is reached. The timers can be configured to reload automatically with the initial count to generate periodic interrupts.

The ICU interfaces with the pipeline control unit. To use an off-chip ICU, connect the off-chip ICU to the nonmaskable interrupt (NMI) pin of the LSI403Z.

The data unit fetches and stores data into the data cache. The data unit contains the data prefetcher and cache, and contains the logic for two circular buffers.

The instruction unit fetches instructions, decodes and dispatches them, and places the instructions in the instruction cache. The instruction unit contains the instruction cache, the instruction prefetcher, and the instruction dispatch unit. The instruction unit also contains branch prediction logic.

The control register file contains a set of 16-bit control registers used for mode control, status, and flag information.

The execution unit performs all arithmetic and logical operations in the LSI403Z. The execution unit contains two 16-bit ALUs, two 16-bit x 16-bit MAC units, and a general purpose (operand) register file.

The two ALUs are identical and can be combined as a single 32-bit ALU. The MAC units can perform two 16-bit x 16-bit multiply operations and a single 40-bit accumulation per cycle, or one 32-bit x 32-bit multiply operation and a single 40-bit accumulation per cycle.

The boot ROM provides processor self-test capabilities and JTAG-based emulation support.

I/O Units

The LSI403Z contains two identical serial ports capable of 8- or 16-bit active or passive transfers. In active mode, the serial port generates its own bit clock and sync signals. The serial port bit clock frequency is determined by the processor clock rate divided by a user-specified value. The maximum transfer rate in both modes is one-half the processor clock rate.

Both LSI403Z serial ports provide a TDM mode compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also establish a serial multiprocessor communication link with only three signals. The user selects the word length (8 or 16 bits) and frame length (1–128 time slots) for TDM transfers. Transmit and receive time slots are programmed individually, and can be modified on the fly.

Serial port frame sync signals are fully programmable for use with all TDM port protocols.

The HPI provides an asynchronous 8-bit parallel port for interfacing with off-chip devices. The HPI is compatible with Motorola- and Intel-style memory interfaces, and supports word transfers. The control, transmit data, and receive data registers are memory-mapped.

Four PIO signals support a general-purpose hardware interface. Each PIO may be configured as an input pin or an output pin.

DMA Controller

The LSI403Z's 8-channel DMA controller supports zero-overhead instruction or data transfers to/from the entire 32 Kwords of internal RAM to the memory interface unit (external expansion bus), one of the serial ports, or the HPI. The eight DMA channels are segmented between four indexed and four nonindexed channels.

Indexed DMA channels perform sequential or indexed accesses to/from internal memory. These channels are designed specifically to work with the TDM serial ports. Data buffers can read from or write to DSP memory corresponding to logical TDM channels (time slots). The user specifies the buffer length and the number of buffers to service, and the DMA controller automatically updates the pointer for each transfer within a frame. When a frame transfer completes, the pointer updates the memory address and begins transferring data for the next frame.

Nonindexed DMA channels perform only sequential accesses to/from internal memory. A transfer occurs at the specified memory location whenever an interrupt from the specified peripheral request occurs. The interrupt request may come from the HPI or one of the two serial ports. After the interrupt, the pointer register updates with the next internal memory location. When the DMA channel pointer reaches the buffer length, the processor generates a DMA interrupt request and terminates the DMA transaction.

When the DMA channel pointer reaches the last location of the last buffer, the processor generates a DMA interrupt and sets the bit corresponding to the channel in the DMA status register. This action terminates the DMA transaction.

The memory interface unit connects the LSI403Z to off-chip memory or peripherals through a 32-bit data bus and an 18-bit address bus. The memory interface unit provides a glueless interface to 16-bit asynchronous memory devices (ROM, EPROM, and SRAM) and 32-bit SBSRAMs.

JTAG Support

The JTAG port is an IEEE 1149.1-compliant test access port (TAP). When coupled with the DEU, JTAG provides access to all on-chip resources. The DEU works in conjunction with code residing in the internal ROM to provide full-speed in-circuit emulation, allowing full visibility and control of the device memory and registers. The JTAG port, DEU, and internal ROM provide the capability to download code to internal and external RAM.

PLL

The LSI403Z uses a PLL to generate a high-frequency processor clock from a slower, off-chip clock source. The off-chip clock source is applied to the CLKIN pin of the DSP and must be a crystal oscillator within the frequency range of 2 to 40 MHz[1]. The CLKOUT pin reflects the processor clock frequency. The processor clock can use an off-chip clock source directly by bypassing the on-chip PLL.

Operating Modes (Power Levels)

The LSI403Z supports four modes of operation to help conserve power:

- Normal mode

  DSP executes at full speed, and all peripherals are active.

- Idle mode

  DSP inactive and all peripherals are active. Any interrupt or reset wakes the device.

- Sleep mode

  DSP and all peripherals inactive. Any interrupt or reset wakes the device.

- Halt mode

  DSP and all peripherals inactive. The PLL retains its lock. Only NMI or reset wakes the device.

1. The LSI403Z is a fully-static device. The CLKIN signal will accept input down to DC when the PLL is bypassed.

Instruction Set Summary

Table 1 summarizes the ZSP instruction set used by the LSI403Z.

Table 1 ZSP Instruction Set

Instruction	Description
ABS	Absolute Value
ABS.E	Absolute Value (Extended Precision)
ADD	Add Immediate
ADD	Add Registers
ADD.E	Add Registers (Extended Precision)
ADDC.E	Add with Carry (Extended Precision)
AGN0	Again0
AGN1	Again1
AGN2	Again2
AGN3	Again3
AND	Logical AND
AND.E	Logical AND (Extended Precision)
BC	Branch on Carry
BGE	Branch on Greater than or Equal to
BGT	Branch on Greater than
BITC	Bit Clear Control Register
BITC	Bit Clear Operand Register
BITI	Bit Invert Control Register
BITI	Bit Invert Operand Register
BITS	Bit Set Control Register
BITS	Bit Set Operand Register
(Sheet 1 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
BITT	Bit Test Control Register
BITT	Bit Test Operand Register
BLE	Branch on Less than or Equal to
BLT	Branch on Less than
BNC	Branch on No Carry
BNOV	Branch on No Overflow
BNZ	Branch on Not Zero
BOV	Branch on Overflow
BR	Unconditional Branch
BZ	Branch on Zero
CALL	Call Label/Operand Register
CMACI.A	Complex MAC Imaginary to Accumulator A
CMACI.B	Complex MAC Imaginary to Accumulator B
CMACR.A	Complex MAC Real to Accumulator A
CMACR.B	Complex MAC Real to Accumulator B
CMP	Compare Immediate/Register to Register
CMP.E	Compare Immediate/Register to Register (Extended Precision)
CMULI.A	Complex Multiplication Imaginary to Accumulator A
CMULI.B	Complex Multiplication Imaginary to Accumulator B
CMULR.A	Complex Multiplication Real to Accumulator A
CMULR.B	Complex Multiplication Real to Accumulator B
DMAC.A	Double MAC to Accumulator A
DMAC.B	Double MAC to Accumulator B
DMUL.A	Multiplication (Extended Precision) to Accumulator A
(Sheet 2 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
DMUL.B	Multiplication (Extended Precision) to Accumulator B
IMUL.A	Integer Multiply to Accumulator A
IMUL.B	Integer Multiply to Accumulator B
LD	Load
LDDU	Load Double with Update
LDU	Load with Update
LDX	Load with Register-Based Offset
LDXU	Load with Register-Based Offset And Update
MAC.A	Multiply Accumulate to Accumulator A
MAC.B	Multiply Accumulate to Accumulator B
MAC2.A	Dual MAC to Accumulator A
MAC2.B	Dual MAC to Accumulator B
MACN.A	Multiply Accumulate with Negation to Accumulator A
MACN.B	Multiply Accumulate with Negation to Accumulator B
MAX	Maximum
MAX.E	Maximum (Extended Precision)
MIN	Minimum
MIN.E	Minimum (Extended Precision)
MOV	Move Control Register to Operand Register
MOV	Move Immediate to Operand Register
MOV	Move Operand Register to Control Register
MOV	Move Operand Register to Operand Register
MOV	Move to PC
MOVH	Move Immediate to Higher Byte of Control Register
(Sheet 3 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
MOVH	Move Immediate to Higher Byte of Operand Register
MOVL	Move Immediate to Lower Byte of Control Register
MOVL	Move Immediate to Lower Byte of Operand Register
MUL.A	Multiply to Accumulator A
MUL.B	Multiply to Accumulator B
MULN.A	Multiply with Negation to Accumulator A
MULN.B	Multiply with Negation to Accumulator B
NEG	Negate
NEG.E	Negate (Extended Precision)
NOP	No Operation
NORM	Normalize
NORM.E	Normalize (Extended Precision)
NOT	Logical Not
NOT.E	Logical Not (Extended Precision)
OR	Logical Or
OR.E	Logical Or (Extended Precision)
PADD.A	Parallel Add Registers to Accumulator A
PADD.B	Parallel Add Registers to Accumulator B
PSUB.A	Parallel Subtract Registers to Accumulator A
PSUB.B	Parallel Subtract Registers to Accumulator B
RET	Return from Subroutine
RETI	Return from Interrupt
REVB	Reverse Bit
ROUND.E	Round (Extended Precision)

(Sheet 4 of 6)

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
SHLA	Shift Left Arithmetic Immediate
SHLA	Shift Left Arithmetic Register
SHLA.E	Shift Left Arithmetic Immediate (Extended Precision)
SHLA.E	Shift Left Arithmetic Register (Extended Precision)
SHLL	Shift Left Logical Immediate
SHLL	Shift Left Logical Register
SHLL.E	Shift Left Logical Immediate (Extended Precision)
SHLL.E	Shift Left Logical Register (Extended Precision)
SHRA	Shift Right Arithmetic Immediate
SHRA	Shift Right Arithmetic Register
SHRA.E	Shift Right Arithmetic Immediate (Extended Precision)
SHRA.E	Shift Right Arithmetic Register (Extended Precision)
SHRL	Shift Right Logical Immediate
SHRL	Shift Right Logical Register
SHRL.E	Shift Right Logical Immediate (Extended Precision)
SHRL.E	Shift Right Logical Register (Extended Precision)
ST	Store
STDU	Store Double with Update
STU	Store with Update
STX	Store with Register-Based Offset
STXU	Store with Register-Based Offset And Update
SUB	Subtract

(Sheet 5 of 6)

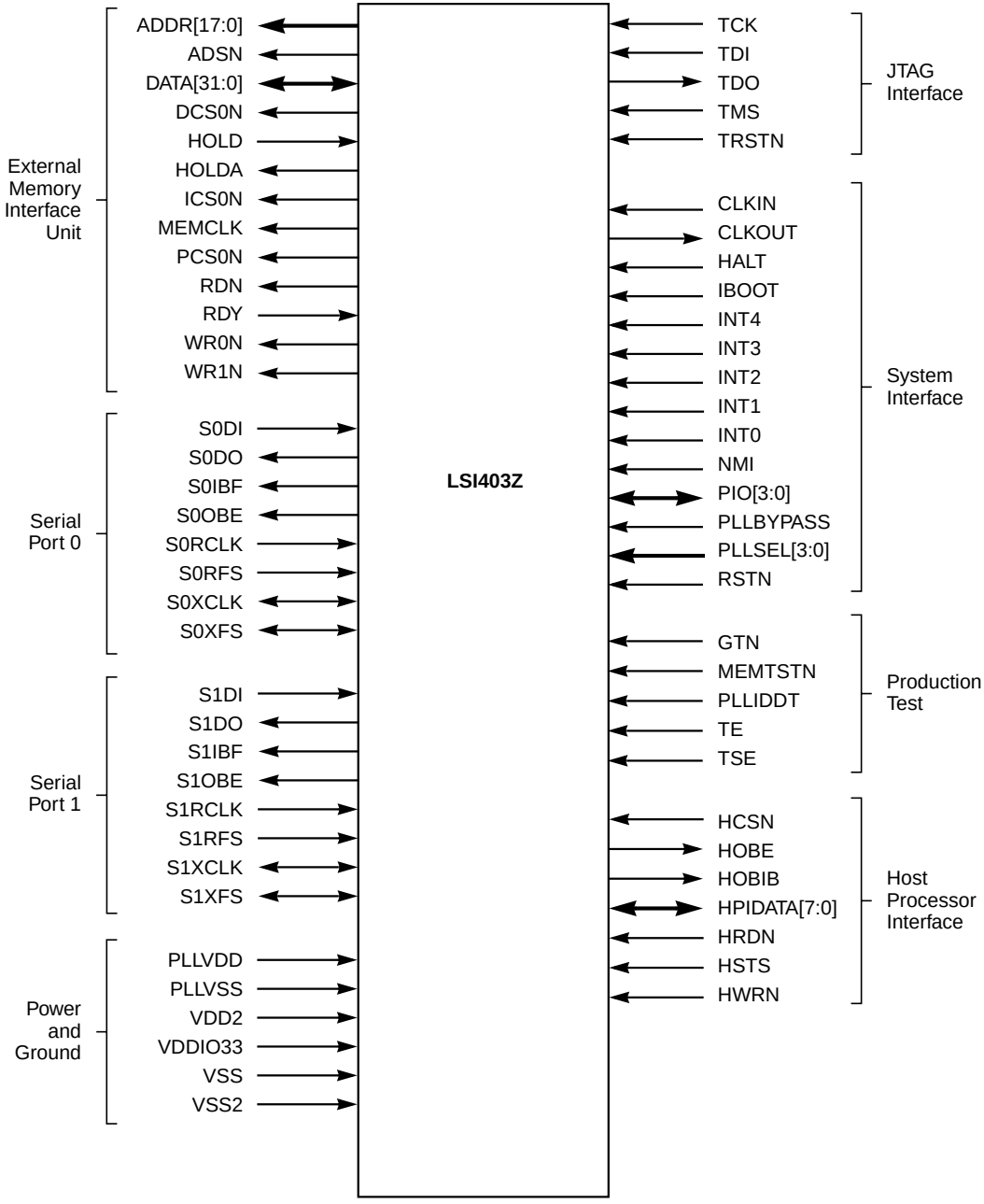
Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
SUB.E	Subtract (Extended Precision)
SUBC.E	Subtract With Carry (Extended Precision)
VIT_A	Viterbi Instruction for Point A
VIT_B	Viterbi Instruction for Point B
XOR	Exclusive Or
XOR.E	Exclusive Or (Extended Precision)
(Sheet 6 of 6)	

Signal Descriptions

This section describes all external LSI403Z signals. Figure 2 shows the LSI403Z interface. Signals that end with an “N” are active LOW signals.

Figure 2 LSI403Z System Interfaces



The signals have been divided into the following tables:

Table 2 External Memory Interface Unit (MXU) Signals

Signal	I/O	Description
ADDR[17:0]	Output	External Memory Address Bus
ADSN	Output	SBSRAM Address Strobe
DATA[31:0]	Bidirectional	External Memory Data Bus
DCS0N	Output	Data Memory Chip Select
HOLD	Input	External Memory Access Hold Request
HOLDA	Output	External Memory Access Hold Acknowledge
ICS0N	Output	Instruction Memory Chip Select
MEMCLK	Output	SBSRAM Clock
PCS0N	Output	Memory-Mapped Peripheral Chip Select
RDN	Output	Read Strobe
RDY	Input	Reserved[1]
WR0N	Output	Write Strobe (DATA[15:0])
WR1N	Output	Write Strobe (DATA[31:16])

1. Tie this pin HIGH for compatibility with future ZSP-based devices.

Table 3 Serial Port Signals

Signal[1]	I/O	Description
SxDI	Input	Data Input
SxDO	Output	Data Output
SxIBF	Output	Input Buffer Full
SxOBE	Output	Output Buffer Empty
SxRCLK	Input	Receive Clock
SxRFS	Input	Receive Frame Sync
SxXCLK	Bidirectional	Transmit Clock
SxXFS	Bidirectional	Transmit Frame Sync

1. Each serial port signal exists for serial port 0 and serial port 1. The signal names are preceded by S0 and S1 (for example, S0DO and S1DO).

Table 4 Power and Ground Signals

Signal	I/O	Description
PLLVDD[1]	Input	PLL Power (1.8 V)
PLLVSS[1]	Input	PLL Ground
VDD2	Input	Core Power (1.8 V)
VDDIO33	Input	I/O Device Power (3.3 V)
VSS	Input	I/O Device Ground
VSS2	Input	Core Ground

1. PLL must have a separate power and ground.

Table 5 JTAG Interface Signals

Signal	I/O	Description
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TMS	Input	Test Mode Select
TRSTN	Input	Test Port Reset

Table 6 System Interface Signals

Signal	I/O	Description
CLKIN	Input	Clock Source
CLKOUT	Output	Clock Output
HALT	Input	Stop Processor Clock
IBOOT	Input	Memory Map Select
INT4	Input	External Hardware Interrupt 4
INT3	Input	External Hardware Interrupt 3
INT2	Input	External Hardware Interrupt 2
INT1	Input	External Hardware Interrupt 1
INT0	Input	External Hardware Interrupt 0
NMI	Input	Nonmaskable Interrupt
PIO[3:0]	Bidirectional	Programmable I/O Bus
PLLBYPASS	Input	PLL Bypass
PLLSEL[3:0]	Input	PLL Mode Select Bus
RSTN	Input	Device Reset

Table 7 Production Test Signals

Signal	I/O	Description
GTN	Input	Global 3-State Enable
MEMTSTN	Input	Memory Test Enable
PLLIDDT	Input	Reserved; Tie LOW
TE	Input	Reserved; Tie LOW
TSE	Input	Reserved; Tie LOW

Table 8 Host Processor Interface (HPI) Signals

Signal	I/O	Description
HCSN	Input	Host Chip Select
HOBE	Output	HPI Output Buffer Empty Flag
HOBIB	Output	HPI Output Status
HPIDATA[7:0]	Bidirectional	HPI Data Bus
HRDN	Input	Intel Mode Read Strobe/Motorola Mode Data Strobe
HSTS	Input	HPI Input Status
HWRN	Input	Intel Mode Write Strobe/Motorola Mode Data Direction Select

Functional Waveforms

This section contains functional waveforms for selected LSI403Z operations. For complete timing information, refer to the *LSI403Z Digital Signal Processor User's Guide,* Document No. DB15-000169-00. In this section, "T" refers to the DSP clock period.

Serial Port Timing

The two serial ports in the LSI403Z are identical. This section contains transmit and receive timing waveforms for the serial ports. The timing for burst/continuous mode and TDM mode is identical.

The advance transmit frame sync (axfs) field of the sp0ct1 and sp1ct1 registers controls the relative position of the frame sync and data signals.

Figure 3 shows the transmit timing for the serial ports when the frame sync and data lines are coincident and the transmit frame sync and clock signals are generated externally. Table 9 shows the timing relations for the signals in Figure 3.

Figure 3 Serial Port Transmit Timing for axfs = 0b00 (SxXCLK/SxXFS as Inputs)

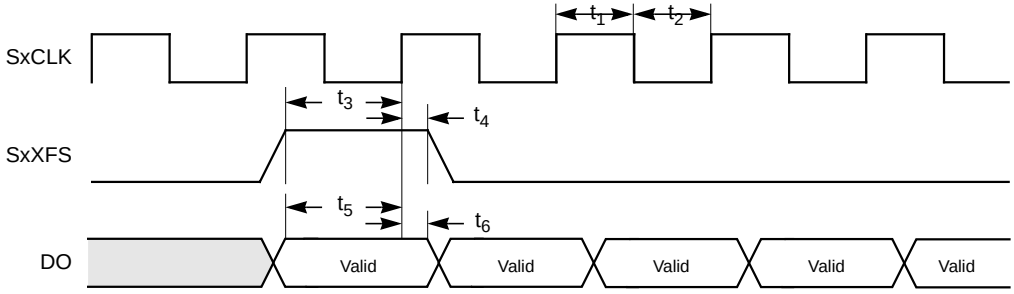


Table 9 Serial Port Transmit Timing Values (SxXCLK/SxXFS as Inputs)

Symbol	Parameter	Minimum	Maximum	Unit
t_1	Clock HIGH[1]	1	–	Processor Clock Periods
t_2	Clock LOW[1]	1	–	
t_3	SxXFS Setup Time	4	–	ns
t_4	SxXFS Hold Time	1	–	
t_5	Data Out Setup Time	4	–	
t_6	Data Out Hold Time	1	–	

1. SxCLK must maintain a 50% duty cycle.

Figure 4 shows the transmit timing for the serial ports when the frame sync and data lines are coincident and the transmit frame sync and clock signals are generated by the serial port. Table 10 shows the timing relations for the signals in Figure 4.

Figure 4 Serial Port Transmit Timing for axfs = 0b00 (SxCLK/SxXFS as Outputs)

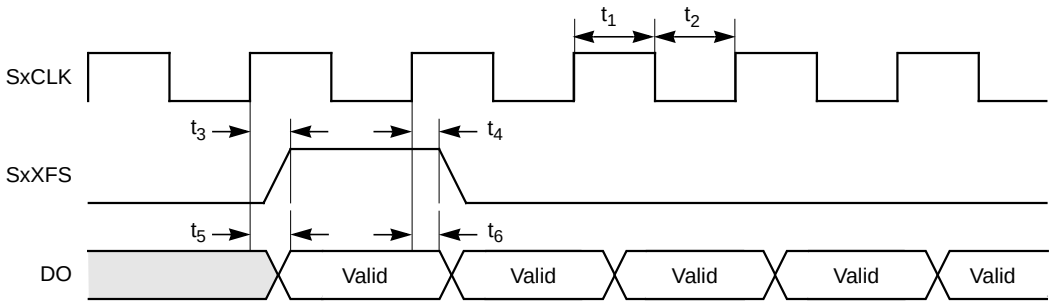


Table 10 Serial Port Transmit Timing Values (SxXCLK/SxXFS as Outputs)

Symbol	Parameter	Minimum	Maximum	Unit
t_1	Clock HIGH	1	–	Processor Clock Periods
t_2	Clock LOW	1	–	
t_3	SxXFS Propagation Delay	1	4	ns
t_4	SxXFS Propagation Delay	1	–	
t_5	Data Out Propagation Delay	1	4	
t_6	Data Out Hold Time	1	–	

The advance receive frame sync (arfs) field of the sp0ct1 and sp1ct1 registers controls the relative position of the frame sync and data signals.

Figure 5 shows the receive timing for the serial ports when the frame sync and data lines are coincident. The receive frame sync and clock signals are always generated externally. Table 11 shows the timing relations for the signals in Figure 5.

Figure 5 Serial Port Receive Timing (arfs = 0b00)

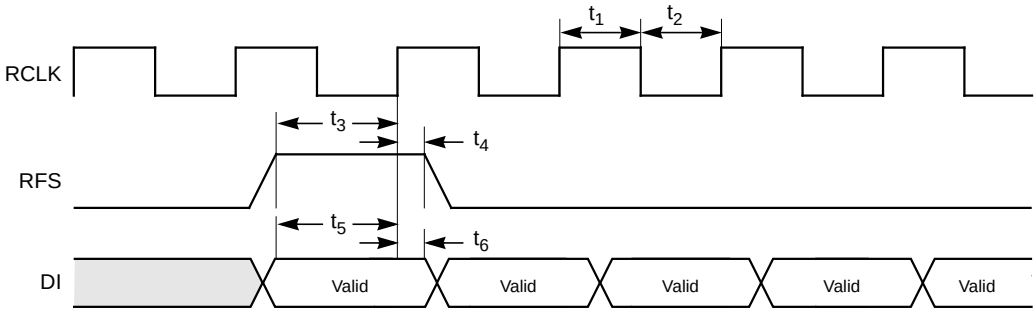


Table 11 Serial Port Receive Timing Values

Symbol	Parameter	Minimum	Maximum	Unit
t_1	Clock HIGH[1]	1	–	Processor Clock Periods
t_2	Clock LOW[1]	1	–	
t_3	RFS Setup Time	4	–	ns
t_4	RFS Hold Time	1	–	
t_5	Data In Setup Time	4	–	
t_6	Data In Hold Time	1	–	

1. RCLK must maintain a 50% duty cycle.

External Memory Interface Unit (MXU) Timing

The MXU connects the LSI403Z to external memory and peripherals.

Asynchronous Mode

For all waveforms in this section, replace xCSxN with the appropriate chip-select signal (DCS0N, ICS0N, or PCS0N). The dwait register fields have the following values:

- csrw is set to 0x0
- rwpw is set to 0x4
- rwcs is set to 0x0

Figure 6 shows an instruction or data memory read with four wait-state cycles. Table 12 describes the timing relationships in Figure 6.

Figure 6 Asynchronous External Instruction or Data Memory Read (4-Cycle Wait State)

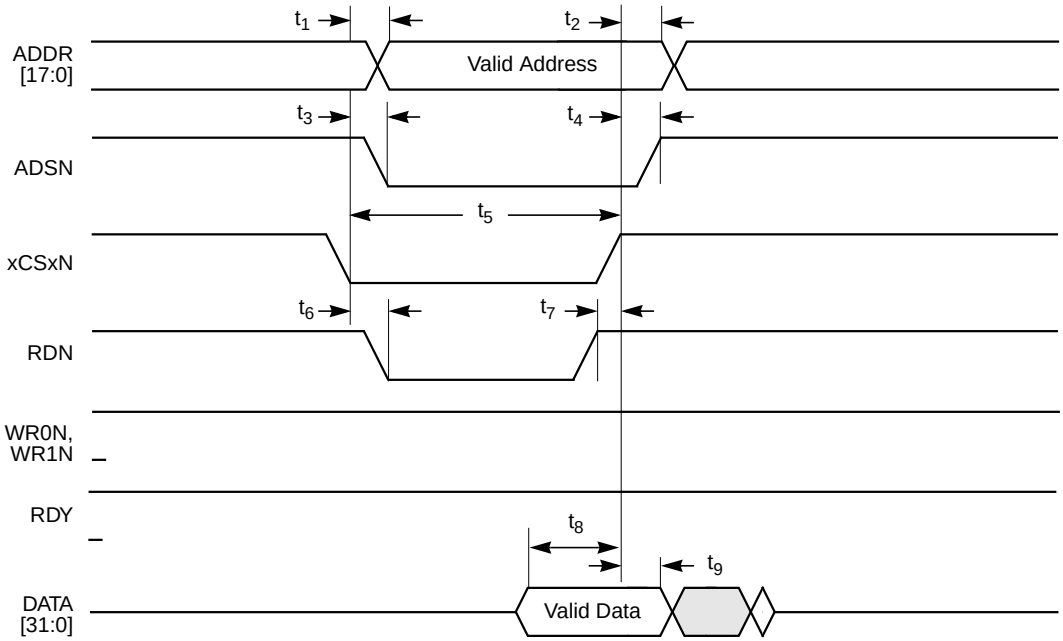


Table 12 Asynchronous External Instruction or Data Memory Read Timing (4-Cycle Wait State)

Reference	Description	Minimum[1]	Maximum[1]	Unit
t_1	xCSxN LOW to ADDR Valid	–	1	ns
t_2	ADDR Hold Time (xCSxN HIGH to ADDR Invalid)	2	–	ns
t_3	xCSxN LOW to ADSN LOW	–	1	ns
t_4	ADSN Hold Time (xCSxN HIGH to ADSN HIGH)	0	–	ns
t_5	Enable Pulse Width (xCSxN LOW to xCSxN HIGH)	T • (csrw + rwpw + rwcs)	–	ns
t_6	xCSxN LOW to RDN LOW	–	T • csrw	ns
t_7	RDN HIGH to xCSxN HIGH	–	T • rwcs	ns
t_8	Data Valid to xCSxN HIGH	T	–	ns
t_9	Data Hold Time	0	–	ns

1. T is the processor clock cycle; csrw, rwpw, and rwcs are fields in the dwait register.

Figure 7 shows an instruction or data memory write with four wait-state cycles. Table 13 describes the timing relationships in Figure 7.

Figure 7 Asynchronous External Data or Instruction Memory Write (4-Cycle Wait State)

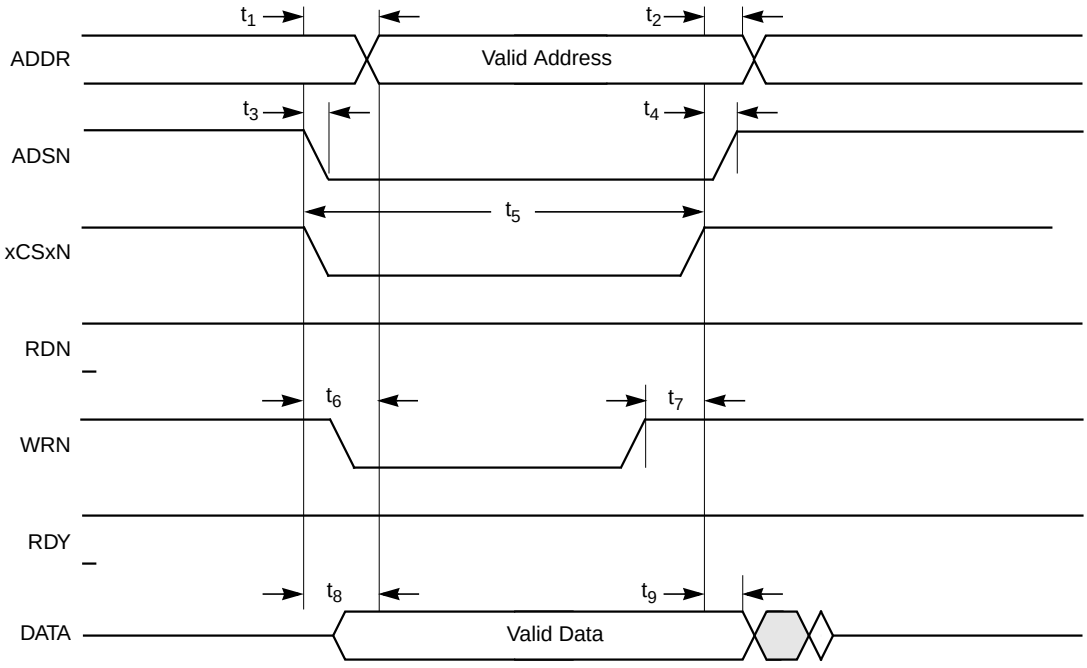


Table 13 Asynchronous/External Data or Instruction Memory Write Timing (4-Cycle Wait State)

Reference	Description	Minimum[1]	Maximum[1]	Unit
t_1	xCSxN LOW to ADDR Valid	–	1	ns
t_2	ADDR Hold Time (xCSxN HIGH to ADDR Invalid)	2	–	ns
t_3	xCSxN LOW to ADSN LOW	–	1	ns
t_4	ADSN Hold Time (xCSxN HIGH to ADSN HIGH)	0	–	ns
t_5	xCSxN LOW to xCSxN HIGH[2]	T • (csrw + rwpw + rwcs)	–	ns

Table 13 Asynchronous/External Data or Instruction Memory Write Timing (4-Cycle Wait State) (Cont.)

Reference	Description	Minimum[1]	Maximum[1]	Unit
t_6	xCSxN LOW to WRN LOW[2]	–	T • csrw	ns
t_7	WRN HIGH to xCSxN HIGH[2]	–	T • rwcs	ns
t_8	xCSxN LOW to Data Valid	–	1	ns
t_9	Data Hold Time (xCSxN HIGH to Data Invalid)	0	–	ns

1. T is the processor clock cycle; csrw, rwpw, and rwcs are fields in the dwait register.
2. These values (~10 ns) are significantly greater than of that of t_9 (~1 ns).

Synchronous Mode

Figure 8 shows the timing for synchronous external instruction or data reads. Table 14 describes the timing relationships shown in Figure 8.

Figure 8 Synchronous Mode Timing (2:1) Mode

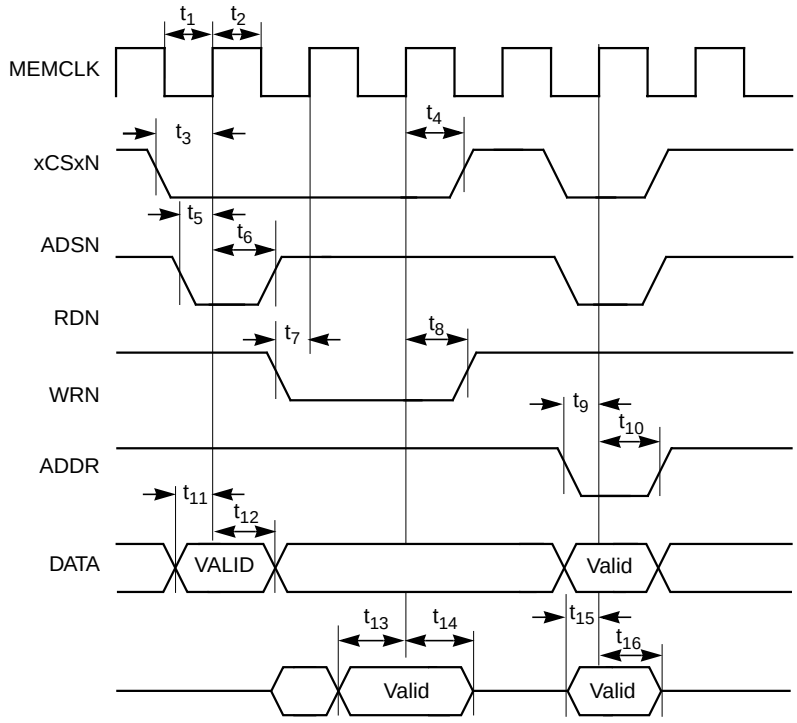


Table 14 Synchronous Mode Timing (2:1) Mode

Symbol	Description	Minimum	Maximum	Unit
t_1	Clock LOW	1	–	Cycles
t_2	Clock HIGH	1	–	Cycles
t_3	Clock LOW to xCSxN LOW	–	1	ns
t_4	Clock LOW to xCSxN HIGH	–	1	ns
t_5	Clock LOW to ADSN LOW	–	1	ns
t_6	Clock LOW to ADSN HIGH	–	1	ns
t_7	Clock LOW to RDN LOW	–	1	ns
t_8	Clock LOW to RDN HIGH	–	1	ns
t_9	Clock LOW to WRN LOW	–	1	ns
t_{10}	Clock LOW to WRN HIGH	–	1	ns
t_{11}	Clock LOW to ADDR Valid	–	1	ns
t_{12}	Clock LOW to ADDR Invalid	–	1	ns
t_{13}	Read Data Setup	2	–	ns
t_{14}	Read Data Hold	1	–	ns
t_{15}	Clock LOW to Write Data Valid	–	1	ns
t_{16}	Clock LOW to Write Data Invalid	–	1	ns

Host Port Interface (HPI) Timing

The HPI provides an asynchronous 16-bit parallel port for interfacing with off-chip devices. The HPI operates in Intel or Motorola mode.

Intel Mode

In Intel mode, HPI read cycles can be initiated/ended by the HRDN read strobe signal or the HCSN chip-select signal. To begin the read, HCSN and HRDN must be LOW. The last falling edge determines the starting time of the read cycle. Conversely, the first rising edge of HCSN or HRDN signals the end of the read cycle.

Figure 9 illustrates a host read initiated and completed by HCSN. Table 15 describes the timing relationships in Figure 9.

Figure 9 HPI Host Read, Intel Mode (HPICTL = 0b0000.00xx)

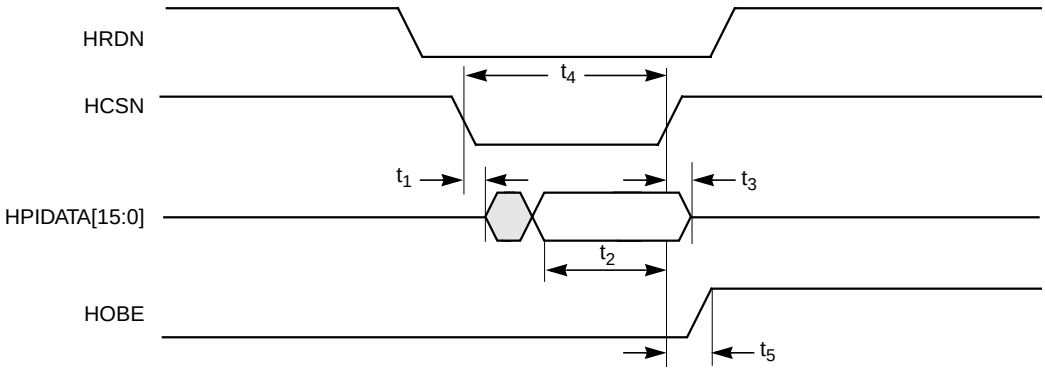


Table 15 HPI Host Read Timing, Intel Mode (HPICTL = 0b0000.00xx)

Reference	Description	Minimum	Maximum	Unit
t_1	Strobe (HRDN or HCSN) to Nonhigh-Z State	0.5	–	ns
t_2	Read Data Setup Time	0	–	ns
t_3	Read Data Hold Time	3 T	–	ns
t_4	Strobe (HRDN or HCSN) LOW Pulse Width	T	–	ns
t_5	HOBE Delay Time	0	–	ns

In Intel mode, HPI write cycles can be initiated/ended by the HWRN write strobe signal or the HCSN chip-select signal. To begin the write, HCSN and HWRN must be LOW. The last falling edge determines the starting time of the write cycle. Conversely, the first rising edge of HCSN or HWRN signals the end of the write cycle.

Figure 10 illustrates a host write initiated and completed by HCSN. Table 16 describes the timing relationships in Figure 10.

Figure 10 HPI Host Write, Intel Mode

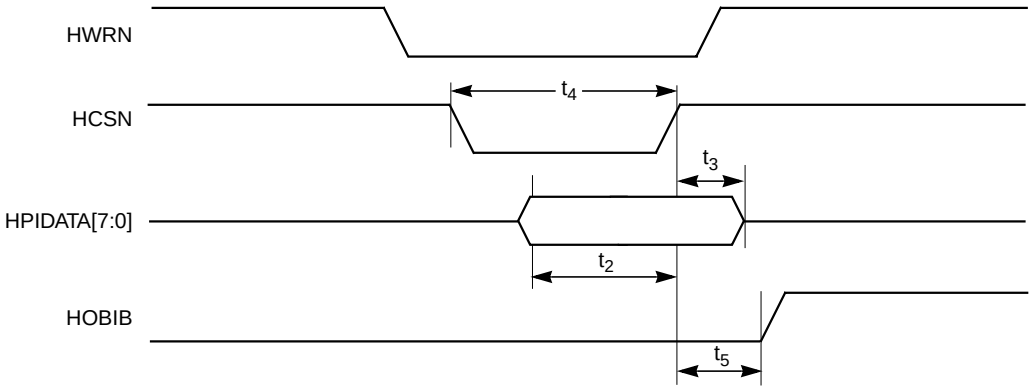


Table 16 HPI Host Write Timing, Intel Mode

Reference	Description	Minimum	Maximum	Unit
t_1	Strobe (HWRN or HCSN) to Nonhigh-Z State	0.5	–	ns
t_2	Write Data Setup Time	0	–	ns
t_3	Write Data Hold Time	3 T	–	ns
t_4	Strobe (HWRN or HCSN) LOW Pulse Width	T	–	ns
t_5	HOBE Delay Time	0	–	ns

Motorola Mode

In Motorola mode, the HRDN signal operates as a data strobe for reads and writes. The HWRN signal determines the data direction. For writes, HWRN must be LOW.

Figure 11 illustrates a host read initiated and completed by HRDN. Table 17 describes the timing relationships in Figure 11.

Figure 11 HPI Host Read, Motorola Mode

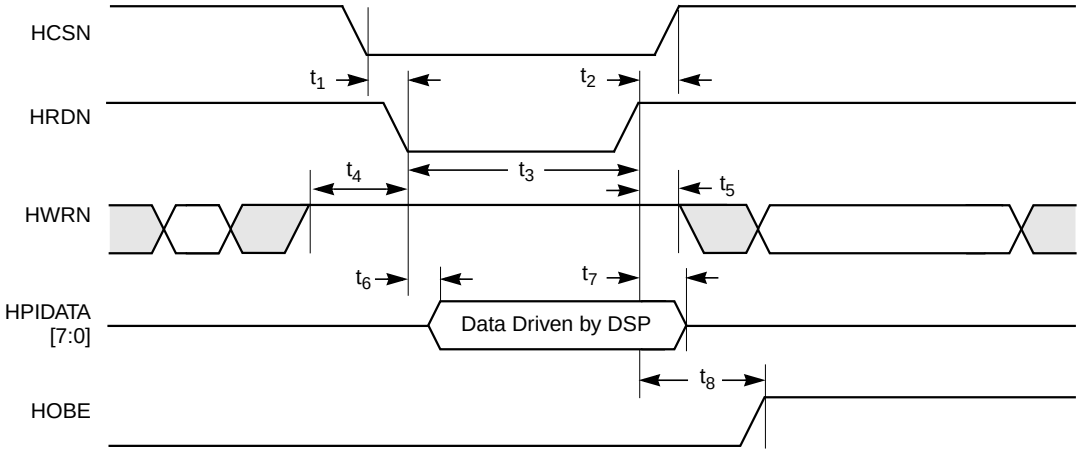


Table 17 HPI Host Read Timing, Motorola Mode

Reference	Description	Minimum	Maximum	Unit
t_1	HCSN to HRDN Setup Time (LOW to LOW)	0.5	–	ns
t_2	HRDN to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t_3	HRDN Pulse Width (LOW to HIGH)	3 T	–	ns
t_4	HWRN to HRDN Setup Time (HIGH to LOW)	T	–	ns
t_5	HRDN to HWRN Hold Time	0	–	ns
t_6	Data Delay Time (LOW to Valid)	–	T	ns
t_7	Data Hold Time (HIGH to Invalid)	0	–	ns
t_8	HOBE Delay Time (HIGH to HIGH)	–	T	ns

In Motorola mode, the HCSN and HRDN signals must both be asserted to perform a host write. The last falling edge determines the starting time of the write cycle. To end the write, HCSN or HRDN must be deasserted.

Figure 12 illustrates a host write initiated and completed by HRDN. Table 18 describes the timing relationships in Figure 12.

Figure 12 HPI Host Write, Motorola Mode

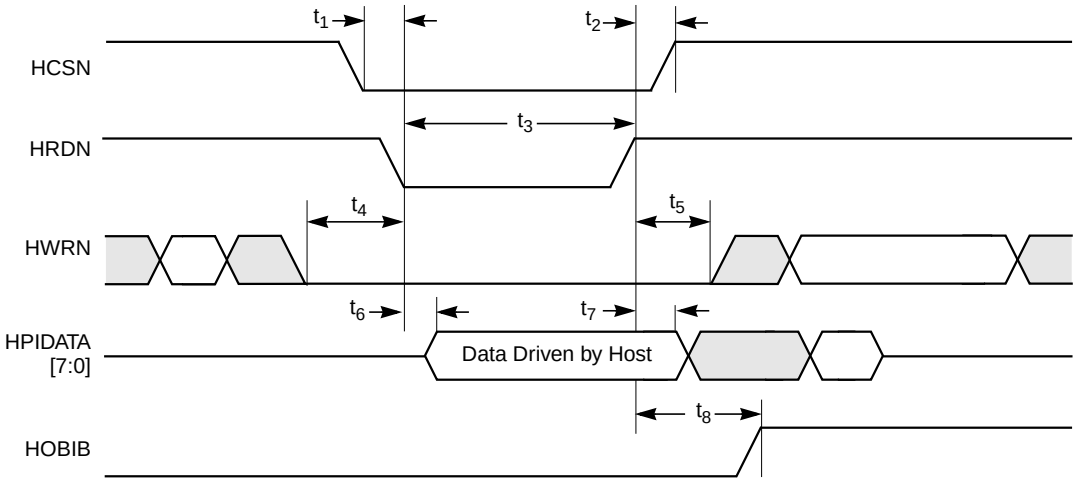


Table 18 HPI Host Write Timing, Motorola Mode

Reference	Description	Minimum	Maximum	Unit
t_1	HCSN to HRDN Setup Time (LOW to LOW)	0.5	–	ns
t_2	HRDN to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t_3	HRDN Pulse Width (LOW to HIGH)	3 T	–	ns
t_4	HWRN to HRDN Setup Time (LOW to LOW)	T	–	ns
t_5	HRDN to HWRN Hold Time	0	–	ns
t_6	Data Delay (LOW to Valid)	–	T	ns
t_7	Data Hold Time (HIGH to Invalid)	0	–	ns
t_8	HOBIB Delay Time (HIGH to HIGH)	–	T	ns

Specifications

This section describes the electrical and mechanical specifications of the LSI403Z.

Table 19 lists the DC characteristics for the LSI403Z.

Table 19 DC Electrical Characteristics

Parameter	Symbol	V_{DD} = 1.8 V, PLLVDD = 1.8 V, V_{DDIO33} = 3.3 V	
		Minimum	Maximum
Input Voltage Low	V_{IL}	0 V	0.8 V
Input Voltage High (1.8 V Supply Core)	V_{IH}	1.05 V	V_{DD} + 0.3 V
Input Voltage High (3.3 V I/O Supply)	V_{IH}	2.0 V	V_{DDIO33} + 0.3 V
Input Current	I_{IN}	–10 µA	10 µA
Output Low Voltage @ +2 mA (Low)	V_{OL}	–	0.4
Output High Voltage @ –2 mA (High)	V_{OH}	2.4	–
Output 3-State Current Low	I_{OZL}	–10 µA	–
Output 3-State Current High	I_{OZH}	–	–10 µA
Input Capacitance	C_I	–	5.5 pF

Table 20 lists the power dissipation characteristics of the LSI403Z.

Table 20 LSI403Z Power Dissipation

Frequency	Voltage	Power Dissipation
170 MHz	1.8 V	890 mW (Maximum)

Table 21 lists the recommended operating conditions for the LSI403Z.

Table 21 Recommended Operating Conditions

Parameter	Symbol	V_{DD} = 1.8 V, PLLVDD = 1.8 V, V_{DDIO33} = 3.3 V	
		Minimum	Maximum
Core Operating Voltage	V_{DD}	1.65 V	1.95 V
PLL Operating Voltage	PLLVDD	1.65 V	1.95 V
I/O Operating Voltage	V_{DDIO33}	3.0 V	3.6 V
Input Voltage	V_I	0 V	3.6 V
Output Voltage	V_O	0 V	V_{DDIO33}
Junction Temperature (Commercial Operating Conditions)	T_J	0 °C	115 °C
Ambient Temperature (Commercial Operating Conditions)	T_A	0 °C	85 °C

Table 22 lists the absolute maximum ratings for the LSI403Z. Operating beyond the limits specified in this table may cause permanent device damage.

Table 22 Absolute Maximum Ratings[1]

Property	Minimum	Maximum
DC Supply Voltage (V_{DD}, PLLVDD)[2]	–0.3 V	2.2 V
3.3 V I/O Input Voltage (V_{DDIO33})	–0.3 V	3.9 V

1. Referenced to V_{SS}.
2. Internal cells operate at 1.8 V.

Mechanical Specifications

The LSI403Z is packaged in a 208-pin PQFP package (package code UP). Table 23 shows the package junction-case thermal resistance.

Table 23 Thermal Resistance (Junction-Case)

Maximum Thermal Resistance (θ_{JC}, °C/W)
7.5

Table 24 shows the package case-to-ambient thermal resistance.

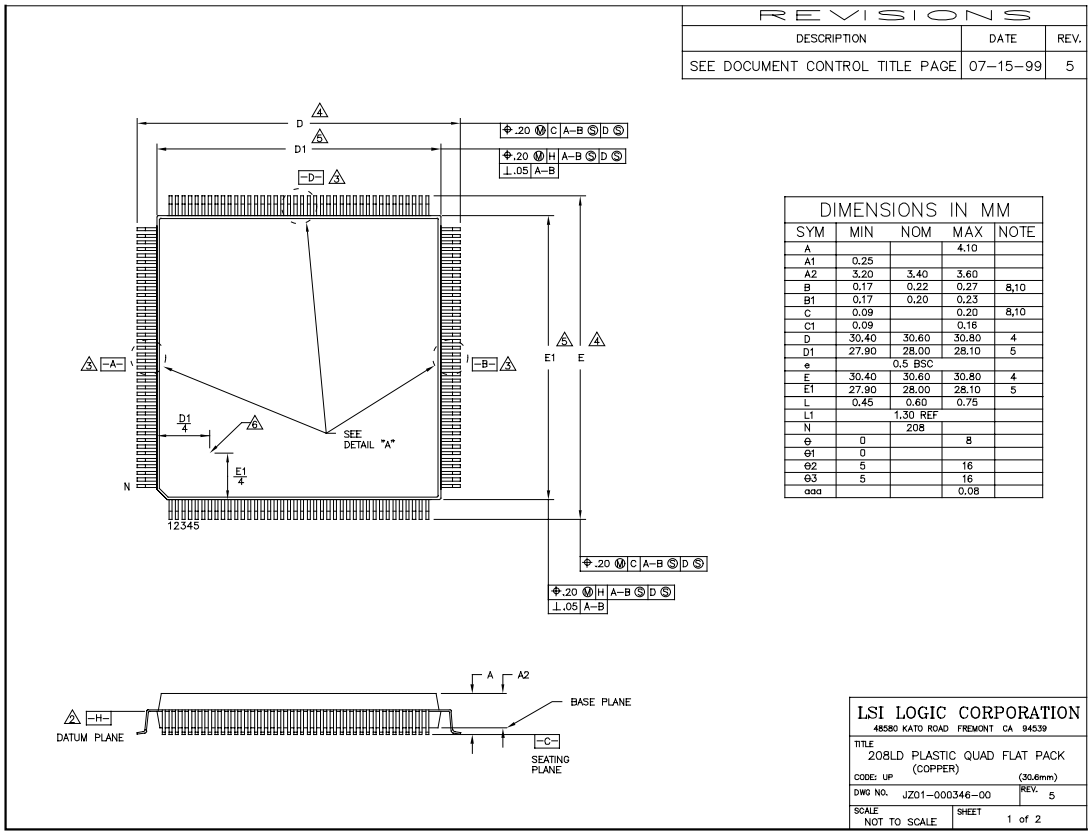
Table 24 Thermal Resistance (Case-Ambient)

Maximum Thermal Resistance (θ_{CA}, °C/W)	Airflow (LFPM)[1]
29.5	0
25.8	200
24.3	400
23.0	600

1. LPFM stands for linear feet per minute.

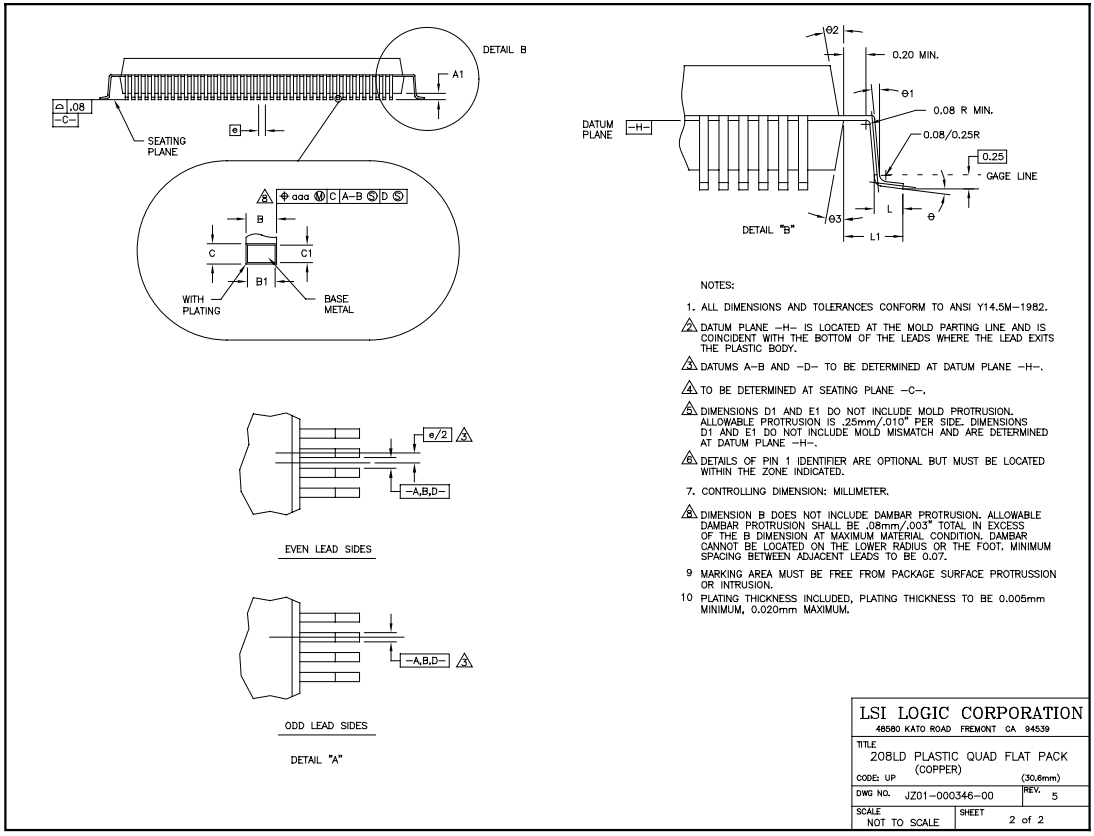
Figure 13 shows a mechanical drawing of the LSI403Z package.

Figure 13 208-pin PQFP Package Code (UP) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic representative by requesting the outline drawing for package code UP.**

Figure 13 208-pin PQFP Package Code (UP) Mechanical Drawing (Cont.)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic representative by requesting the outline drawing for package code UP.**

Table 25 lists the mapping of LSI403Z signals to package pins.

Table 25 LSI403Z Alphabetical Pinlist

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ADDR0	142	DATA21	73	PIO1	35	VDD2	72	VSS	177
ADDR1	141	DATA22	68	PIO2	32	VDD2	86	VSS	193
ADDR2	140	DATA23	67	PIO3	31	VDD2	100	VSS	206
ADDR3	139	DATA24	66	PLLBYPASS	148	VDD2	109	VSS2	4
ADDR4	136	DATA25	65	PLLIDDT	158	VDD2	123	VSS2	19
ADDR5	133	DATA26	64	PLLSEL0	164	VDD2	137	VSS2	33
ADDR6	132	DATA27	61	PLLSEL1	163	VDD2	152	VSS2	47
ADDR7	131	DATA28	60	PLLSEL2	160	VDD2	161	VSS2	57
ADDR8	130	DATA29	59	PLLSEL3	159	VDD2	175	VSS2	71
ADDR9	129	DATA30	56	PLLVDD	150	VDD2	189	VSS2	85
ADDR10	126	DATA31	55	PLLVSS	151	VDD2	203	VSS2	99
ADDR11	125	DCS0N	39	RDN	41	VDDIO33	9	VSS2	110
ADDR12	122	GTN	197	RDY	45	VDDIO33	21	VSS2	124
ADDR13	121	HALT	8	RSTN	181	VDDIO33	37	VSS2	138
ADDR14	120	HCSN	188	S0DI	29	VDDIO33	54	VSS2	153
ADDR15	117	HOBE	182	S0DO	22	VDDIO33	63	VSS2	162
ADDR16	116	HOBIB	183	S0IBF	26	VDDIO33	70	VSS2	176
ADDR17	115	HOLD	145	S0OBE	25	VDDIO33	79	VSS2	190
ADSN	44	HOLDA	146	S0RCLK	27	VDDIO33	88	VSS2	204
CLKIN	149	HPIDATA0	174	S0RFS	28	VDDIO33	95	WR0N	43
CLKOUT	147	HPIDATA1	173	S0XCLK	24	VDDIO33	112	WR1N	42
DATA0	114	HPIDATA2	172	S0XFS	23	VDDIO33	119		
DATA1	113	HPIDATA3	171	S1DI	17	VDDIO33	128		
DATA2	102	HPIDATA4	170	S1DO	10	VDDIO33	135		
DATA3	101	HPIDATA5	169	S1IBF	14	VDDIO33	144		
DATA4	98	HPIDATA6	168	S1OBE	13	VDDIO33	166		
DATA5	97	HPIDATA7	167	S1RCLK	15	VDDIO33	178		
DATA6	96	HRDN	185	S1RFS	16	VDDIO33	194		
DATA7	93	HSTS	184	S1XCLK	12	VSS	18		
DATA8	92	HWRN	187	S1XFS	11	VSS	30		
DATA9	91	IBOOT	7	TCK	198	VSS	46		
DATA10	90	ICS0N	38	TDI	196	VSS	62		
DATA11	89	INT0	205	TDO	195	VSS	69		
DATA12	84	INT1	202	TE	154	VSS	78		
DATA13	83	INT2	201	TMS	192	VSS	87		
DATA14	82	INT3	200	TRSTN	191	VSS	94		
DATA15	81	INT4	199	TSE	186	VSS	111		
DATA16	80	MEMCLK	179	VDD2	5	VSS	118		
DATA17	77	MEMTSTN	6	VDD2	20	VSS	127		
DATA18	76	NMI	180	VDD2	34	VSS	134		
DATA19	75	PCS0N	40	VDD2	48	VSS	143		
DATA20	74	PIO0	36	VDD2	58	VSS	165		

Notes

Notes

Notes

Sales Offices and Design Resource Centers

LSI Logic Corporation
Corporate Headquarters
Tel: 408.433.8000
Fax: 408.433.8989

NORTH AMERICA

California
Irvine
♦ Tel: 949.809.4600
Fax: 949.809.4444

Pleasanton Design Center
Tel: 925.730.8800
Fax: 925.730.8700

San Diego
Tel: 858.467.6981
Fax: 858.496.0548

Silicon Valley
♦ Tel: 408.433.8000
Fax: 408.954.3353

Wireless Design Center
Tel: 858.350.5560
Fax: 858.350.0171

Colorado
Boulder
♦ Tel: 303.447.3800
Fax: 303.541.0641

Colorado Springs
Tel: 719.533.7000
Fax: 719.533.7020

Fort Collins
Tel: 970.223.5100
Fax: 970.206.5549

Florida
Boca Raton
Tel: 561.989.3236
Fax: 561.989.3237

Georgia
Alpharetta
Tel: 770.753.6146
Fax: 770.753.6147

Illinois
Oakbrook Terrace
Tel: 630.954.2234
Fax: 630.954.2235

Kentucky
Bowling Green
Tel: 270.793.0010
Fax: 270.793.0040

Maryland
Bethesda
Tel: 301.897.5800
Fax: 301.897.8389

Massachusetts
Waltham
♦ Tel: 781.890.0180
Fax: 781.890.6158

Burlington - Mint Technology
Tel: 781.685.3800
Fax: 781.685.3801

Minnesota
Minneapolis
♦ Tel: 612.921.8300
Fax: 612.921.8399

New Jersey
Red Bank
Tel: 732.933.2656
Fax: 732.933.2643

Cherry Hill - Mint Technology
Tel: 856.489.5530
Fax: 856.489.5531

New York
Fairport
Tel: 716.218.0020
Fax: 716.218.9010

North Carolina
Raleigh
Tel: 919.785.4520
Fax: 919.783.8909

Oregon
Beaverton
Tel: 503.645.0589
Fax: 503.645.6612

Texas
Austin
Tel: 512.388.7294
Fax: 512.388.4171

Plano
♦ Tel: 972.244.5000
Fax: 972.244.5001

Houston
Tel: 281.379.7800
Fax: 281.379.7818

Canada
Ontario
Ottawa
♦ Tel: 613.592.1263
Fax: 613.592.3253

INTERNATIONAL

France
Paris
LSI Logic S.A.
Immeuble Europa
♦ Tel: 33.1.34.63.13.13
Fax: 33.1.34.63.13.19

Germany
Munich
LSI Logic GmbH
♦ Tel: 49.89.4.58.33.0
Fax: 49.89.4.58.33.108

Stuttgart
♦ Tel: 49.711.13.96.90
Fax: 49.711.86.61.428

Italy
Milan
LSI Logic S.P.A.
♦ Tel: 39.039.687371
Fax: 39.039.6057867

Japan
Tokyo
LSI Logic K.K.
♦ Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

Osaka
♦ Tel: 81.6.947.5281
Fax: 81.6.947.5287

Korea
Seoul
LSI Logic Corporation of Korea Ltd
Tel: 82.2.528.3400
Fax: 82.2.528.2250

The Netherlands
Eindhoven
LSI Logic Europe Ltd
Tel: 31.40.265.3580
Fax: 31.40.296.2109

Singapore
Singapore
LSI Logic Pte Ltd
Tel: 65.334.9061
Fax: 65.334.4749

Sweden
Stockholm
LSI Logic AB
♦ Tel: 46.8.444.15.00
Fax: 46.8.750.66.47

Taiwan
Taipei
LSI Logic Asia, Inc.
Taiwan Branch
Tel: 886.2.2718.7828
Fax: 886.2.2718.8869

United Kingdom
Bracknell
LSI Logic Europe Ltd
♦ Tel: 44.1344.426544
Fax: 44.1344.481039

♦ Sales Offices with Design Resource Centers

To receive product literature, visit us at http://www.lsilogic.com

ISO 9000 Certified

Printed on Recycled Paper

GT
Printed in USA
Order No. R15012
Doc. No. DB08-000130-00

This document is preliminary. As such, it contains data derived from functional simulations and performance estimates. LSI Logic has not verified the functional descriptions or electrical and mechanical specifications using production parts.

The LSI Logic logo design and G12 are trademarks or registered trademarks of LSI Logic Corporation. All other brand and product names may be trademarks of their respective companies.

LSI Logic Corporation reserves the right to make changes to any products and services herein at any time without notice. LSI Logic does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by LSI Logic; nor does the purchase, lease, or use of a product or service from LSI Logic convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual property rights of LSI Logic or of third parties.