

These drawings and specifications are the property of Densitron International and may not be reproduced, copied or used without written permission		REVISIONS			
		REV.	DESCRIPTION	DATE	APPROVED
<p> 1. Specification subject to change without notice. 2. All dimensions and specifications apply to standard modules. This information may vary for modules with optional features. 3. All dimensions are in millimetres. 4. Precautions: These precautions apply equally to modules from all makers, not just Densitron. Violation of these guidelines may void the warranty and can cause problems ranging from erratic operation to catastrophic display failure. </p> <p><i>Handling precautions:</i></p> <ul style="list-style-type: none"> ◆ This device is susceptible to Electro-Static Discharge (ESD) damage. Observe Anti-Static precautions. <p><i>Power supply precautions:</i></p> <ul style="list-style-type: none"> ◆ Identify and, at all times, observe absolute maximum ratings for both logic and LC drivers. Note that there is some variance between models. ◆ Prevent the application of reverse polarity to VDD and VSS, however briefly. ◆ Use a clean power source free from transients. Power up conditions are occasionally “jolting” and may exceed the maximum ratings of the module. ◆ The +5V power of the module should also supply the power to all devices that may access the display. Don’t allow the data bus to be driven when the logic supply to the module is turned off. ◆ DO NOT install a capacitor between the VO (contrast) pin and ground. VDD must, at all times, exceed the VO voltage level. The capacitor combines with the contrast potentiometer to form an R-C network which “holds-up” VO, at power-down, possibly damaging the module. <p><i>Operating precautions:</i></p> <ul style="list-style-type: none"> ◆ DO NOT plug or unplug the module when the system is powered up. ◆ Minimise the cable length between the module and host MPU. (Recommended max. length 30 cm). ◆ For models with EL backlights, do not disable the backlight by interrupting the HV line. Unloaded inverters produce voltage extremes that may arc within a cable or at the display. ◆ Operate the module within the limits of the modules temperature specifications. <p><i>Mechanical / Environmental precautions:</i></p> <ul style="list-style-type: none"> ◆ Improper soldering is the major cause of module difficulty. Use of flux cleaner is not recommended as they may seep under the elastomeric connection and cause display failure. Densitron recommends the use of Kester “245” no-clean solder. ◆ Mount the module so that it is free from torque and mechanical stress. ◆ Surface of LCD panel should not be touched or scratched. The display front surface is an easily scratched, plastic polariser. Avoid contact and clean only when necessary with soft, absorbent cotton dampened with petroleum benzene. ◆ ALWAYS employ anti-static procedure while handling the module. ◆ Prevent moisture build-up upon the module and observe the environmental constraints for storage temperature and humidity. ◆ DO NOT store in direct sunlight. ◆ If leakage of the liquid crystal material should occur, avoid contact with this material, particularly ingestion. If the body or clothing becomes contaminated by the liquid crystal material, wash thoroughly with water and soap. <p>Notes: (unless otherwise specified)</p>					
Unless otherwise specified: Dimensions are mm Tolerances are: X = ± 3 0.X = ± 0.5 0.XX = ± 0.05	APPROVALS	DATE	DENSITRON EUROPE LTD BIGGIN HILL, ENGLAND		
	DRAWN				
	CHECKED		TITLE	33 X 100 GRAPHIC LCD MODULE	
	ISSUED		DWG.NO.	LM4900	SHEET 1 of 9

1.0 DESCRIPTION

Dot matrix display module consisting of a Liquid Crystal Display, CMOS controller-driver LSI, printed circuit board, edge type Light Emitting Diode (LED) backlight and FFC cable.

Available LC fluids types are: NTN (supertwisted nematic)

Features fast 8-bit parallel interface, on-board negative voltage generation, software contrast control, low power standby function and other useful software command functions.

Note: type of parallel interface is determined by hardware settings at the factory and must be specified when ordering. See Section 13.0 'PART NUMBER DESCRIPTION FOR AVAILABLE OPTIONS'.

2.0 MECHANICAL CHARACTERISTICS

Item	Specifications	Unit
Package Dimensions	75.0 x 35.0 x 8.6	mm
Display format	100x33 pixels	-
Character font format	n/a	dots
Driving method	1/33 duty, 1/6 bias	duty, bias
Dot size	0.56 x 0.62	mm
Dot pitch	0.6 x 0.66	mm
Character Size	n/a	mm
Active display area	59.96 x 21.74	mm
Viewing area	67.15 x 25.0	mm
Weight	20 approx.	g

Notes:W-Width;H-Height;D-Depth.

3.0 ABSOLUTE MAXIMUM RATINGS

VSS=0V;Ta=25°C

Item	Symbol	NTN		NTN-H		Unit
		Min.	Max.	Min.	Max.	
Logic supply voltage	VDD-VSS	0	7	-	-	V
LC driver supply voltage	VDD-VO	0	6	-	-	V
Operating temperature	TOP	-10	+60	-	-	°C
Storage temperature (Note 1)	TST	-20	+70	-	-	
Humidity: Operating (@40°C)	-	-	85%	-	-	RH (Note 2)
Non-operating (@40°C)	-	-	95%	-	-	RH (Note 2)

Notes: 1: Tested to 100 hrs.
2: Refers to non-condensing conditions.

4.0 ELECTRICAL CHARACTERISTICS

VDD=5±0.25V;Ta=25°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input "High" voltage	VIH	-	0.7 x Vdd	-	VDD	V
Input "Low" voltage	VIL	-	Vss	-	0.3 x Vdd	V
Power supply current	IDD	VDD=5.0V	-	1	-	mA

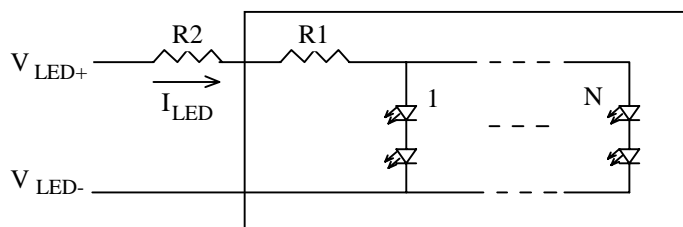
5.0 RECOMMENDED LC DRIVE VOLTAGE (VDD-VO)

Display contrast is software selectable via the controller (see 'Electronic Volume Register Set' in Section 8).

6.0 BACKLIGHT SPECIFICATIONS:

T_a=20°C,60%RH,Darkroom.

Item	Symbol	Typ.	Max	Unit
LED input voltage	V _{LED}	6	8	V
LED input current	I _{LED}	90	180	mA
Built-in current limiting resistor	R1	n/a	-	Ohm,W
External current limiting resistor	R2	10 (V _{dd} =5V) (V _{dd} =3V)	-	Ohm, W
Number of nodes	N	6	-	-



7.0 INTERFACE DESCRIPTION

Pin No	Symbol	I/O	Function
1	$\overline{\text{CS1}}$	I	Chip Select 1 (active low)
2	CS2	I	Chip Select 2
3	E ($\overline{\text{RD}}$)	I	Enable clock (6800 MPU) Read (8080 MPU)
4	DB0	I/O	Data bits 0 - 5
5	DB1	I/O	
6	DB2	I/O	
7	DB3	I/O	
8	DB4	I/O	
9	DB5	I/O	
10	A0	I	Command/display data flag input. This is connected to the LSB of the MPU address bus <ul style="list-style-type: none"> When LOW, the data on DB0 – DB7 is command data When HIGH, the data on DB0 – DB7 is display data
11	DB6	I/O	Data bit 6
12	R/ $\overline{\text{W}}$	I	Read/ $\overline{\text{Write}}$ (6800 MPU) $\overline{\text{Write}}$ (8080 MPU)
13	DB7	I/O	Data bit 7
14	V _{ss}	-	Ground
15	$\overline{\text{RES}}$	I	Reset (active low)
16	V _{dd}	-	Power supply
17	LED-	-	LED backlight cathode
18	LED+	-	LED backlight anode

8.0 COMMAND SET

Note: this command set is for 80-series MPU.

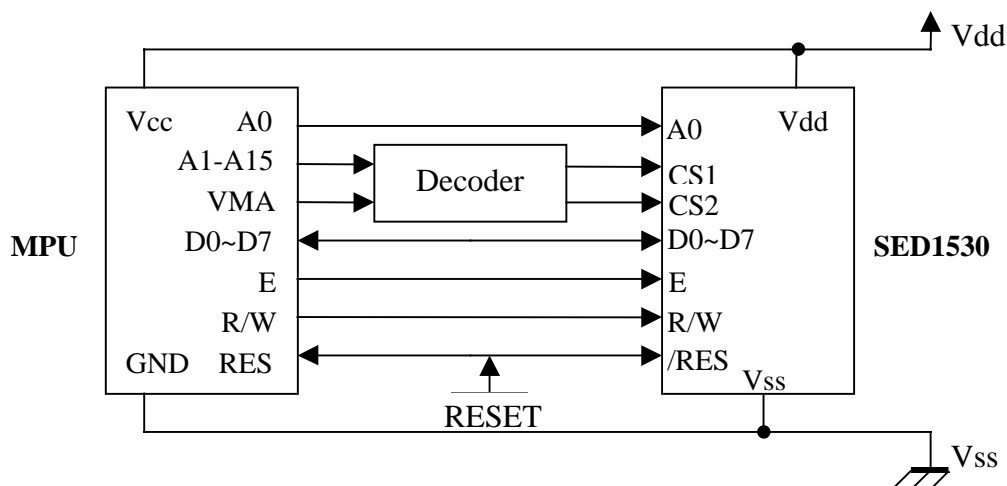
Command	Code											Function
	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	Turns the LCD display on and off. “0” : OFF “1” : ON
Display start line set	0	1	0	0	1	Display start address						Determines the RAM display line displayed to COM0
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page to the page address register
Column address set, first 4 bits	0	1	0	0	0	0	1	Most significant column address bits				Sets the 4 most significant bits of the display RAM column address to the register
Column address set, last 4 bits	0	1	0	0	0	0	0	Least significant column address bits				Sets the 4 least significant bits of the display RAM column address to the register
Status read	0	0	1	Status				0	0	0	0	Read status data.
Write display data	1	1	0	Write data								Writes to the display RAM
Read display data	1	0	1	Read data								Reads from the display RAM
ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the relationship between the display RAM address and the SEG output “0” : Normal “1” : Reverse
Display: Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0	Sets ‘inverted video mode’. “0” : Normal “1” : Reverse
Display: All Pixel Lit: On/Off	0	1	0	1	0	1	0	0	1	0	0	Display: All pixels lit “0” : Normal “1” : all pixels ON
LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage ratio
Read/Modify/Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address counter by 1 when write, zero when read
End	0	1	0	1	1	1	0	0	0	1	0	Gets out of read/modify/write mode
Reset	0	1	0	1	1	1	0	1	1	1	0	Internal reset
Output mode register set	0	1	0	1	1	0	0	0	*	*	*	Selects the direction of the COM output scan * = disabled
Power control set	0	1	0	0	0	1	0	1	1	1	1	Switches internal power supply ON
Electronic volume register set	0	1	0	1	0	0	Electronic volume level					Sets LCD contrast. Recommend 00101 for 5V version at 25 °C.
Standby set	0	1	0	1	0	1	0	1	1	0	0	Selects the standby mode “0” : OFF “1” : ON
Power save												A composite command with display: OFF and display: All pixels ON.

NOTE:

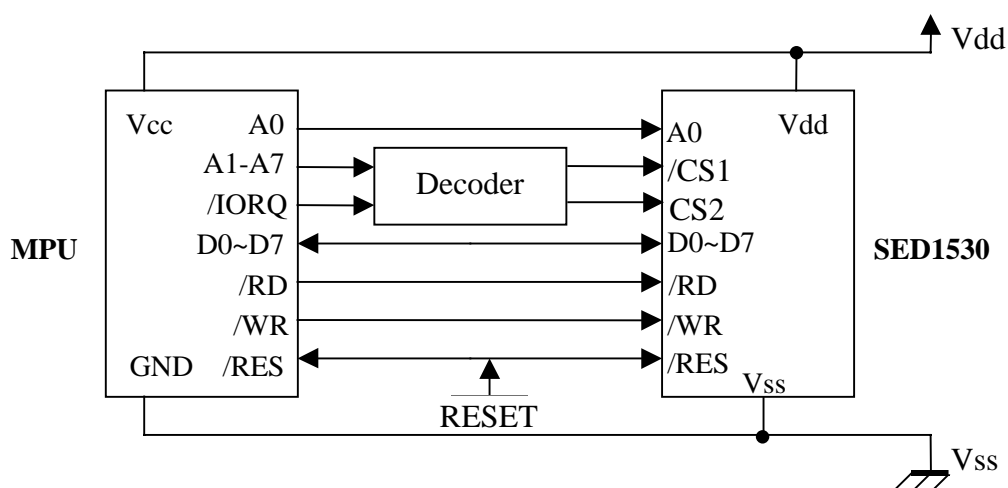
1. ‘ADC select’ must be set BEFORE ‘Display ON’ command.
2. Do not use any command that is not described above, or a system malfunction may result.
3. For a detailed description of the SED1530 controller-driver IC refer to Seiko-Epson manual (available from Epson and Densitron websites).

9.0 BLOCK DIAGRAM

6800 series MPU

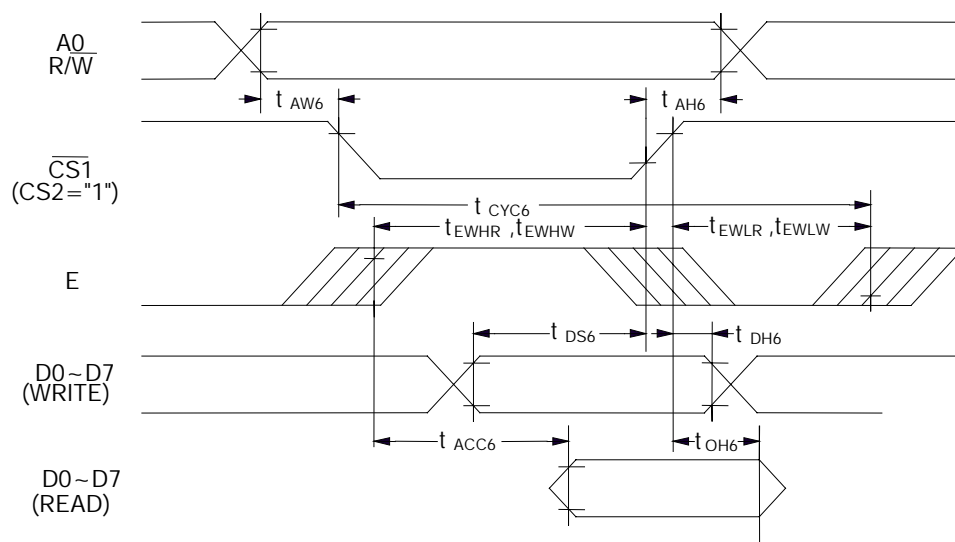


8080 MPU



10.0 TIMING CHARACTERISTICS

6800 MPU



VDD = 5.0V ± 10%, T _a = - 10 to 85 °C						
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		t_{CYC6}		200	-	ns
Address set up time	A0	t_{AW6}		10	-	ns
Address hold time	R/ \overline{W}	t_{AH6}		10	-	ns
Data setup time	D0 ~ D7	t_{DS6}		20	-	ns
Data hold time		t_{DH6}		10	-	ns
Output disable time		t_{OH6}	CL=100pF	10	50	ns
Access time		t_{ACC6}		-	70	ns
Enable H	Read	E	t_{EWHR}	77	-	ns
Pulse width	Write		t_{EWHW}	22	-	ns
Enable L	Read	E	t_{EWLR}	117	-	ns
Pulse width	Write		t_{EWLW}	172	-	ns

VDD=3.0V, Ta = - 10 to 85 C						
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		t _{CYC6}		450	-	ns
Address setup time	A0	t _{AW6}		25	-	ns
Address hold time	R/ \overline{W}	t _{AH6}		25	-	ns
Data setup time	D0 ~ D7	t _{DS6}	CL=100pF	40	-	ns
Data hold time		t _{DH6}		20	-	ns
Output disable time		t _{OH6}		20	50	ns
Access time		t _{ACC6}		-	70	ns
Enable H Pulse width	Read	E		194	-	ns
	Write			44	-	ns
Enable L Pulse width	Read	E		244	-	ns
	Write			394	-	ns

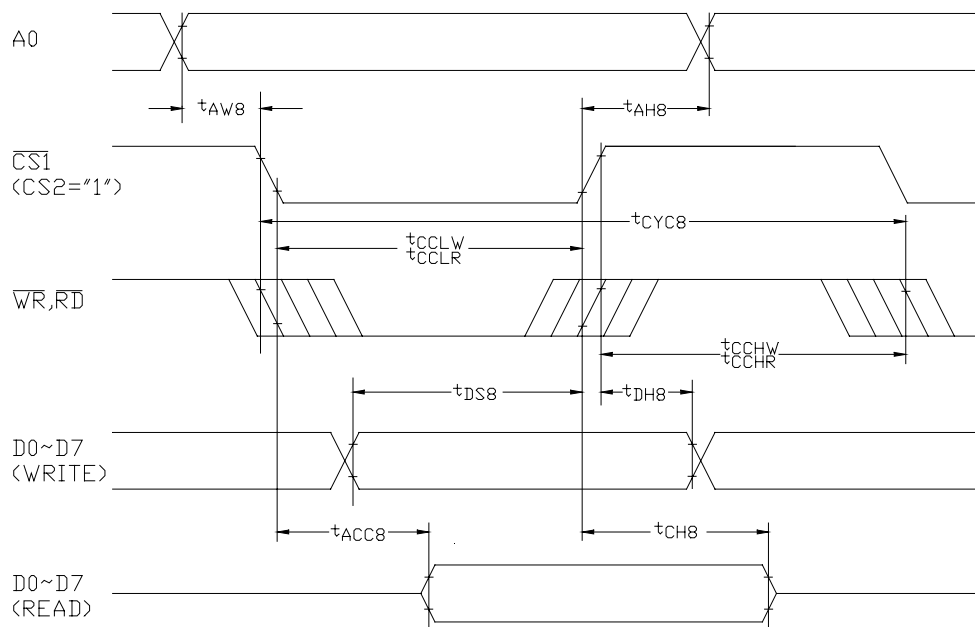
*1. The input signal rise time and fall time (tr, tf) are specified at 15 ns or less. When the cycle time is used at high speed, the specification is

tr + tf ≤ (t_{CYC6} - t_{EHLW} - t_{EHLW}) or is tr + tf ≤ (t_{CYC6} - t_{EHLR} - t_{EHLR})

*2. All timings are specified based on 20% and 80% of V_{DD}.

*3. t_{EHLR} and t_{EHLW} are specified by the overlap period of CS1 = "0" (CS2 = "1") and E = "1" level.

8080 MPU



V _{DD} =5V±10%, Ta= -10 °C ~ +60 °C						
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0, CS	t _{AH8}		10		nS
Address setup time		t _{AW8}		10		
System cycle time		t _{CYC8}		166		
Control L pulse width (WR)	\overline{WR}	t _{CCLW}		30		
Control L pulse width (RD)	\overline{RD}	t _{CCLR}		70		
Control H pulse width (WR)	\overline{WR}	t _{CCHW}		100		
Control H pulse width (RD)	\overline{RD}	t _{CCHR}		70		
Data setup time		t _{DS8}		20		
Data hold time		t _{DH8}		10		
/RD access time	D0~D7	t _{ACC8}	C _L =100pF		70	
Output disable time		t _{CH8}		10	50	

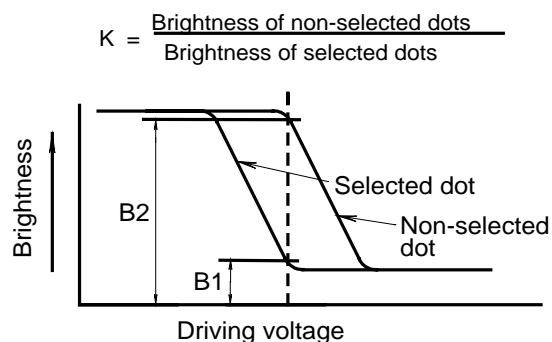
$V_{DD} = 3V \pm 10\%$, $T_a = -10^\circ C \sim +60^\circ C$						
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0, CS	t_{AH8}		19		nS
Address setup time		t_{AW8}		15		
System cycle time		t_{CYC8}		450		
Control L pulse width (WR)	\overline{WR}	t_{CCLW}		60		
Control L pulse width (RD)	\overline{RD}	t_{CCLR}		140		
Control H pulse width (WR)	\overline{WR}	t_{CCHW}		200		
Control H pulse width (RD)	\overline{RD}	t_{CCHR}		140		
Data setup time		t_{DS8}		40		
Data hold time		t_{DH8}		15		
/RD access time	D0~D7	t_{ACC8}	$C_L = 100pF$		140	
Output disable time		t_{CH8}		10	100	

Notes: 1. $t_r + t_f \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ at all times.
2. For timing purposes, LOW=20% Vdd, HIGH=80% Vdd.
3. READ/WRITE operation is performed while CS (/CS1 and CS2) is active and RD (WR) signal is LOW.

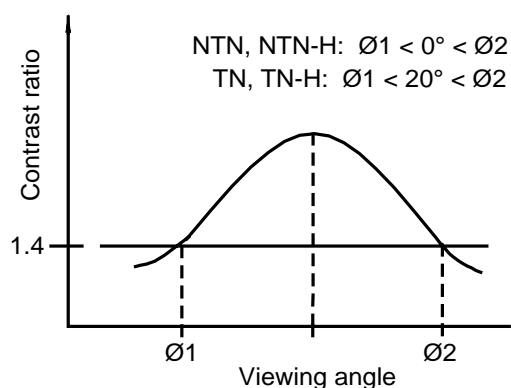
11.0 OPTICAL CHARACTERISTICS

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Contrast ratio STN	K	$\theta = 20^\circ \theta = 0^\circ$	5	-	-	-
Viewing angle STN	θ	$\theta = 0^\circ K \geq 1.4$ $\theta = 20^\circ K = 1.4$	40 ± 30	-	-	Deg. Deg.
Response time Rise	t_r	$\theta = 20^\circ \theta = 0^\circ$	-	150	250	mS
Fall	t_f	$\theta = 20^\circ \theta = 0^\circ$	-	150	250	mS

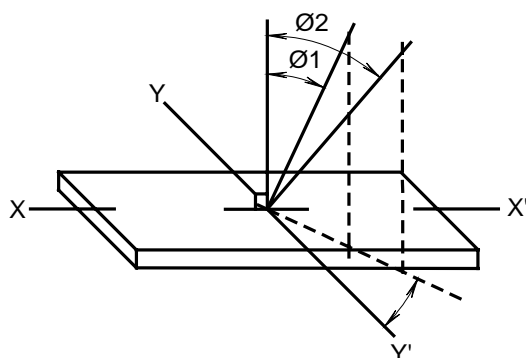
DEFINITION OF CONTRAST RATIO (K)



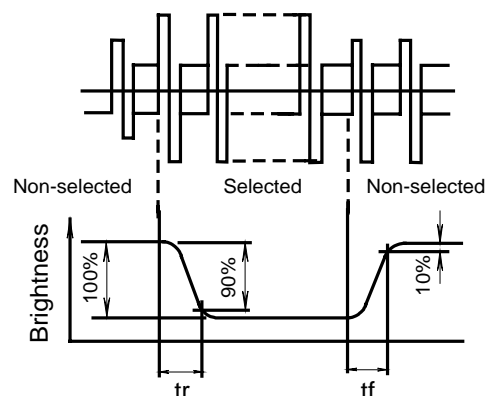
CONTRAST VERSUS VIEWING ANGLE



DEFINITION OF ANGLES θ AND

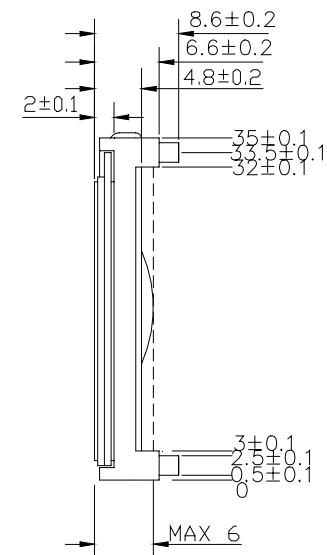
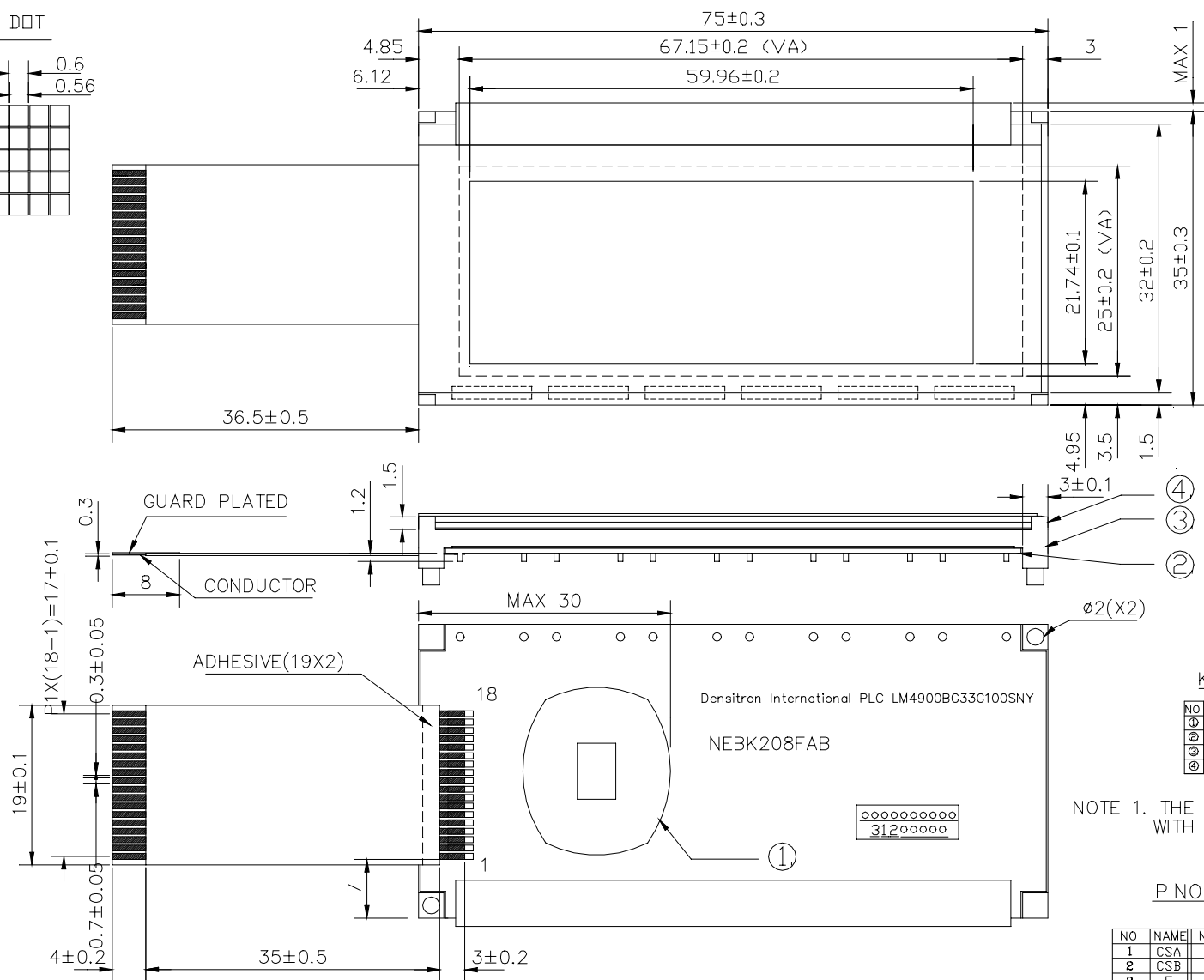
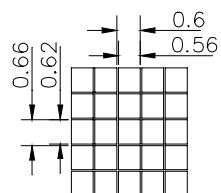


DEFINITION OF OPTICAL RESPONSE



12.0 DRAWING

DETAIL DOT



LABEL



KEY PART LIST

NO	NAME	NUMBER	SPEC
①	LSI	1	SED1530DOA
②	PWB	1	FR-4 0.6t
③	LED	1	PLASTIC MOULDING
④	LCD	1	

NOTE 1. THE LCD IS STN POSITIVE TYPE
WITH LED BACK LIGHT

PINOUT

NO	NAME	NO	NAME
1	CSA	10	A0
2	CSB	11	DB6
3	E	12	R/W
4	DB0	13	DB7
5	DB1	14	VSS
6	DB2	15	/RES
7	DB3	16	VDD
8	DB4	17	LED-
9	DB5	18	LED+

The Tolerance Unspecified	
below 6	±0.15
6 ~ 18	±0.20
18 ~ 50	±0.25
50 ~ 125	±0.30
above 125 add 0.1 per 50	
Angle	±1°

13.0 PART NUMBER DESCRIPTION FOR AVAILABLE OPTIONS

LM4900①②33G100③④⑤/X/Y

①

Polariser Type

B = Transflective: light background with backlight

②

LED Backlight Color

G = Yellow-green (standard)

③

Fluid Type and Power Supply

S = NTN with +5VDC operation

④

Fluid Type

N = STN

⑤

Background Color for STN Fluid

G = Gray background

Y = Yellow background

/X

Operating Voltage

Blank = 5V DC

/3V = 3V DC

/Y

Interface Type

Blank = 6800 MPU

/80 = 8080 MPU