REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED

1. **Specification subject to change without notice.**
2. **All dimensions and specifications apply to standard modules. This information may vary for modules with optional features.**
3. **All dimensions are in millimetres.**
4. **Precautions: These precautions apply equally to modules from all makers, not just Densitron. Violation of these guidelines may void the warranty and can cause problems ranging from erratic operation to catastrophic display failure.**

Handling precautions:

- This device is susceptible to Electro-Static Discharge (ESD) damage. Observe Anti-Static precautions.

Power supply precautions:

- Identify and, at all times, observe absolute maximum ratings for both logic and LC drivers. Note that there is some variance between models.
- Prevent the application of reverse polarity to VDD and VSS, however briefly.
- Use a clean power source free from transients. Power up conditions are occasionally "jolting" and may exceed the maximum ratings of the module.
- The +5V power of the module should also supply the power to all devices that may access the display. Don't allow the data bus to be driven when the logic supply to the module is turned off.
- DO NOT install a capacitor between the VO (contrast) pin and ground. VDD must, at all times, exceed the VO voltage level. The capacitor combines with the contrast potentiometer to form an R-C network which "holds-up" VO, at power-down, possibly damaging the module.

Operating precautions:

- DO NOT plug or unplug the module when the system is powered up.
- Minimise the cable length between the module and host MPU. (Recommended max. length 30 cm).
- For models with EL backlights, do not disable the backlight by interrupting the HV line. Unloaded inverters produce voltage extremes that may arc within a cable or at the display.
- Operate the module within the limits of the modules temperature specifications.

Mechanical / Environmental precautions:

- Improper soldering is the major cause of module difficulty. Use of flux cleaner is not recommended as they may seep under the elastomeric connection and cause display failure. Densitron recommends the use of Kester "245" no-clean solder.
- Mount the module so that it is free from torque and mechanical stress.
- Surface of LCD panel should not be touched or scratched. The display front surface is an easily scratched, plastic polariser. Avoid contact and clean only when necessary with soft, absorbent cotton dampened with petroleum benzene.
- ALWAYS employ anti-static procedure while handling the module.
- Prevent moisture build-up upon the module and observe the environmental constraints for storage temperature and humidity.
- DO NOT store in direct sunlight.
- If leakage of the liquid crystal material should occur, avoid contact with this material, particularly ingestion. If the body or clothing becomes contaminated by the liquid crystal material, wash thoroughly with water and soap.

Notes: (unless otherwise specified)

Unless otherwise specified: Dimensions are mm Tolerances are: X = ± 3 0.X = ± 0.5 0.XX = ± 0.05	APPROVALS	DATE	DENSITRON EUROPE LTD BIGGIN HILL, ENGLAND	
	DRAWN			
	CHECKED		100 X 64 PIXEL MINI-GRAPHIC ARRAY WITH EDGELIT LED BACKLIGHT	
	ISSUED		DWG.NO. **LM4068**	SHEET 1 of 10

1.0 DESCRIPTION

Graphic matrix display module consisting of a Liquid Crystal Display, CMOS driver and controller LSI, printed circuit board and edgelit Light Emitting Diode (LED) backlight.

Available LC fluid types are STN (supertwisted nematic) yellow. Available backlight colour: yellow-green.

Features include on-board DC/DC, temperature compensation, software contrast control, serial or 8-bit parallel interface.

2.0 MECHANICAL CHARACTERISTICS

Item	Specifications	Unit
Package Dimensions	79(W) x 53(H) x 7.9(D)	mm
Display format	100 x 64	-
Character font format	defined by on-board controller (SED1560)	dots
Driving method	1/64 duty, 1/9 bias	duty
Dot size	0.51 x 0.54	mm
Dot pitch	0.56 x 0.59	mm
Character Size	2.75 x 4.08 (user-generated 5 x 7 matrix)	mm
Active display area	55.95 x 37.71	mm
Viewing area	67 x 45.1	mm
Weight	30 approx	g

Notes: W-Width; H-Height; D-Depth.

3.0 ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V;T_a=25°C

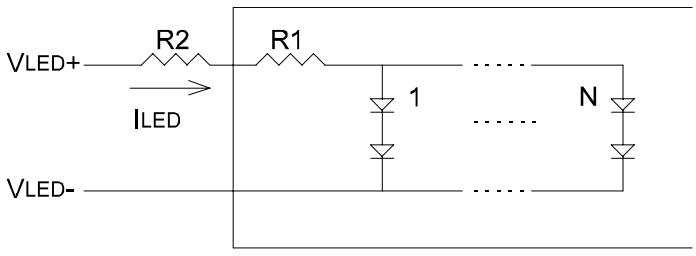
Item	Symbol	STN		Unit
		Min	Max	
Logic supply voltage	V_{DD}-V_{SS}	0	7	V
LC driver supply voltage	V_{DD}-V_O	0	6	V
Operating temperature	T_{OP}	0	+60	°C
Storage temperature (Note 1)	T_{ST}	-20	+70	
Humidity: Operating (@40°C)	-	-	85%	RH (Note 2)
Non-operating (@40°C)	-	-	95%	RH (Note 2)

Notes: 1: Tested to 100 hrs.
2: Refers to non-condensing conditions.
3. With backlight switched off.

4.0 BACKLIGHT SPECIFICATIONS:

T_a=20°C,60%RH,Darkroom.

Item	Symbol	Typ.	Max.	Unit
LED forward bias voltage	V_{FB}	4.1	4.3	Vrms
Nominal LED current	I_F	120	-	mA
LED peak current	I_P	-	180	mA
Average luminous intensity	I_V	18	-	Cd/m^2
Peak emission wavelength	λ_P	572	-	nm
Spectral line half-width	$\Delta\lambda$	30	-	nm
		n/a		Ω
Life to half initial brightness	-	10		Ω
Recommended backlight inverter	-	4		-



5.0 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Specification value			Unit
			Min	Typ	Max	
Operating voltage	V_{DD}		4.5	5.0	5.5	V
High level input voltage Low level input voltage	V_{IHC} V_{ILC}		0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}	
High level output voltage Low level output voltage	V_{OHC} V_{OLC}		0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}	
Input leakage current Output leakage current	I_{LI} I_{LO}	V_{IN}=V_{DD} or V_{SS}	–1.0 –3.0	— —	1.0 3.0	µA
Static current consumption (with backlight switched off)	I_{SSQ}		—	0.01	5	µA
Dynamic current consumption (with backlight switched off)	I_{DD}	V_{DD} = 5V, Ta=25°C	—	200	350	µA
Input pin capacitance	C_{IN}	Ta=25°C, f=1MHz	—	5.0	8.0	pF

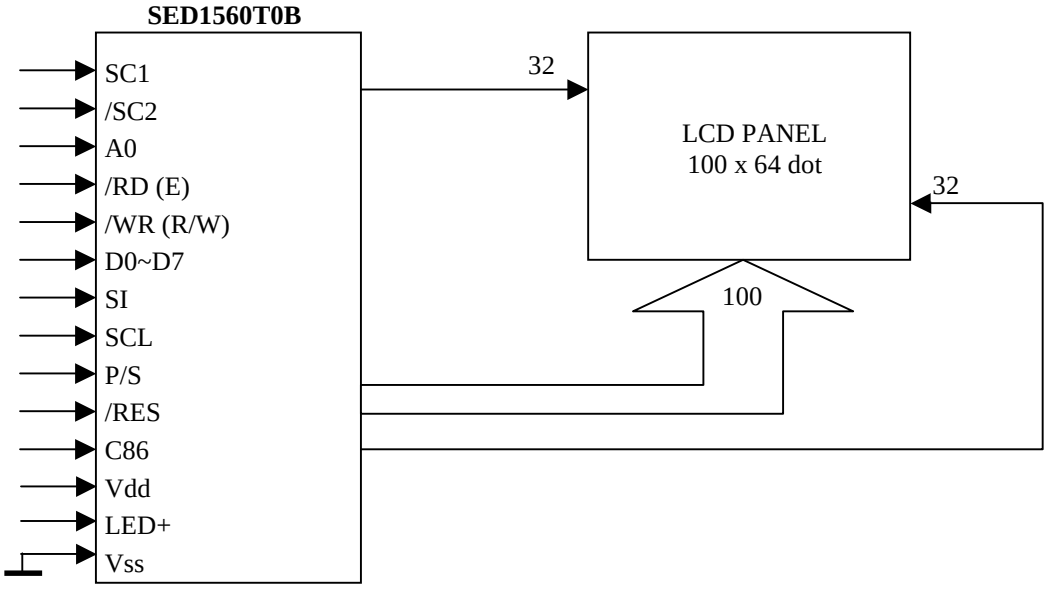
6.0 INTERFACE DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>V_{SS}</td><td>-</td><td>Ground (0V)</td></tr>
<tr><td>2</td><td>V_{DD}</td><td>-</td><td>Logic Supply Voltage (+3/+5V)</td></tr>
<tr><td>3</td><td>D7</td><td>I/O</td><td rowspan="8">Bidirectional data bus</td></tr>
<tr><td>4</td><td>D6</td><td>I/O</td></tr>
<tr><td>5</td><td>D5</td><td>I/O</td></tr>
<tr><td>6</td><td>D4</td><td>I/O</td></tr>
<tr><td>7</td><td>D3</td><td>I/O</td></tr>
<tr><td>8</td><td>D2</td><td>I/O</td></tr>
<tr><td>9</td><td>D1</td><td>I/O</td></tr>
<tr><td>10</td><td>D0</td><td>I/O</td></tr>
<tr><td>11</td><td>/CS1</td><td>I</td><td rowspan="2">Chip Select input. Data input/output is enabled when CS1 is LOW and CS2 is HIGH</td></tr>
<tr><td>12</td><td>CS2</td><td>I</td></tr>
<tr><td>13</td><td>A0</td><td>I/O</td><td>Control/Display data flag input. This is connected to the LSB of the microprocessor address bus.
• When LOW, data on D0 to D7 is command data
• When HIGH, data on D0 to D7 is display data</td></tr>
<tr><td>14</td><td>RD</td><td>I/O</td><td>Read</td></tr>
<tr><td>15</td><td>/WR</td><td>I/O</td><td>Write</td></tr>
<tr><td>16</td><td>SI</td><td>I</td><td>Serial data input</td></tr>
<tr><td>17</td><td>SCL</td><td>I</td><td>Serial Clock input. Data is read on the rising edge of CSL and converted to 8-bit parallel data</td></tr>
<tr><td>18</td><td>P/S</td><td>I</td><td>Parallel/Serial input select

<table>
<tr><th>P/S</th><th>Operating Mode</th><th>Chip Select</th><th>Data/Command</th><th>Data I/O</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>/CS1, CS2</td><td>A0</td><td>D0 ~ D7</td><td>RD, WR</td><td>-</td></tr>
<tr><td>LOW</td><td>Serial</td><td>/CS1, CS2</td><td>A0</td><td>SI</td><td>WR only</td><td>SCL</td></tr>
</table>

In serial mode, data can not be read from the RAM, and D0 to D7, RD and WR must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW</td></tr>
<tr><td>19</td><td>RES</td><td>I</td><td>Reset input. Setting this LOW initialises the LCM</td></tr>
<tr><td>20</td><td>C86</td><td>I</td><td>Microprocessor interface select input
• LOW when interfacing to 8080-series
• HIGH when interfacing to 6800-series</td></tr>
<tr><td>21</td><td>LED_A</td><td>-</td><td>Power supply for LED backlight (anode)</td></tr>
<tr><td>22</td><td>N/C</td><td>-</td><td>Not connected</td></tr>
</table>

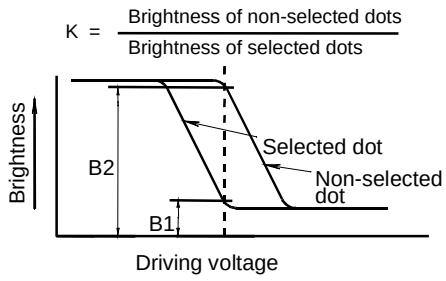
7.0 BLOCK DIAGRAM



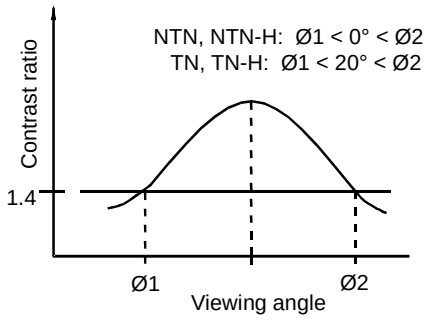
8.0 ELECTRO-OPTICAL CHARACTERISTICS

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Contrast ratio TN, TN-H		K	Ø=20° θ=0°	3	-	-	-
Contrast ratio STN		K	Ø=20° θ=0°	4	-	-	-
Contrast ratio NTN-H		K	Ø=20° θ=0°	5	-	-	-
Viewing angle	TN, TN-H	Ø2-Ø1	θ=0° K≥1.4	20	-	-	Deg.
		θ	Ø=20° K=1.4	±30	-	-	Deg.
Viewing angle	STN	Ø2-Ø1	θ=0° K≥1.4	40	-	-	Deg.
		θ	Ø=20° K=1.4	±30	-	-	Deg.
Viewing angle	NTN-H	Ø2-Ø1	θ=0° K≥1.4	40	-	-	Deg.
		θ	Ø=20° K=1.4	±40	-	-	Deg.
Response time	Rise	t_r	Ø=20° θ=0°	-	180	290	mS
	Fall	t_f	Ø=20° θ=0°	-	210	340	mS

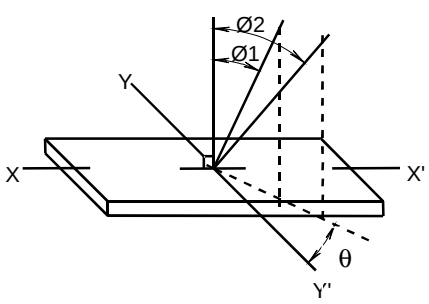
DEFINITION OF CONTRAST RATIO (K)



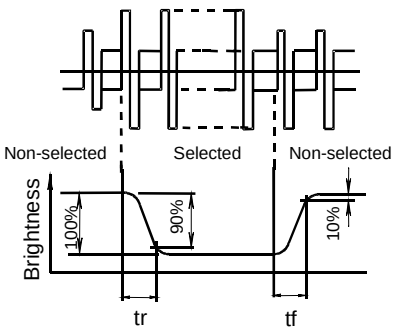
CONTRAST VERSUS VIEWING ANGLE



DEFINITION OF ANGLES Ø AND θ

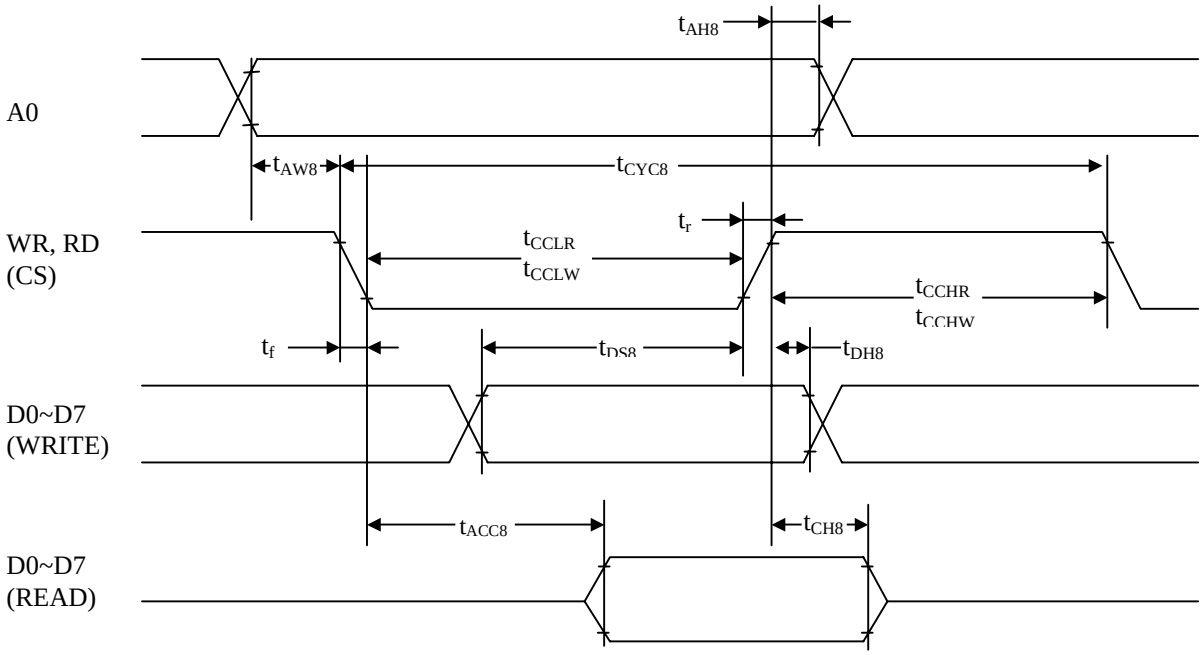


DEFINITION OF OPTICAL RESPONSE



9.0 INTERFACE TIMING CHARACTERISTICS

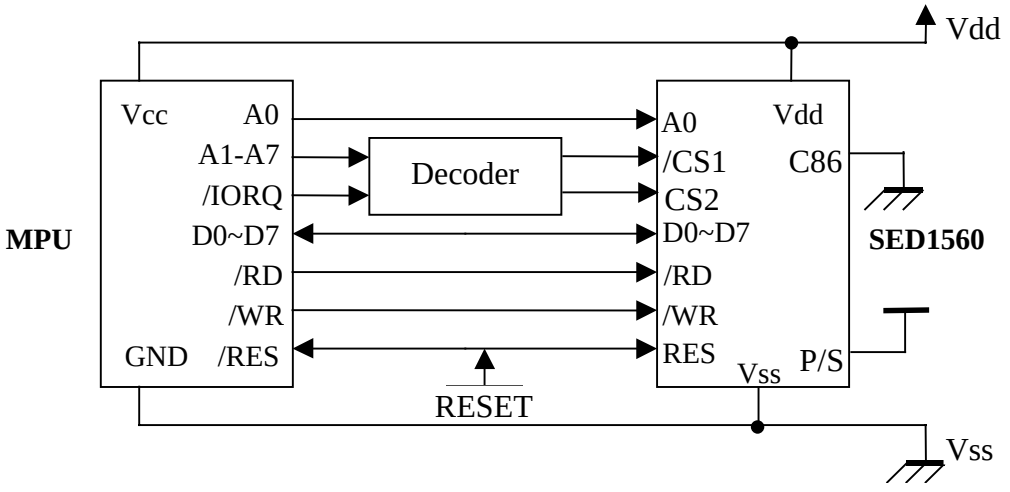
9.1 8080-SERIES MPU



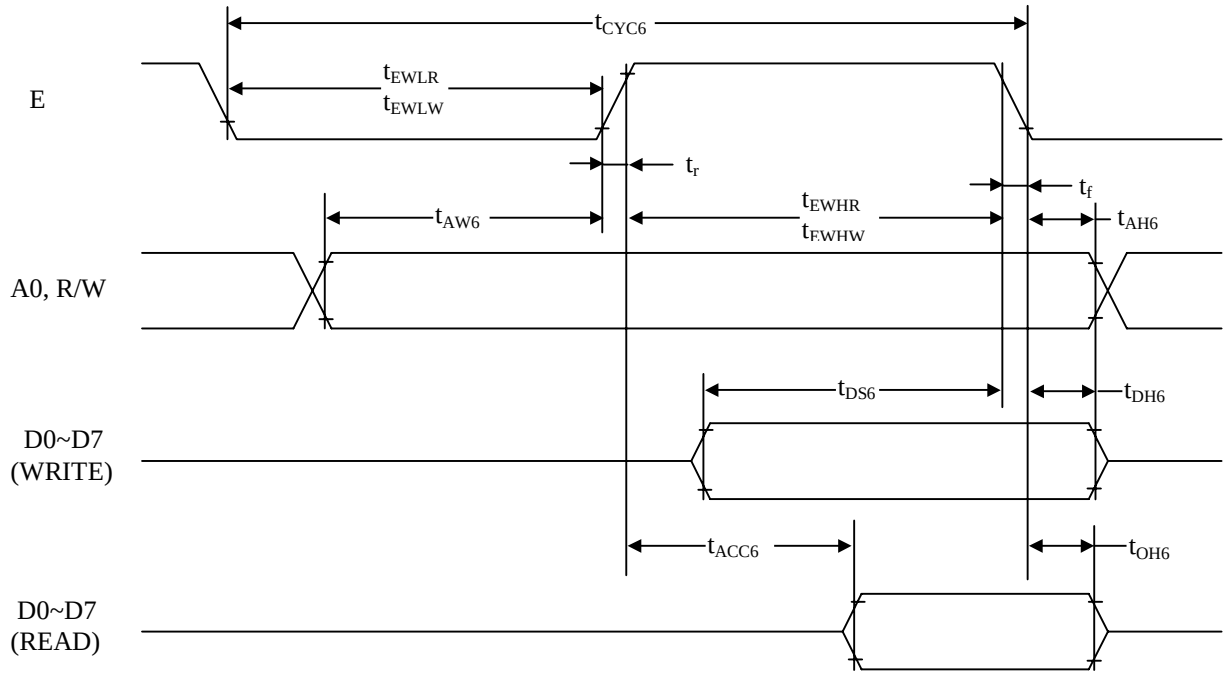
V_{DD} =5V±10%, Ta= 0 °C ~ +60 °C

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0, CS	t_{AH8}		10		nS
Address setup time		t_{AW8}		10		
System cycle time		t_{CYC8}		200		
Control L pulse width (WR)	/WR	t_{CCLW}		22		
Control L pulse width (RD)	/RD	t_{CCLR}		77		
Control H pulse width (WR)	/WR	t_{CCHW}		172		
Control H pulse width (RD)	/RD	t_{CCHR}		117		
Data setup time		t_{DS8}		20		
Data hold time		t_{DH8}		10		
/RD access time	D0~D7	t_{ACC8}	C_L =100pF		70	
Output disable time		t_{CH8}		10	50	
Input signal change time		t_r, t_f			15	

Notes: 1. $t_r + t_f \le (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \le (t_{CYC8} - t_{CCLR} - t_{CCHR})$ at all times.
2. For timing purposes, LOW=20% Vdd, HIGH=80%Vdd.
3. READ/WRITE operation is performed while CS (/CS1 and CS2) is active and RD (WR) signal is LOW.



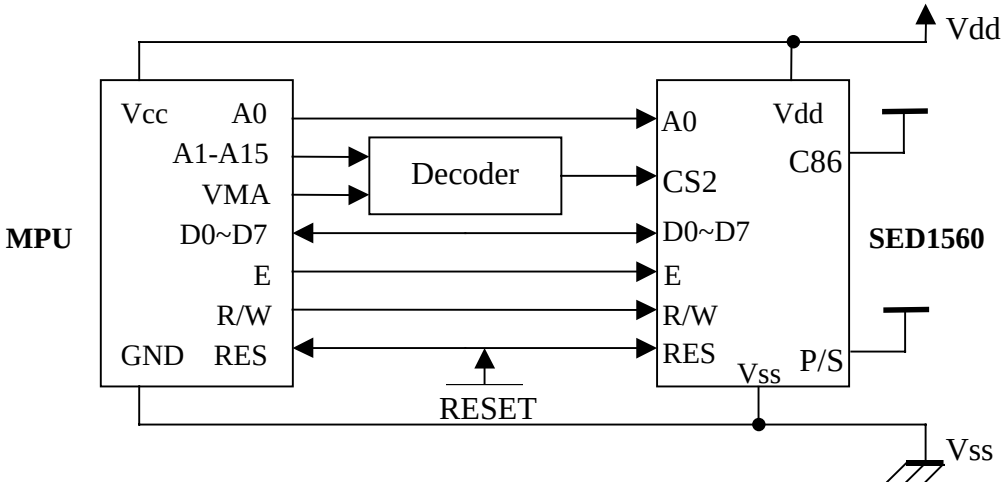
9.2 68-SERIES MPU



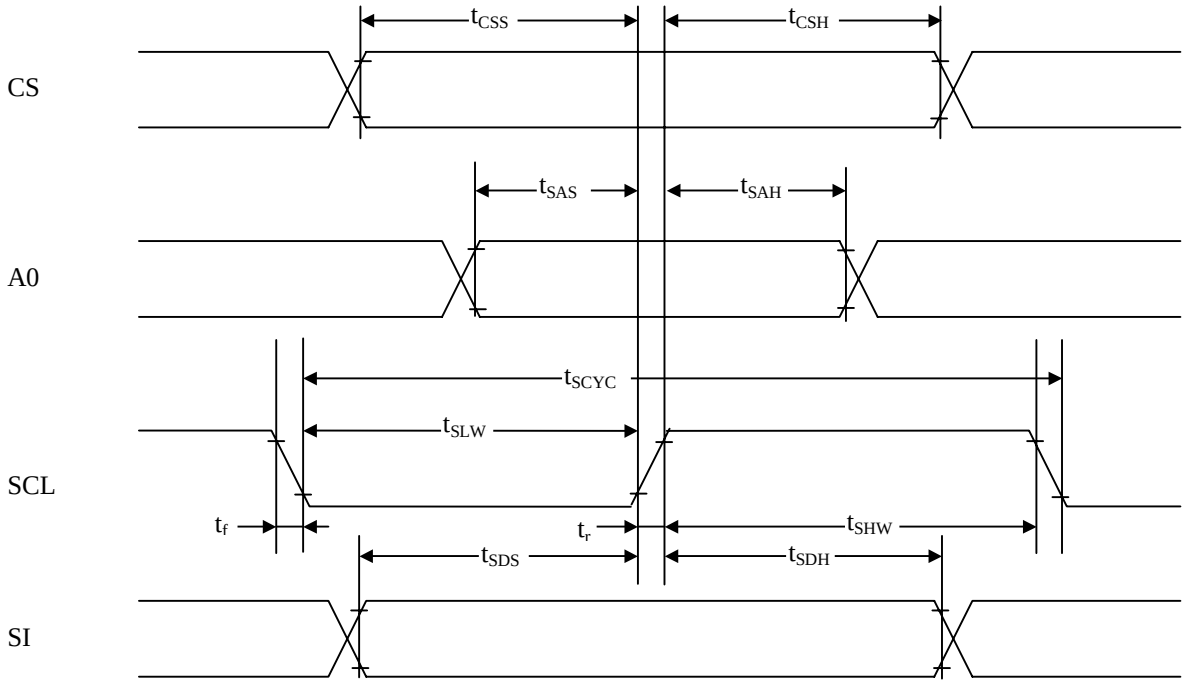
V_{DD} =5V±10%, Ta= 0 °C ~ +60 °C

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	tAH6		0	-	nS
Address setup time			tAW6		0	-	
System cycle time			tCYC6		800	-	
Data setup time		D0 to D7	tDS6		80	-	
Data hold time			tDH6		30	-	
Access time			tACC6	CL=100pF	-	280	
Output disable time			tOH6		10	200	
Enable H pulse width	READ	E	tEWHR		240	-	
	WRITE		tEWHW		120	-	
Enable L pulse width	READ	E	tEWLR		120	-	
	WRITE		tEWLW		120	-	
Input signal change time							

Notes: 1. $t_r + t_f \le (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $t_r + t_f \le (t_{CYC6} - t_{EWLR} - t_{EWHR})$ at all times.
2. For timing purposes, LOW=20% Vdd, HIGH=80%Vdd.

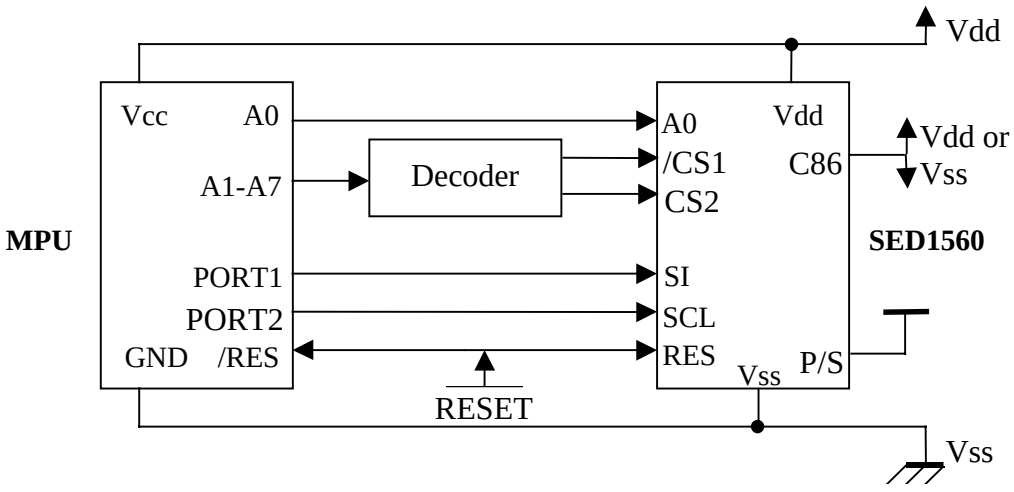


9.3 SERIAL INTERFACE



V_{DD} =5V±10%, Ta= 0 °C ~ +60 °C

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		250		nS
SCL High pulse width		t_{SHW}		75		
SCL Low pulse width		t_{SLW}		75		
Address setup time	A0	t_{SAS}		50		
Address hold time		t_{SAH}		200		
Data setup time	SI	t_{SDS}		50		
Data hold time		t_{SDH}		30		
CS-SCL time	CS	t_{CSS}		30		
		t_{CSH}		400		
Input signal change time		t_r, t_f			50	



10.0 DISPLAY COMMAND SET (8080-series MPU example)

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	Turns the LCD display ON and OFF 0: OFF 1: ON
Display START line set	0	1	0	0	1	Display start address						Load RAM line address of start display line (COM 0) into start line register
Page address set	0	1	0	1	0	1	1	Page address				Load page RAM page address into page address register
Column address set: higher-order 4 bits	0	1	0	0	0	0	1	High-order column address				Load 4 higher-order bits of RAM column address into column address register
Column address set: lower- order 4 bits	0	1	0	0	0	0	0	Low-order column address				Load 4 lower-order bits of RAM column address into column address register
Status read	0	0	1	Status bits				0	0	0	0	Read LCD controller status
Display data write	1	1	0	Write data								Write data to display RAM location specified by column address and page address registers
Display data read	1	0	1	Read data								Reads data from display RAM
ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Set column scan direction 0: normal 1: reversed
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Set normal/inverted display mode 0: normal 1: reversed
All segments ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Toggle between normal display operation and ALL SEGMENTS ON 0: Normal display 1: All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1) 0: 1/48 1: 1/64
Duty + 1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2) 0: Normal 1: Duty + 1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed n-lines				Sets the period for inverting LCD drive waveform in terms of a number of lines (2-16).
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Restore normal 2-frame inversion period
Read Modify write	0	1	0	1	1	1	0	0	0	0	0	Change data read mode: column address no longer incremented automatically by Read Display Data command
End	0	1	0	1	1	1	0	1	1	1	0	Cancel Read Modify write mode
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Output status register set	0	1	0	1	1	0	0	Output status				Sets COM/SEG function of dual outputs
Built-in DC/DC generator ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: DC generator OFF 1: DC generator ON
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Complete the turn -on sequence
Software contrast control register set	0	1	0	1	0	0	Contrast control value					Sets output voltage for contrast control in contrast control register
Power save												A complex command to turn off the display while preserving display content

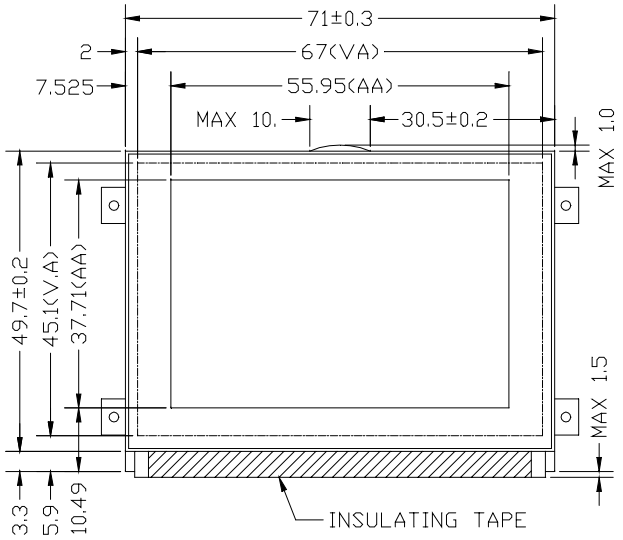
Note: RESET signal

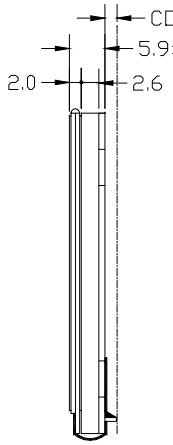
When power is turned ON, the display is initialised on the rising edge of /RES. Initial settings are as follows:

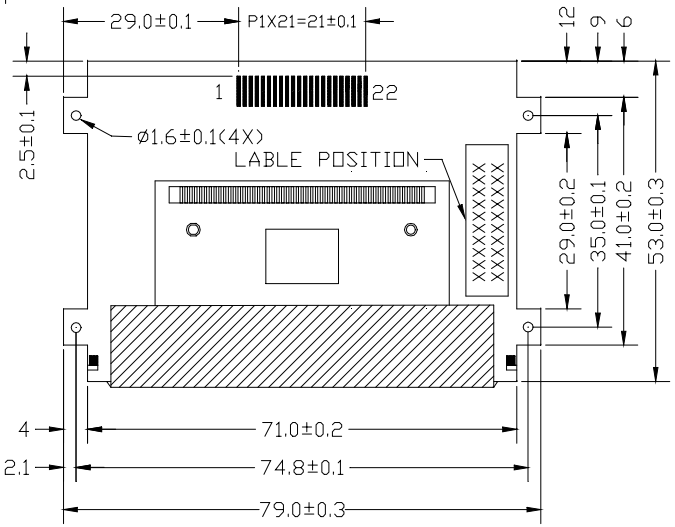
Display : OFF
Duty cycle : 1/64
Internal power supply : OFF
Column address counter : 0
n-line inversion register : 16
Display mode : Normal
ADC select : Normal (D0 = L)
Serial interface register data: Cleared
Page address register : Page 0
Contrast control register : 0
n-line inversion : OFF
Read/write modify : OFF
Display initial line register : Line 1
Output selection circuit : Case 6

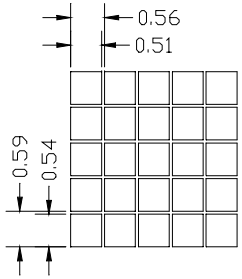
/RES must be LOW for at least 1 μS to reset the controller correctly. Normal operation starts 1 μS after the rising edge of /RES.

11.0 DRAWING

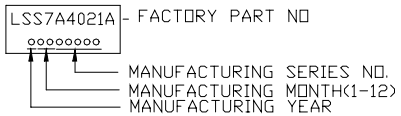








MANUFACTURE LABEL



NOTE:

1.LCD DISPLAY MODE:STN/YELLOW-GREEN/TRANSFLECTIVE TYPE.
2.VIEWING ANGLE: 6 O'CLOCK.
3.OPERATING TEMP:0 TO 50 DEGREE.
4.STORAGE TEMP:-20 TO 60 DEGREE.
5.THE LCD DRIVING CODITION IS:1/64D,1/9B,Vop=9.4V.

12.0 ENVIRONMENTAL TESTING

The test criteria for LM4064 LCM require that the module operate normally after application of the following conditions:

- High temperature operation, under normal humidity (less than 30% RH) at 50 °C for 120 hours.
- Low temperature operation, under normal humidity (less than 60% RH) at 0 °C for 120 hours (no dew).
- High temperature storage, under normal humidity (less than 30% RH) at 60 °C for 120 hours.
- Low temperature storage, under normal humidity (less than 60% RH) at –20 °C for 120 hours.
- High temperature and high humidity storage, under condition of 90% RH at 40 °C for 120 hours (no dew).
- Vibration, under the following conditions:

Frequency	: 10-55 Hz
Max. acceleration	: 5G
1 cycle time	: 1 min
Duration:	: 15 mins

- Drop impact test, 0.7 m drop to concrete floor (inside packaging).

- Expected lifetime of LM4064 module is more than 50,000 hours (under normal operating conditions).

13.0 PART NUMBER DESCRIPTION FOR AVAILABLE OPTIONS

LM4068①②64G100③④⑤/X

① **Poliriser type**
B = transflective positive (light background, with backlight)

② **LED Backlight Colour**
G = yellow-green

③ **Fluid type and Power Supply**
S = standard temperature range (0 to +50 ºC) single-rail 3V or 5V with on-board DC/DC
W = extended temperature range (-20 to +70 ºC) single-rail 3V or 5V with on-board DC/DC

④ **Fluid Type And Temperature Compensation**
C = STN with on-board temperature compensation

⑤ **Background Colour**
G = Gray background
Y = Yellow-Green background

X **Operating Voltage**
Blank = 5VDC operation
3V = 3VDC operation