REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED

1. **Specification subject to change without notice.**
2. **All dimensions and specifications apply to standard modules. This information may vary for modules with optional features.**
3. **All dimensions are in millimetres.**
4. **Precautions: These precautions apply equally to modules from all makers, not just Densitron. Violation of these guidelines may void the warranty and can cause problems ranging from erratic operation to catastrophic display failure.**

Handling precautions:

- This device is susceptible to Electro-Static Discharge (ESD) damage. Observe Anti-Static precautions.

Power supply precautions:

- Identify and, at all times, observe absolute maximum ratings for both logic and LC drivers. Note that there is some variance between models.
- Prevent the application of reverse polarity to VDD and VSS, however briefly.
- Use a clean power source free from transients. Power up conditions are occasionally "jolting" and may exceed the maximum ratings of the module.
- The +5V power of the module should also supply the power to all devices that may access the display. Don't allow the data bus to be driven when the logic supply to the module is turned off.
- DO NOT install a capacitor between the VO (contrast) pin and ground. VDD must, at all times, exceed the VO voltage level. The capacitor combines with the contrast potentiometer to form an R-C network which "holds-up" VO, at power-down, possibly damaging the module.

Operating precautions:

- DO NOT plug or unplug the module when the system is powered up.
- Minimise the cable length between the module and host MPU. (Recommended max. length 30 cm).
- For models with EL backlights, do not disable the backlight by interrupting the HV line. Unloaded inverters produce voltage extremes that may arc within a cable or at the display.
- Operate the module within the limits of the modules temperature specifications.

Mechanical / Environmental precautions:

- Improper soldering is the major cause of module difficulty. Use of flux cleaner is not recommended as they may seep under the elastomeric connection and cause display failure. Densitron recommends the use of Kester "245" no-clean solder.
- Mount the module so that it is free from torque and mechanical stress.
- Surface of LCD panel should not be touched or scratched. The display front surface is an easily scratched, plastic polariser. Avoid contact and clean only when necessary with soft, absorbent cotton dampened with petroleum benzene.
- ALWAYS employ anti-static procedure while handling the module.
- Prevent moisture build-up upon the module and observe the environmental constraints for storage temperature and humidity.
- DO NOT store in direct sunlight.
- If leakage of the liquid crystal material should occur, avoid contact with this material, particularly ingestion. If the body or clothing becomes contaminated by the liquid crystal material, wash thoroughly with water and soap.

Notes: (unless otherwise specified)

Unless otherwise specified: Dimensions are mm Tolerances are: X = ± 3, 0.X = ± 0.5, 0.XX = ± 0.05	APPROVALS	DATE	DENSITRON EUROPE LTD BIGGIN HILL, ENGLAND	
	DRAWN			
	CHECKED		96 X 16 PIXEL MINI-GRAPHIC ARRAY	
	ISSUED		DWG.NO. **LM3097**	SHEET 1 of 10

1.0 DESCRIPTION

Graphic matrix display module consisting of a Liquid Crystal Display, CMOS driver and controller LSI.

Available LC fluid types are STN (supertwisted nematic) yellow.

Features include on-board DC/DC, temperature compensation, software contrast control, serial or 8-bit parallel interface.

2.0 MECHANICAL CHARACTERISTICS

Item	Specifications	Unit
Package Dimensions	43(W) x 17.5(H) x 1.7(D)	mm
Display format	96 x 16	-
Character font format	defined by on-board controller (NJU6580)	dots
Driving method	1/16 duty	duty
Dot size	0.37 x 0.50	mm
Dot pitch	0.40 x 0.53	mm
Character Size	3.68(H) x 2.62(W) (7 x 5 user generated)	mm
Active display area	38.37 x 8.45	mm
Viewing area	40.40 x 11.00	mm
Weight	25	g

Notes: W-Width; H-Height; D-Depth.

3.0 ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V;T_a=25°C

Item	Symbol	STN		Unit
		Min.	Max.	
Logic supply voltage	V_{DD}-V_{SS}	0	7	V
LC driver supply voltage	V_{DD}-V_O	0	6	V
Operating temperature	T_{OP}	0	+50	°C
Storage temperature (Note 1)	T_{ST}	-20	+60	
Humidity: Operating (@40°C)	-	-	85%	RH (Note 2)
Non-operating (@40°C)	-	-	95%	RH (Note 2)

Notes: 1: Tested to 100 hrs.
2: Refers to non-condensing conditions.

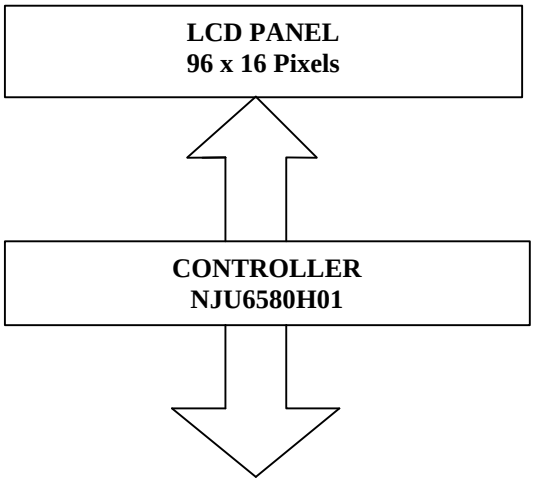
5.0 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Specification value			Unit
			Min	Typ	Max	
Operating voltage	V_{DD}		4.5	5.0	5.5	V
High level input voltage Low level input voltage	V_{IHC} V_{ILC}		0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}	
High level output voltage Low level output voltage	V_{OHC} V_{OLC}		0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}	
Input leakage current Output leakage current	I_{LI} I_{LO}	V_{IN}=V_{DD} or V_{SS}	–1.0 –3.0	— —	1.0 3.0	µA
Static current consumption (with backlight switched off)	I_{SSQ}		—	0.01	5	µA
Dynamic current consumption (with backlight switched off)	I_{DD}	V_{DD} = 5V, Ta=25°C	—	30.0		µA
Input pin capacitance	C_{IN}	Ta=25°C, f=1MHz	—	10.0		pF

6.0 PIN CONNECTIONS

Pin No.	Symbol	I/O	Function
1	NC	-	No Connection
2	T2	I	LCD Bias Voltage
3	T1	I	LCD Bias Voltage
4	SCL	I	Serial Data Clock
5	CL1	I	External Clock
6	P/S	I	Serial/Parallel Interface Select
7	RST	I	Reset
8	DREQ	O	Data Request Signal
9	CSX	I	Chip Select
10	SI	I	Serial Data
11	C86	I	MPU Interface Select
12	A0	I	Data/Instruction Select
13	R/W	I	Read/Write Select
14	E		
15	V_{DD}	Power	Logic Supply Voltage (5V)
16	DO	I/O	Tri-State Data Bus Bit 0
17	D1	I/O	Tri-State Data Bus Bit 1
18	D2	I/O	Tri-State Data Bus Bit 2
19	D3	I/O	Tri-State Data Bus Bit 3
20	D4	I/O	Tri-State Data Bus Bit 4
21	D5	I/O	Tri-State Data Bus Bit 5
22	D6	I/O	Tri-State Data Bus Bit 6
23	D7	I/O	Tri-State Data Bus Bit 7
24	V_{SS}	GND	Ground (0V)
25	V_{out}	O	Step-up Voltage
26	C1+	O	Step-up Capacitor Connection
27	C1-	O	Step-up Capacitor Connection
28	C2+	O	Step-up Capacitor Connection
29	C2-	O	Step-up Capacitor Connection
30	V_{out}	O	Step-up Voltage Output
31	Vr	I	Voltage Adjust
32	V_{DD}	Power	Logic Supply Voltage (+5V)
33	V1	Power	LCD Driving Voltage
34	V2	Power	LCD Driving Voltage
35	V3	Power	LCD Driving Voltage
36	V4	Power	LCD Driving Voltage
37	V5	Power	LCD Driving Voltage
38	NC	-	No Connection

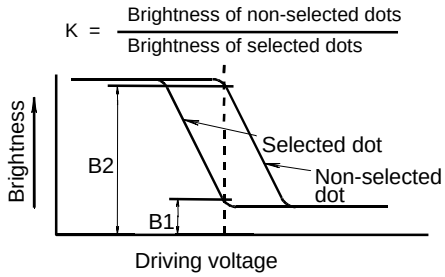
7.0 BLOCK DIAGRAM



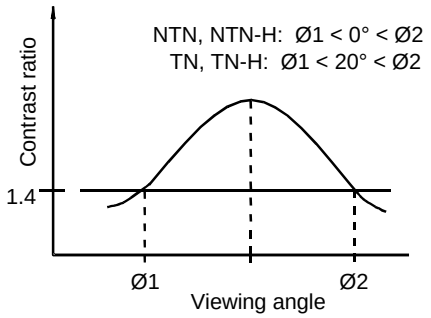
8.0 ELECTRO-OPTICAL CHARACTERISTICS

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Contrast ratio STN	K	Ø=20° θ=0°	4	5	-	-
Viewing angle STN	Ø2-Ø1	θ=0° K≥1.4	40	50	-	Deg.
	θ	Ø=20° K=1.4	-	±25	-	Deg.
Response time Rise	t_r	Ø=20° θ=0°	-	120	200	
Fall	t_f	Ø=20° θ=0°	-	140	230	

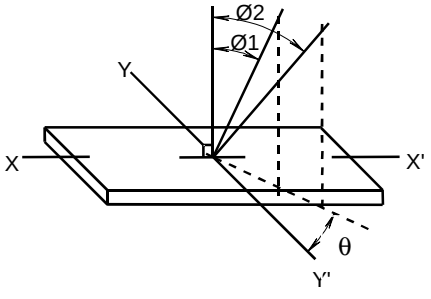
DEFINITION OF CONTRAST RATIO (K)



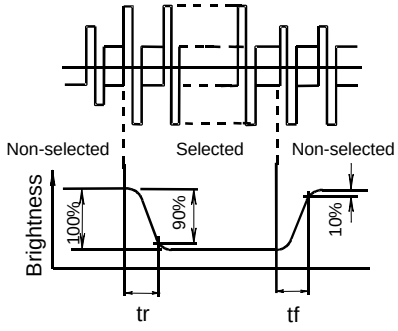
CONTRAST VERSUS VIEWING ANGLE



DEFINITION OF ANGLES Ø AND θ

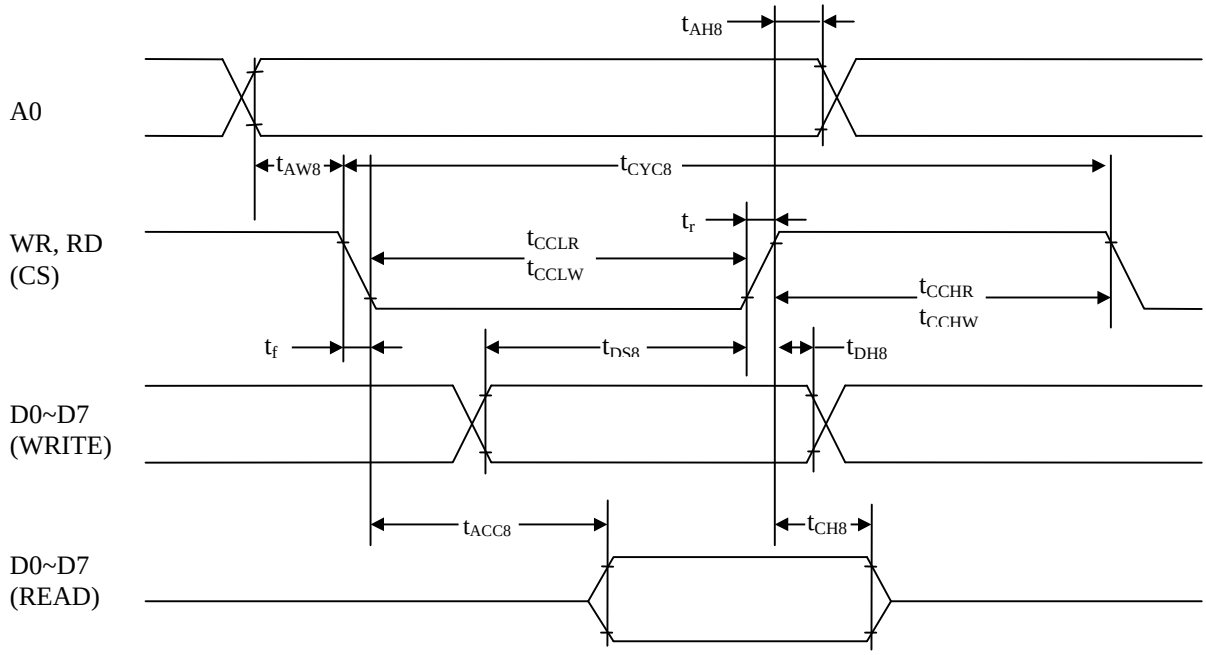


DEFINITION OF OPTICAL RESPONSE



9.0 INTERFACE TIMING CHARACTERISTICS

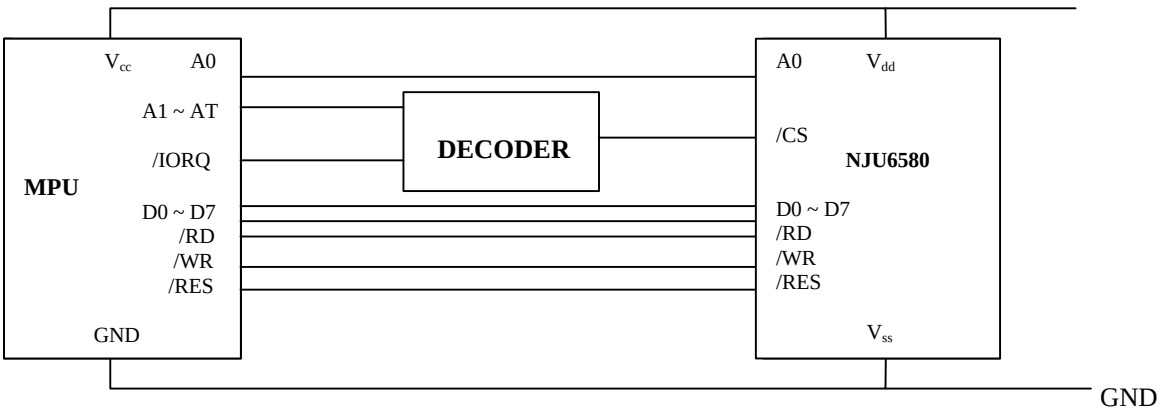
9.1 80-SERIES MPU



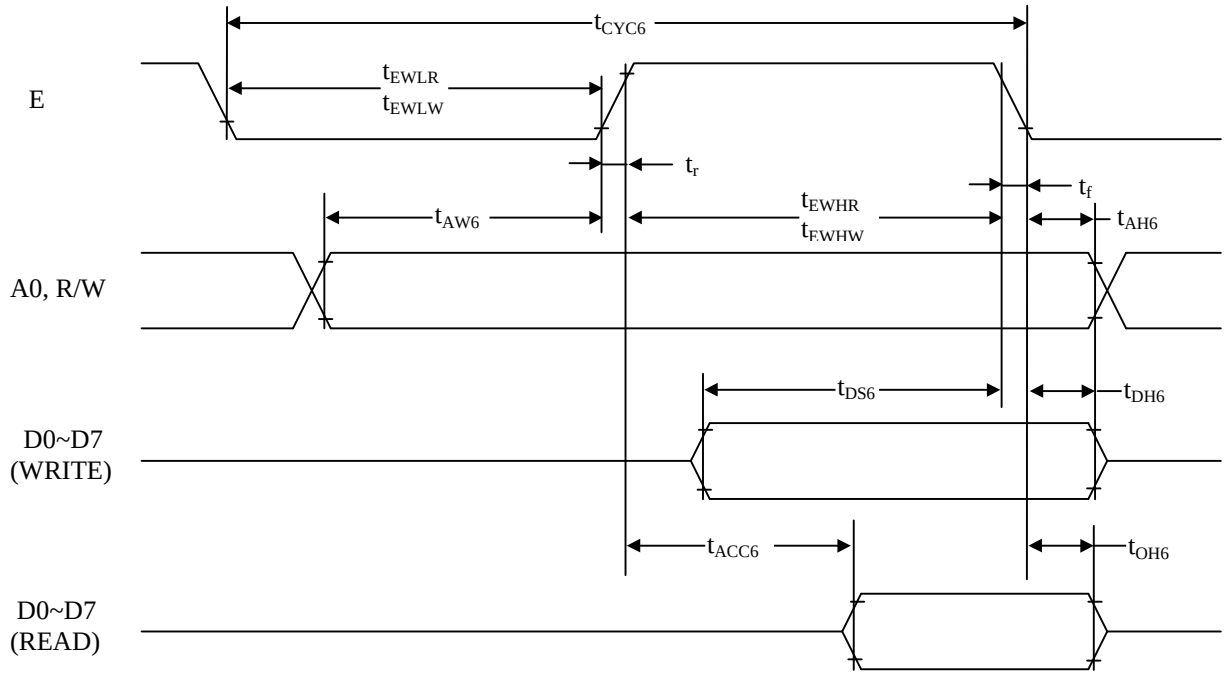
V_{DD} =5V±10%, Ta= 0 °C ~ +60 °C

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0, CS	t_{AH8}		10		nS
Address setup time		t_{AW8}		10		
System cycle time		t_{CYC8}		200		
Control L pulse width (WR)	/WR	t_{CCLW}		25		
Control L pulse width (RD)	/RD	t_{CCLR}		80		
Control H pulse width (WR)	/WR	t_{CCHW}		90		
Control H pulse width (RD)	/RD	t_{CCHR}		90		
Data setup time		t_{DS8}		60		
Data hold time		t_{DH8}		10		
/RD access time	D0~D7	t_{ACC8}	C_L =100pF		70	
Output disable time		t_{CH8}		0	30	
Input signal change time		t_r, t_f			15	

Notes: 1. $t_r + t_f \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ at all times.
2. For timing purposes, LOW=20% Vdd, HIGH=80%Vdd.
3. READ/WRITE operation is performed while CS (/CS1 and CS2) is active and RD (WR) signal is LOW.



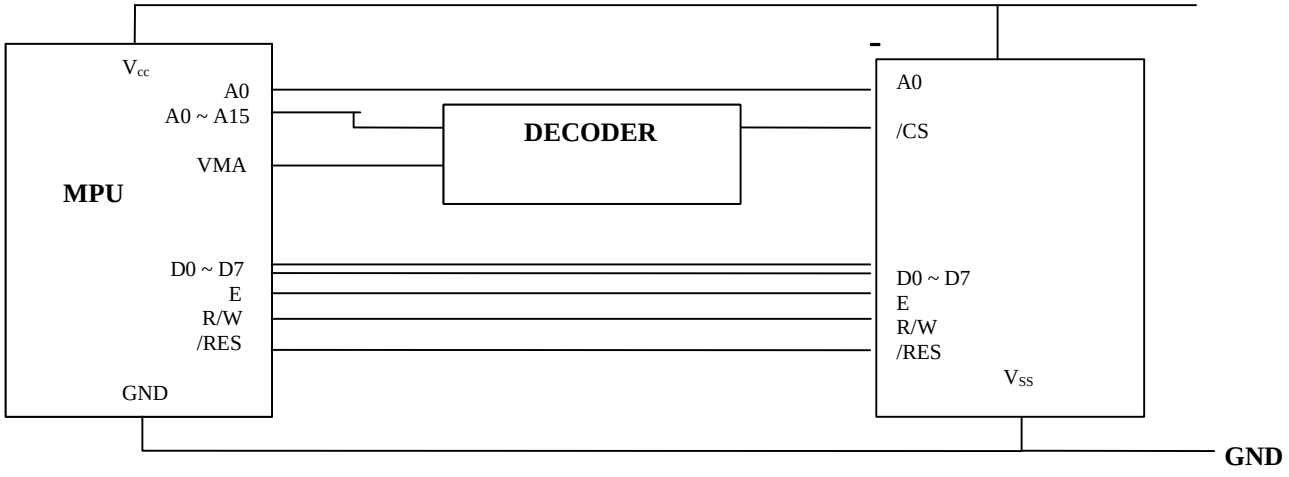
9.2 68-SERIES MPU



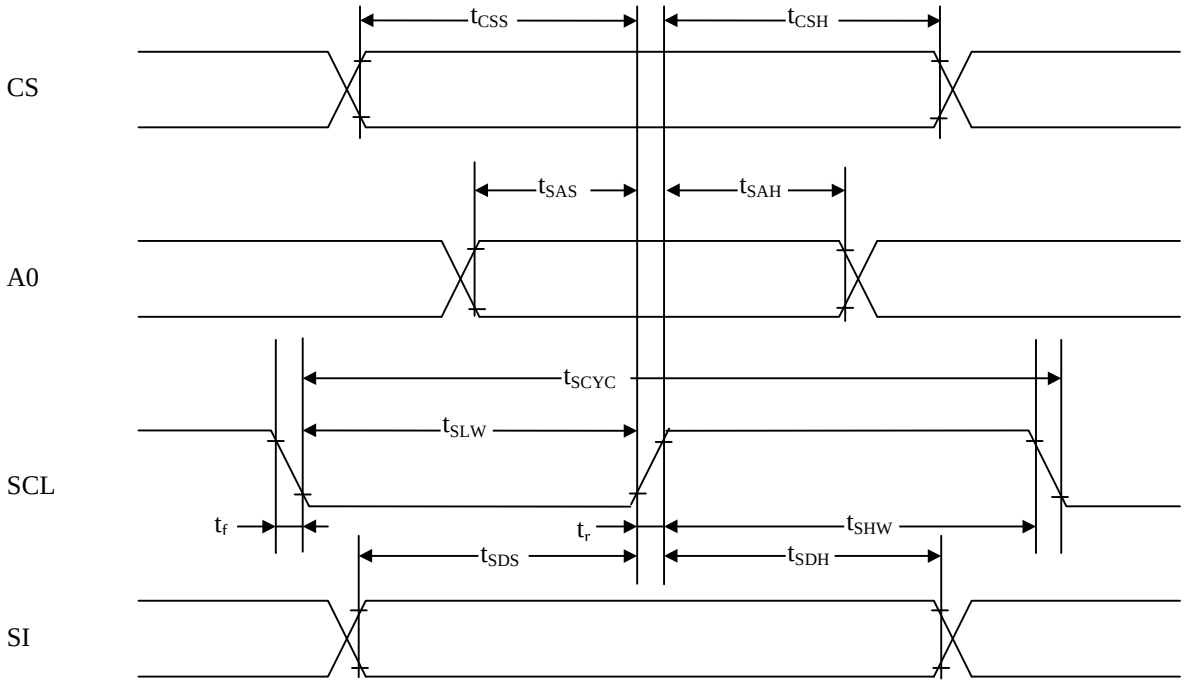
V_{DD} =5V±10%, Ta= 0 °C ~ +60 °C

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0, CS, R/W	tAH6		10	-	nS
Address setup time			tAW6		10	-	
System cycle time			tCYC6		200	-	
Data setup time		D0 to D7	tDS6		60	-	
Data hold time			tDH6		20	-	
Access time			tACC6	CL=100pF	-	70	
Output disable time			tOH6		0	25	
Enable H pulse width	READ	E	tEWHR		100	-	
	WRITE		tEWHW		25	-	
Enable L pulse width	READ	E	tEWLR		-	-	
	WRITE		tEWLW		-	-	
Input signal change time		A0,CS,R/W, E,D0 ~ D7	Tr, tf		-	15	

Notes: 1. t_r and tf of input signal should be< 15nS
2. For timing purposes, LOW=20% Vdd, HIGH=80%Vdd.

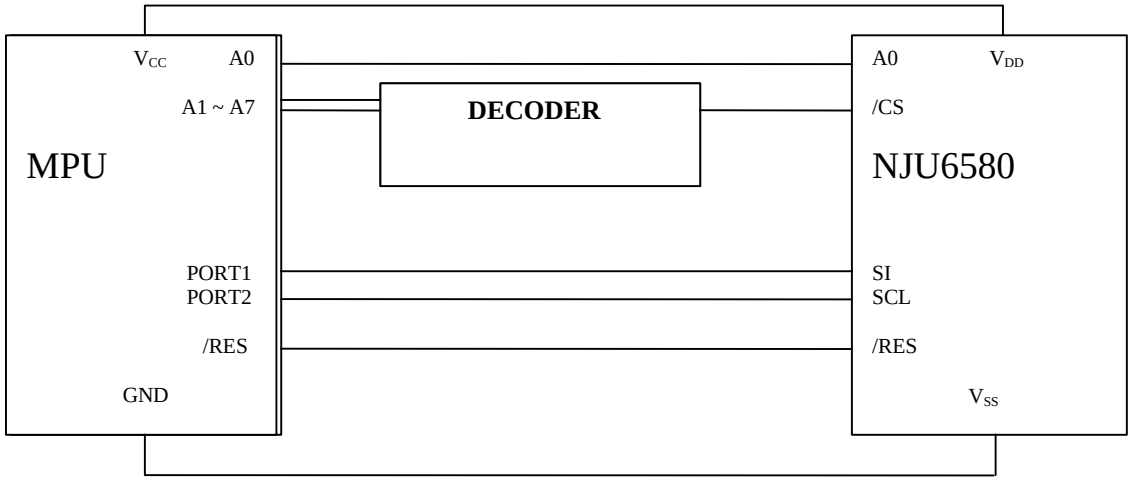


9.3 SERIAL INTERFACE



V_{DD} =5V±10%, Ta= 0 °C ~ +60 °C

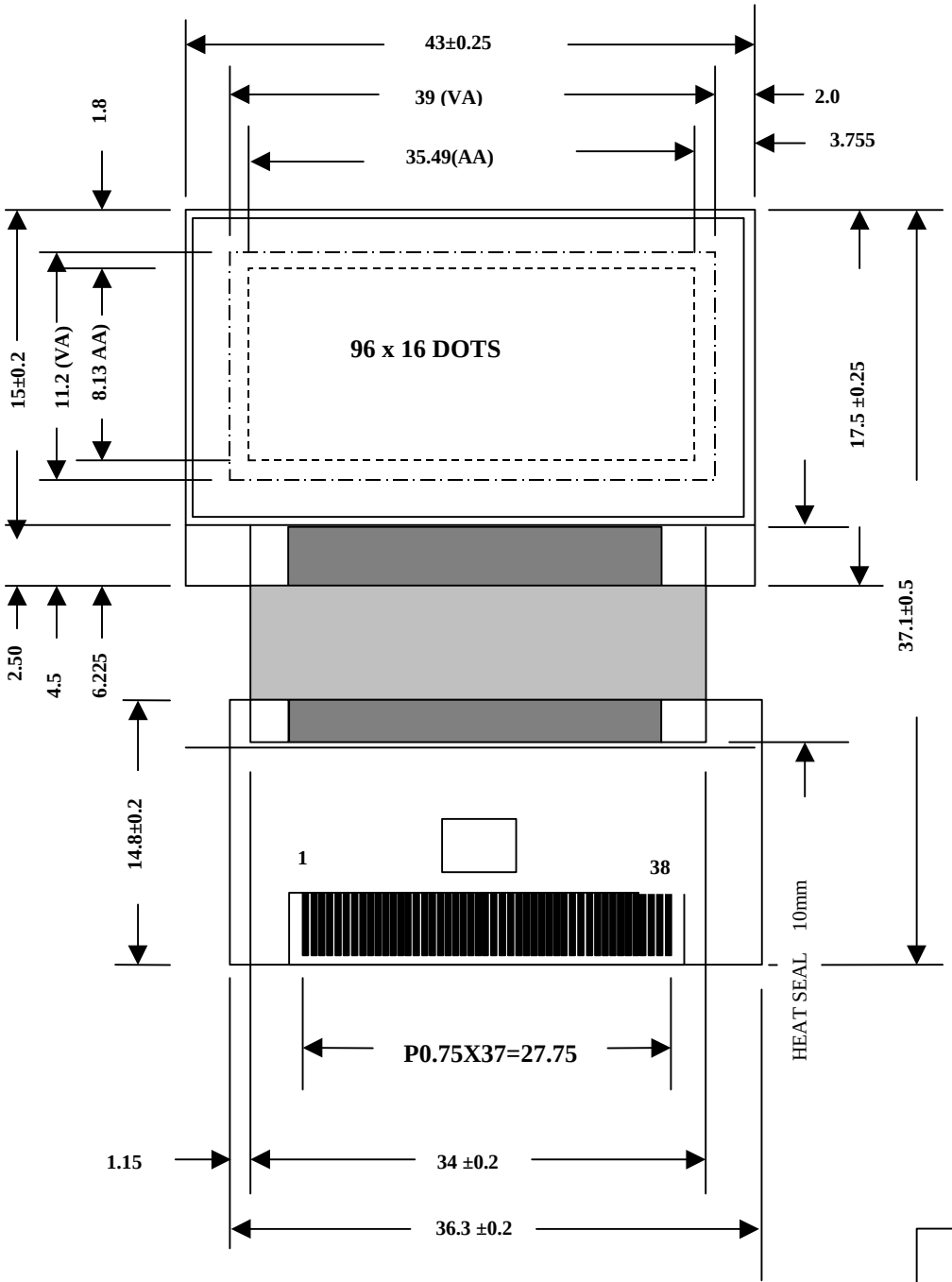
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		500		nS
SCL High pulse width		t_{SHW}		150		
SCL Low pulse width		t_{SLW}		150		
Address setup time	A0	t_{SAS}		120		
Address hold time		t_{SAH}		200		
Data setup time	SI	t_{SDS}		120		
Data hold time		t_{SDH}		50		
CS-SCL time	CS	t_{CSS}		30		
		t_{CSH}		400		
Input signal change time		t_r, t_f			15	

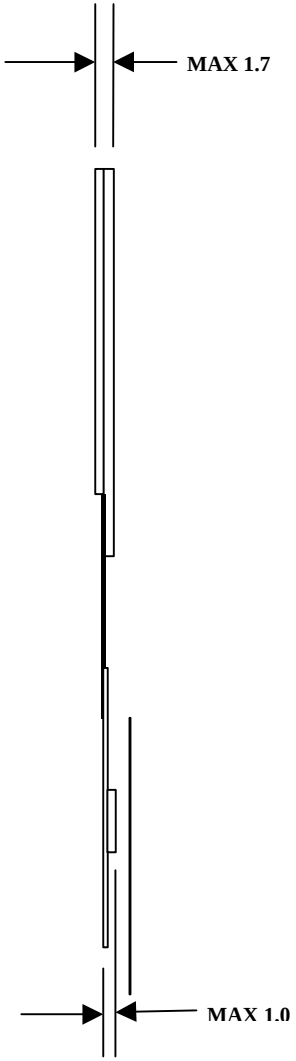


10.0 DISPLAY COMMAND SET

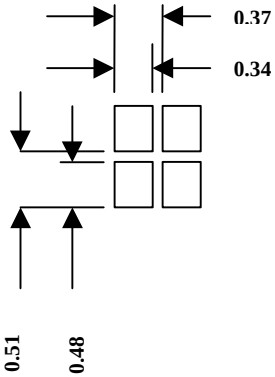
Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	Turns the LCD display ON and OFF 0: OFF 1: ON
Page address set	0	1	0	1	0	1	1	*	*	Page Add		Set the page of DD Ram to the page address register
Column address set: higher-order 4 bits	0	1	0	0	0	0	1	High-order column address				Load 4 higher-order bits of RAM column address into column address register
Column address set: lower- order 4 bits	0	1	0	0	0	0	0	Low-order column address				Load 4 lower-order bits of RAM column address into column address register
Status read	0	0	1	Status bits				0	0	0	0	Read LCD controller status
Display data write	1	1	0	Write data								Write data to display RAM location specified by column address and page address registers
Display data read	1	0	1	Read data								Reads data from display RAM
ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0: Normal 1: Inverse
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Set normal/inverted display mode 0: normal 1: reversed
Whole DisplayOn	0	1	0	1	0	1	0	0	1	0	0 1	Toggle between normal display operation and ALL SEGMENTS ON 0: Normal display 1: All ON
Icon Display	0	1	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0: No Icon 1: With Icon
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address Register when Writing but No-Change when Reading
End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Command
Reset	0	1	0	1	1	1	0	0	0	1	0	Initialise the Internal Circuits
Com Output/ Scroll Set Up	0	1	0	1	1	0	0	A3	M	S1	S0	Set the COM (A3) and Scroll (M, S0, S1)
Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0 1	Internal Power Supply Off Internal Power Supply On
LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the Internal (External) Power Supply is Turned On
EVR Register Set	0	1	0	1	0	0	0	Set Data				Set the V5 output level to The EVR Register
Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power Save Mode
Scroll Page Set	0	1	0	0	1	*	*	*	*	P1	P0	Set the Scroll Page P=0 : Used Scroll P=1 : No Scroll
Scroll On/Off Set	0	1	0	1	0	1	0	1	0	0	0	Scroll On/Off 0: Off 1: On
Data Request Reset	0	1	0	0	0	1	0	0	0	0	0	Reset the Data Request Signal

(* : Don't Care)





DOT DETAIL



DWG. NO. LM3907	SHEET 9 of 10	REV.

12.0 ENVIRONMENTAL

13.0 PART NUMBER DESCRIPTION FOR AVAILABLE OPTIONS

LM3097①②96G16③④⑤/X

①

Polariser type
B = Transflective positive (light background, with backlight)

②

LED Backlight Colour
N/A Leave Blank

③

Fluid type and Power Supply
S = Standard temperature range (0 to +50 ºC)

④

Fluid Type And Temperature Compensation
C = On-board temperature compensation

⑤

Background Colour
F = FSTN (Black/White)

X

Operating Voltage
Blank = 5VDC operation