SHARP

SPEC No.	CC10Y006
ISSUE:	Nov. 19 1998

To ;

PRELIMINARY

SPECIFICATIONS

Product Type 1/2.7-type(6.72mm) Interline Color CCD Area Sensor with 1310k Pixels

Model No. LZ23J3G

※This specifications contains 30 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: K. Misawa
K. MISAWA
Dept. General Manager

REVIEWED BY: N. Fukuba

PREPARED BY: T. Ohshima

Image Device Engineering Dept. 1
System LSI Development Center
Integrated Circuits Development Group
SHARP CORPORATION

- Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.

- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
  - ·Office electronics
  - ·Instrumentation and measuring equipment
  - ·Machine tools
  - ·Audiovisual equipment
  - ·Home appliances
  - ·Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
  - ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  - ·Mainframe computers
  - ·Traffic control systems
  - ·Gas leak detectors and automatic cutoff devices
  - ·Rescue and security equipment
  - ·Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
  - ·Aerospace equipment
  - ·Communications equipment for trunk lines
  - ·Control equipment for the nuclear power industry
  - ·Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

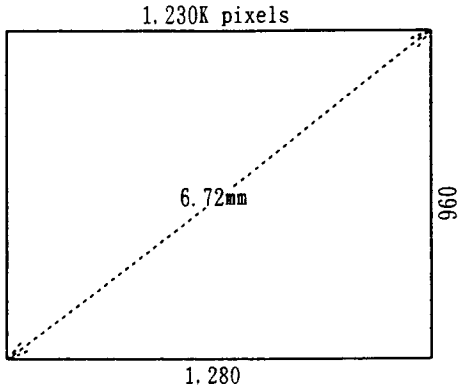
CONTENTS

1. GENERAL DESCRIPTION

LZ23J3 is a 1/2.7-type(6.72mm) solid-state image sensor consists of PN photo-diodes and CCDs(charge-coupled devices). Having approximately 1,310,000 pixels(horizontal 1344 x vertical 971), the sensor provides a high resolution stable color image.

Features

1) Optical size : 6.72mm (Aspect ratio 4:3)



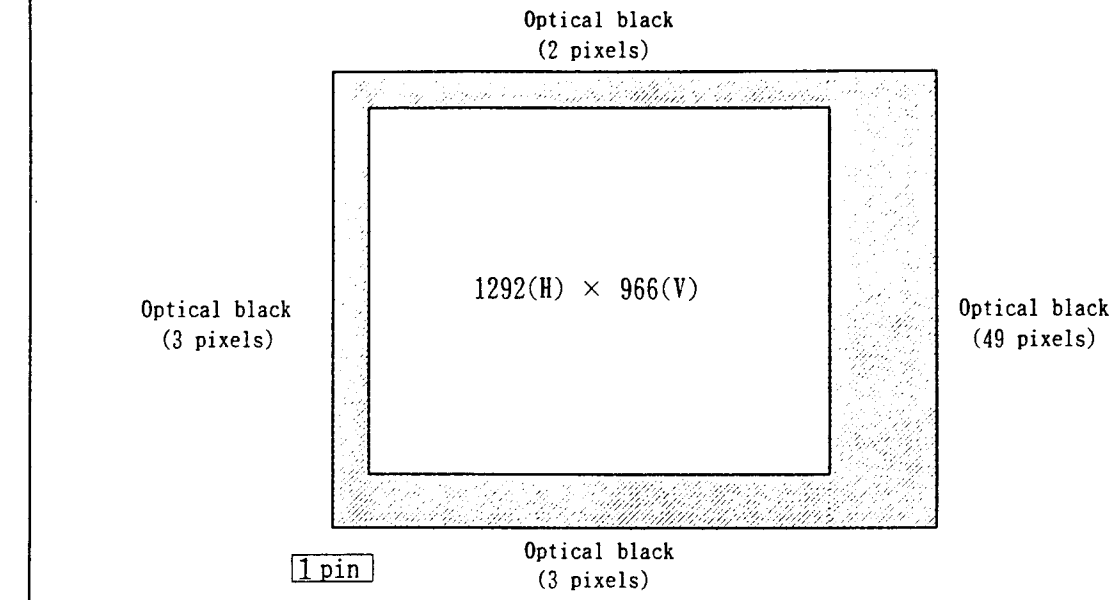
2) Interline scan format
3) Square pixel
4) Number of image pixels : Horizontal 1292 x vertical 966
   Pixel pitch : Horizontal 4.2 μm x vertical 4.2μm
   Number of optical black pixels : Horizontal ; front 3 and rear 49
   Vertical ; front 3 and rear 2
   Number of dummy bits : Horizontal ; 28, Vertical ; 2
5) Primary color mosaic filter composed of R, G, B
6) Supports monitering mode
7) Built-in overflow drain voltage output circuit, and built-in reset gate bias output circuit
8) Variable electronic shutter
9) Low fixed pattern noise and lag
10) No burn-in and no image lag
11) Blooming suppression structure
12) Built-in output amplifier
13) 16-pin shulink-pitch DIP, plastic pakage (Row space : 12.7mm)
14) N-type silicon substrate, N-MOS process,
    Not designed or rated as radiation hardened

Applications

1) Electronic still camaras, video capturing devices for PC, etc.
2) Pattern recognition

※ The circuit diagram and others included in this specification are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2. ARRANGEMENT OF PIXELS AND COLOR FILTERS



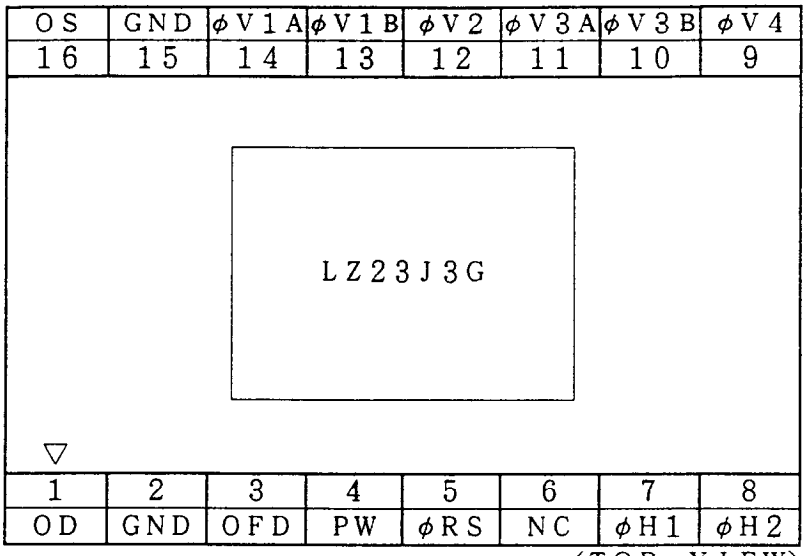
Pin arrangement of the vertical readout clock

(1, 966) (1292, 966)

φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1A	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3A	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1A	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3A	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1A	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G
φV3B	G	B	G	B	G	B	G	B		G	B	G	B	G	B	G	B
φV1B	R	G	R	G	R	G	R	G		R	G	R	G	R	G	R	G

(1, 1) (1292, 1)

3. PIN IDENTIFICATION



(TOP VIEW)

Symbol	Pin name
OD	Output transistor drain
OS	Video output
φRS	Reset transistor clock
φV1A, φV1B, φV2, φV3A, φV3B, φV4	Vertical shift resister clock
φH1, φH2	Horizontal shift resister clock
OFD	Overflow drain
PW	P well
GND	Ground
NC	Non connection

4. ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

Parameter	Symbol	Ratings	Unit
Output transistor drain voltage	VOD	0～+18	V
Overflow drain voltage	VOFD	internal output(note1)	
Reset gate clock voltage	VφRS	internal output(note2)	
Vertical shift register clock voltage	VφV	VPW～+18	V
Horizontal shift register clock voltage	VφH	-0.3～+12	V
Voltage difference between Pwell and vertical clock	VPW-VφV	-29～ 0	V
Voltage difference between vertical clock	VφW-VφV	0～+15(note3)	V
Storage temparature	Tstg	-40～+80	℃
Operating ambient temparature	Topr	-20～+70	℃

(note1) Do not connect to DC voltage directly. When OFD is connected to GND, connect VOD to GND. Overflow drain clock is applied below 33Vp-p.

(note2) Do not connect to DC voltage directly. When φRS is connected to GND, connect VOD to GND. Reset gate clock is applied below 8Vp-p.

(note3) When clock width is below 10μs, and clock duty factor is below 0.1%, voltage difference between vertical clock is guaranteed to 28V.

5. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating ambient temperature	Topr		25.0		℃
Output transistor drain voltage	VOD	15.0	15.5	16.0	V
Overflow drain clock p-p level (note1)	$V\phi_{OFD}$	28.0	30.0	32.0	V
Ground	GND		0.0		V
P well voltage (note2)	VPW	-9.0		VφVL	V
Vertical shift register clock LOW level	VφV1AL, VφV1BL, VφV2L VφV3AL, VφV3BL, VφV4L	-8.5	-8.0	-7.5	V
Vertical shift register clock INTERMEDIATE level	VφV1AI, VφV1BI, VφV2I VφV3AI, VφV3BI, VφV4I		0.0		V
Vertical shift register clock HIGH level	VφV1AH, VφV1BH VφV3AH, VφV3BH	15.0	15.5	16.0	V
Horizontal shift register clock LOW level	VφH1L, VφH2L	-0.05	0.0	0.05	V
Horizontal shift register clock HIGH level	VφH1H, VφH2H	3.6	3.9	4.2	V
Reset gate clock p-p level (note3)	VφRS	3.6	3.9	4.2	V
Vertical shift register clock frequency	fφV1A, fφV1B, fφV2 fφV3A, fφV3B, fφV4		7.87		kHz
Horizontal shift register clock frequency	fφH1, fφH2		12.27		MHz
Reset gate clock frequency	fφRS		12.27		MHz

(note1) Use the circuit parameter indicated in "8. STANDARD OPERATING CIRCUIT EXAMPLE" (p.21), and do not connect to DC voltage directly.

(note2) VPW is set below VφVL that is low level of vertical shift register clock, or use the same power supply that is connected to VL of V driver IC.

(note3) Use the circuit parameter indicated in "8. STANDARD OPERATING CIRCUIT EXAMPLE" (p.21), and do not connect to DC voltage directly.

♦ To apply power, first connect GND and then turn on OD. After turning on OD, turn on PW first and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

6. CHARACTERISTICS (Drive method : 1/30sec. frame accumulation)

Ambient temperature : +25℃, but +60℃ for parameter No. 4 and 5.
Operating conditions : the typical values specified in recommended conditions.
Color Temperature of light source : 3200K / IR cut-off filter(CM-500, 1mmt) is used.

No.	Parameter		Symbol	Note	Minimum	Typical	Maximum	Unit
1	Standard output voltage		Vo	(a)		150		mV
2	Photo response non-uniformity		PRNU	(b)			10	%
3	Saturation output voltage		Vsat	(c)(d)	470	550		mV
				(c)(e)	340	420		mV
4	Dark output voltage		Vdark	(f)		0.5	3.0	mV
5	Dark signal non-uniformity		DSNU	(g)		0.5	2.0	mV
6	Sensitivity		R	(h)	150	200	250	mV
7	Sensitivity ratio	R/G	Rr	(i)	0.30	0.45	0.60	
		B/G	Rb		0.27	0.42	0.57	
8	Smear ratio		SMR	(j)		-75	-65	dB
9	Image lag		AI	(k)			1.0	%
10	Blooming suppression ratio		ABL	(l)	500			
11	Current dissipation		IOD			4.0	8.0	mA

【Note】

(a) The average output voltage of G signal under the uniform illumination. The standard exposure condition is defined when Vo is 150 mV.

(b) The image area is divided into 10 x 10 segments under the standard exposure condition. The voltage of a segment is the average output voltage of all pixels within the segment. PRNU is defined by (Vmax - Vmin) / Vo, where Vmax and Vmin are the maximum and minimum values of each segment's voltage respectively.

(c) The image area is divided into 10 x 10 segments. The segment's voltage is the average output voltages of all pixels within the segment. Vsat is the minimum segment's voltage under 10 times exposure of the standard exposure condition.

(d) The operation of OFDC is high. (for still image capturing)

(e) The operation of OFDC is low.

(f) The average output voltage under the non-exposure condition.

(g) The image area is divided into 10 x 10 segments under the non-exposure condition. DSNU is defined by (Vdmax - Vdmin), where Vdmax and Vdmin are the maximum and minimum values of each segment's voltage respectively.

(h) The average output voltage of G signal when a 1000 lux light source with a 90% reflector is imaged by a lens of F4, f50 mm.

(i) Rr and Rb are defined by V_R/V_G and V_B/V_G respectively, where V_R, V_G and V_B are the each average output voltages of R, G and B signals respectively.

(j) The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the output voltage in the V/10 square.

(k) The sensor is exposed at the exposure level corresponding to the standard condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.

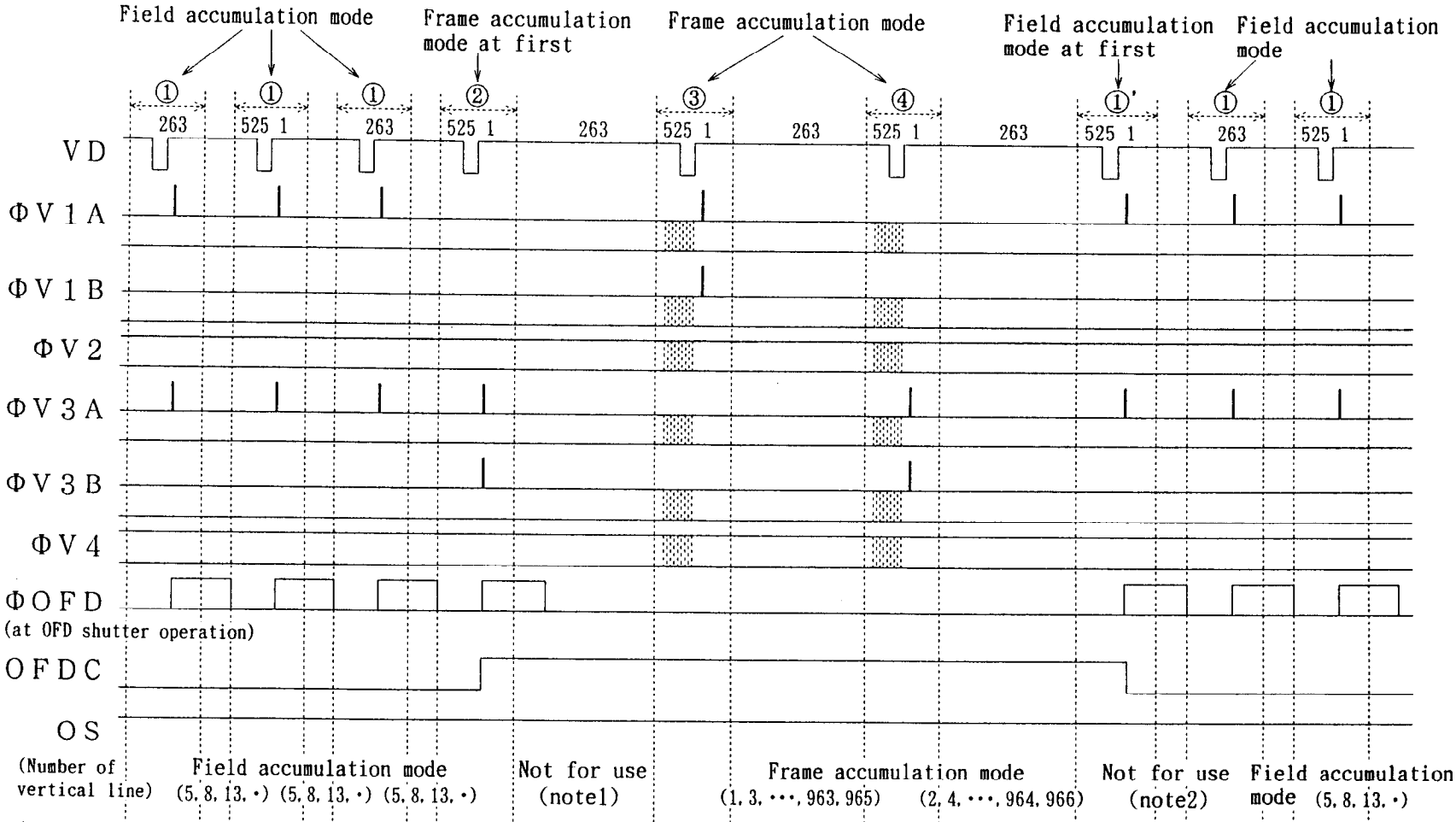
(l) The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.

♦ Within the recommended operating condition of VOD, VOFD of the internal output satisfy with ABL larger than 500 times exposure of the standard exposure condition, and Vsat larger than 340mV.

7. TIMING DIAGRAM EXAMPLE

TIMING DIAGRAM EXAMPLE

·····→ Pulse diagram in more detail is shown in the figure ①~④ after next page.

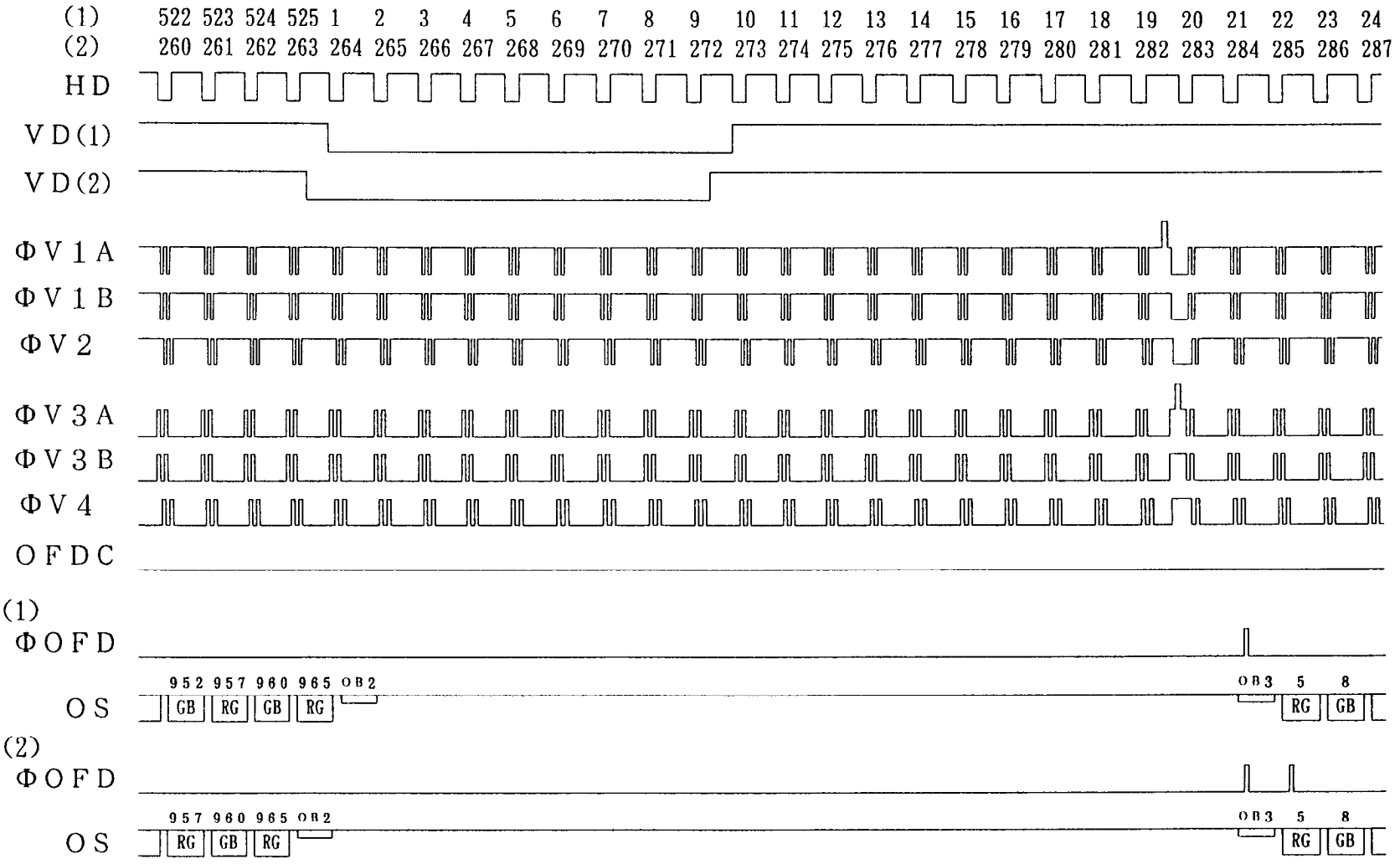


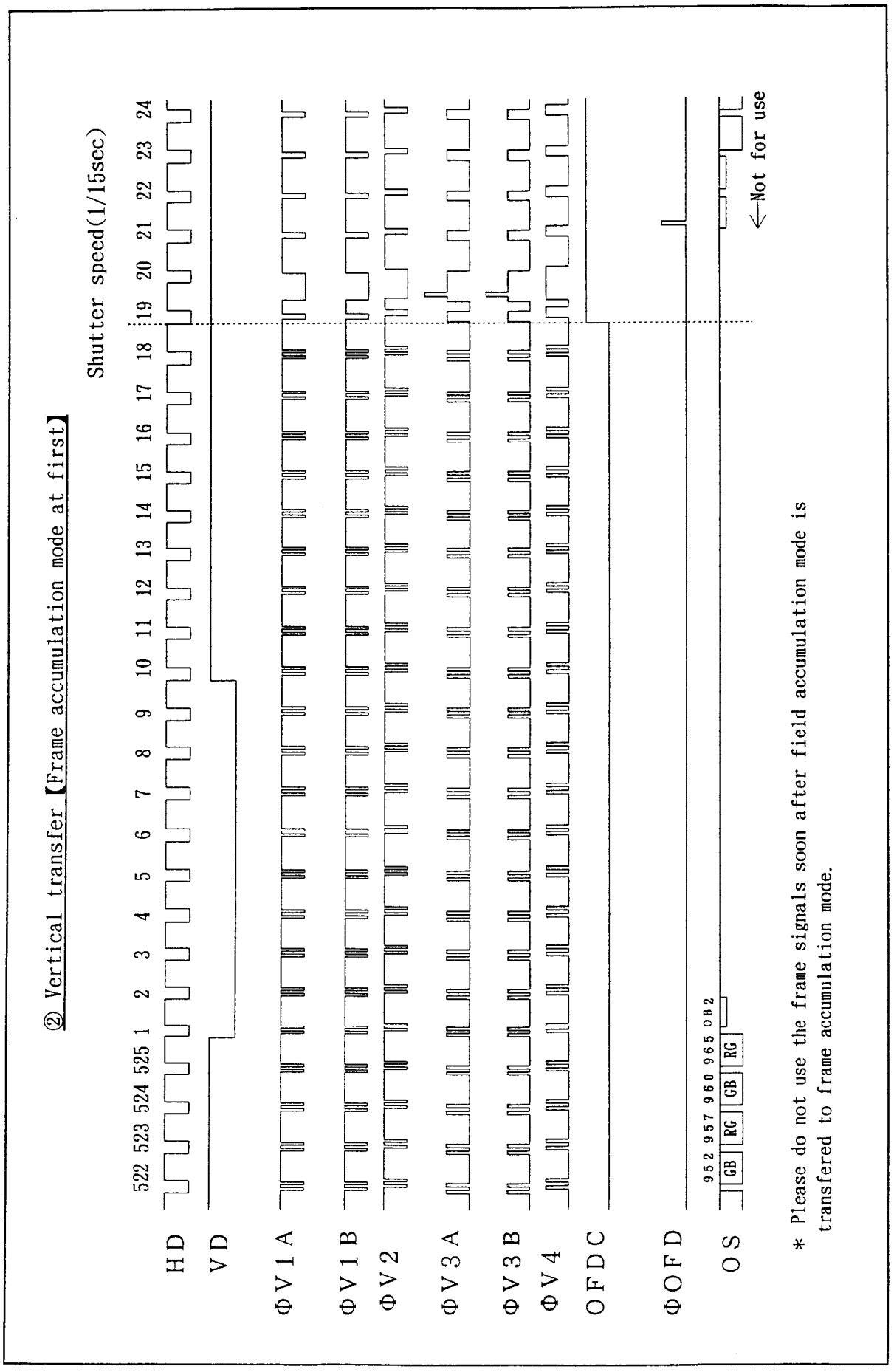
(note1) Please do not use these signals soon after field accumulation mode is transfered to frame accumulation mode for still image capturing.
(note2) Please do not use these signals soon after frame accumulation mode is transfered to field accumulation mode for monitoring image.

* Please start the exposure period after 10ms later that OFDC is high, and finish before charge swept transfer.
* Please apply at least a OFD shutter pulse to OFD in each field accumulation mode.

① Vertical transfer【Field accumulation mode】

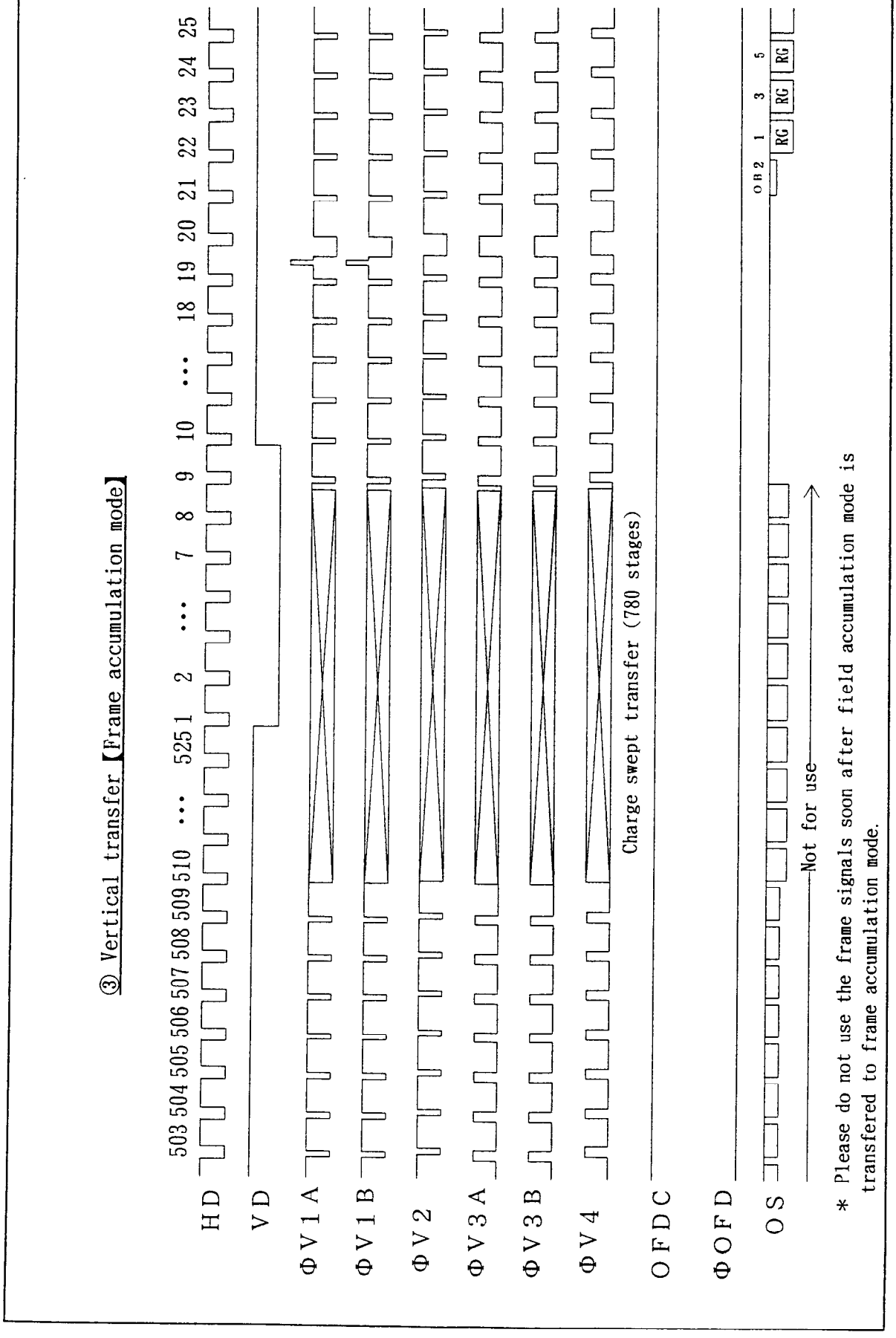
Shutter speed(1/30sec)



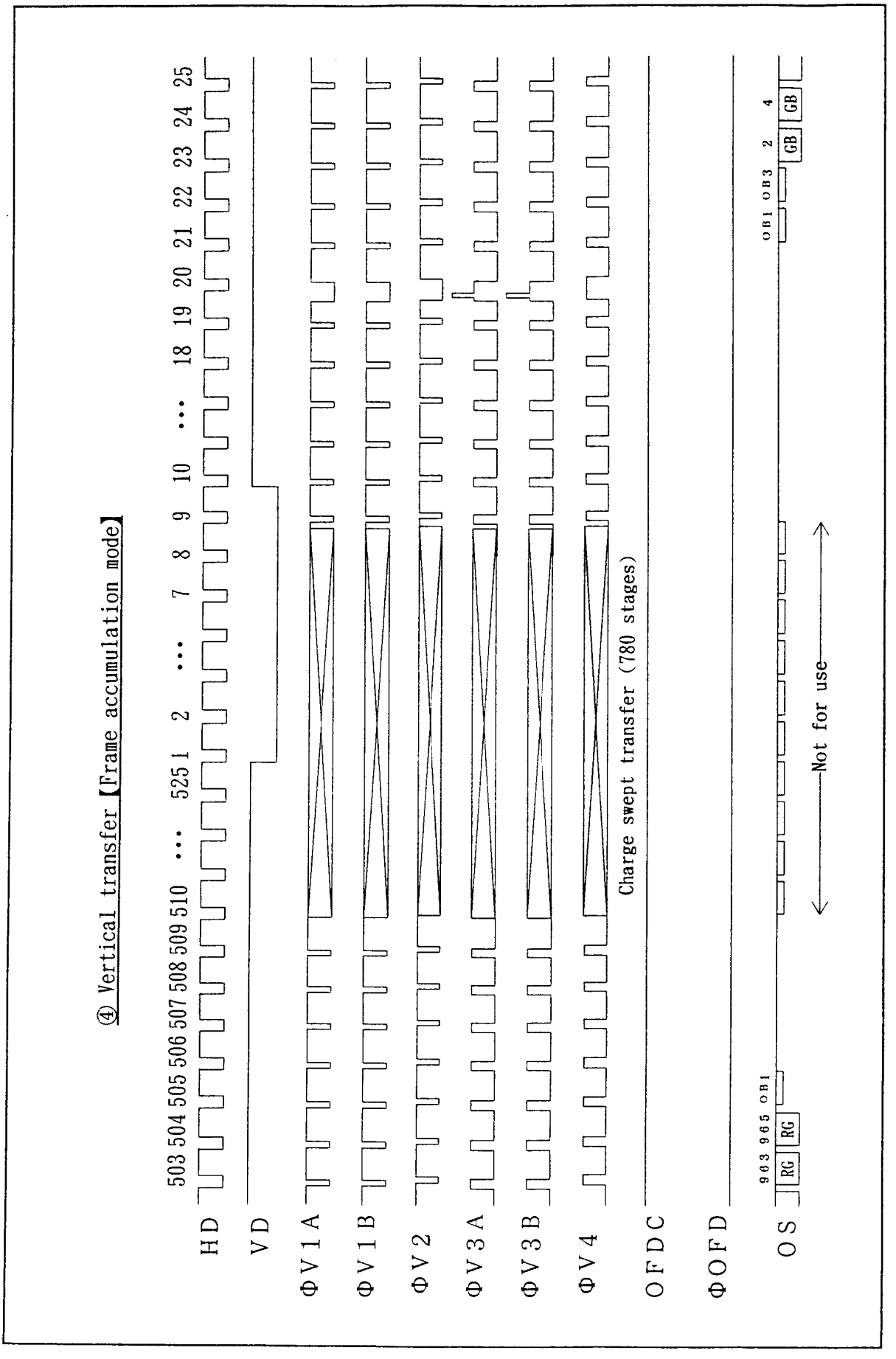


* Please do not use the frame signals soon after field accumulation mode is transfered to frame accumulation mode.

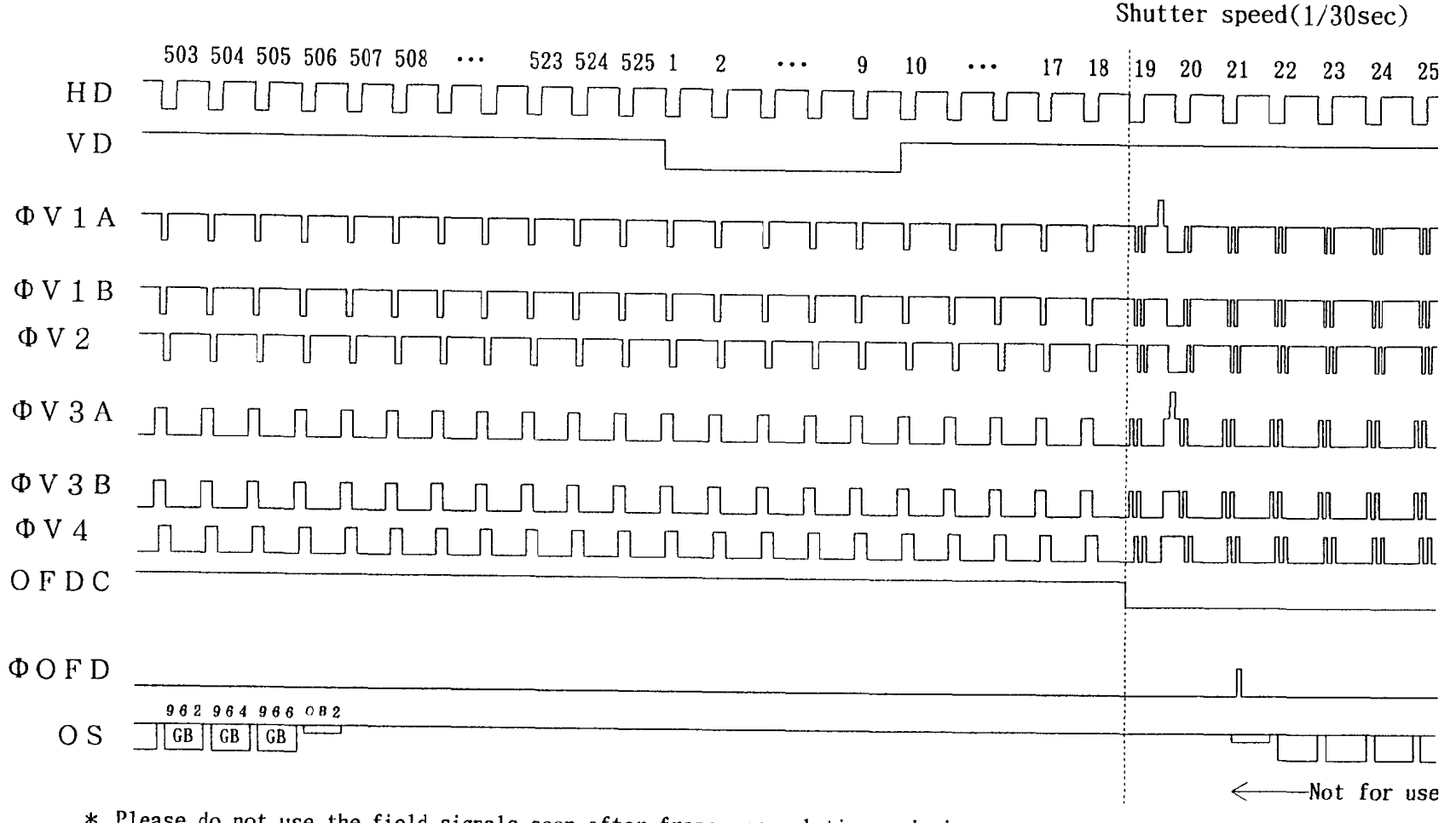
③ Vertical transfer [Frame accumulation mode]



* Please do not use the frame signals soon after field accumulation mode is transfered to frame accumulation mode.

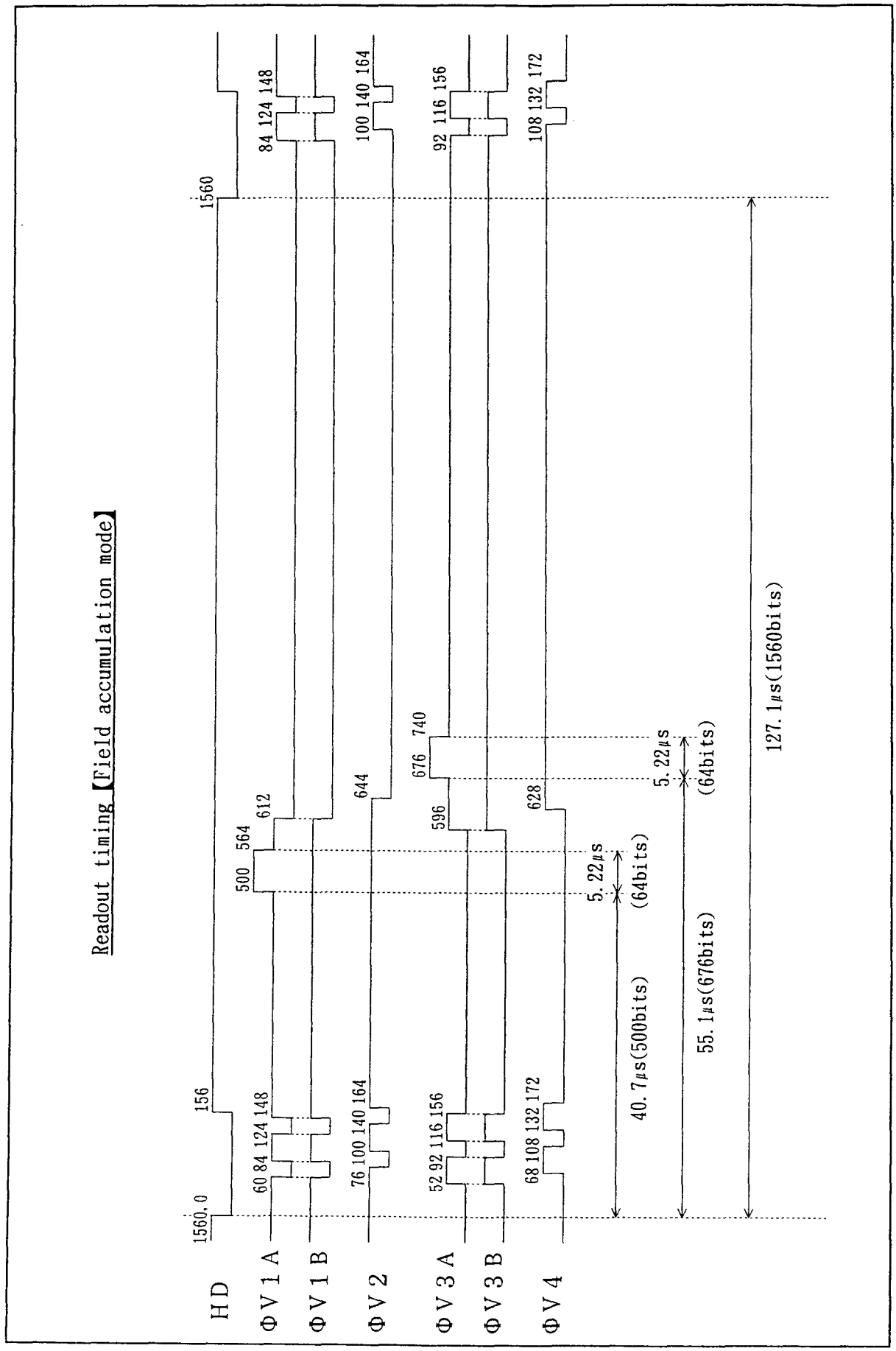

④ Vertical transfer【Frame accumulation mode】
503 504 505 506 507 508 509 510 ••• 525 1 2 ••• 7 8 9 10 ••• 18 19 20 21 22 23 24 25
HD
VD
ΦV1A
ΦV1B
ΦV2
ΦV3A
ΦV3B
ΦV4
OFDC
ΦOFD
OS
963 965 OB1
RG
RG
OB1 OB3 2 4
GB
GB
Charge swept transfer (780 stages)
Not for use

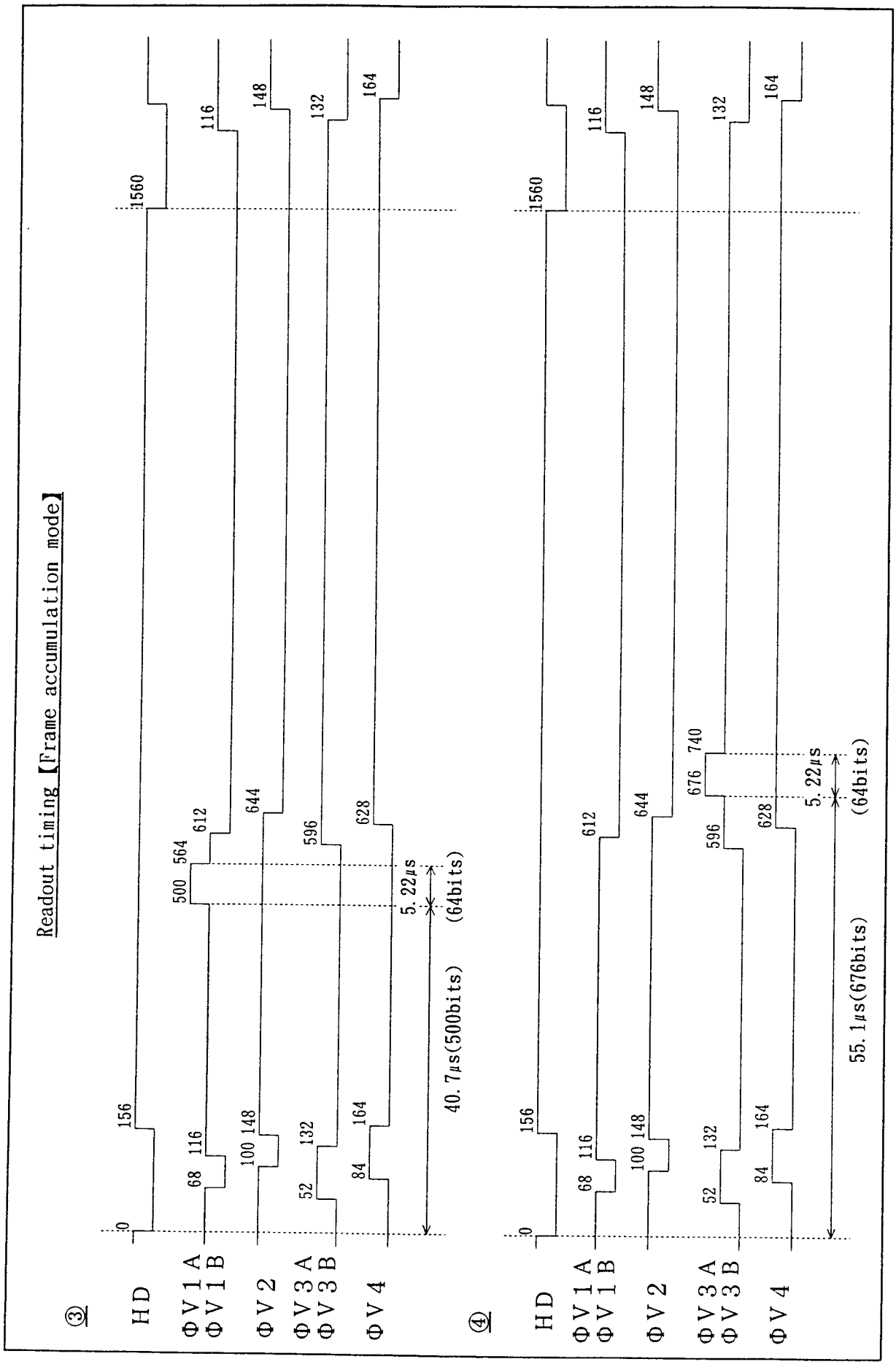
①' Vertical transfer【Field accumulation mode at first】



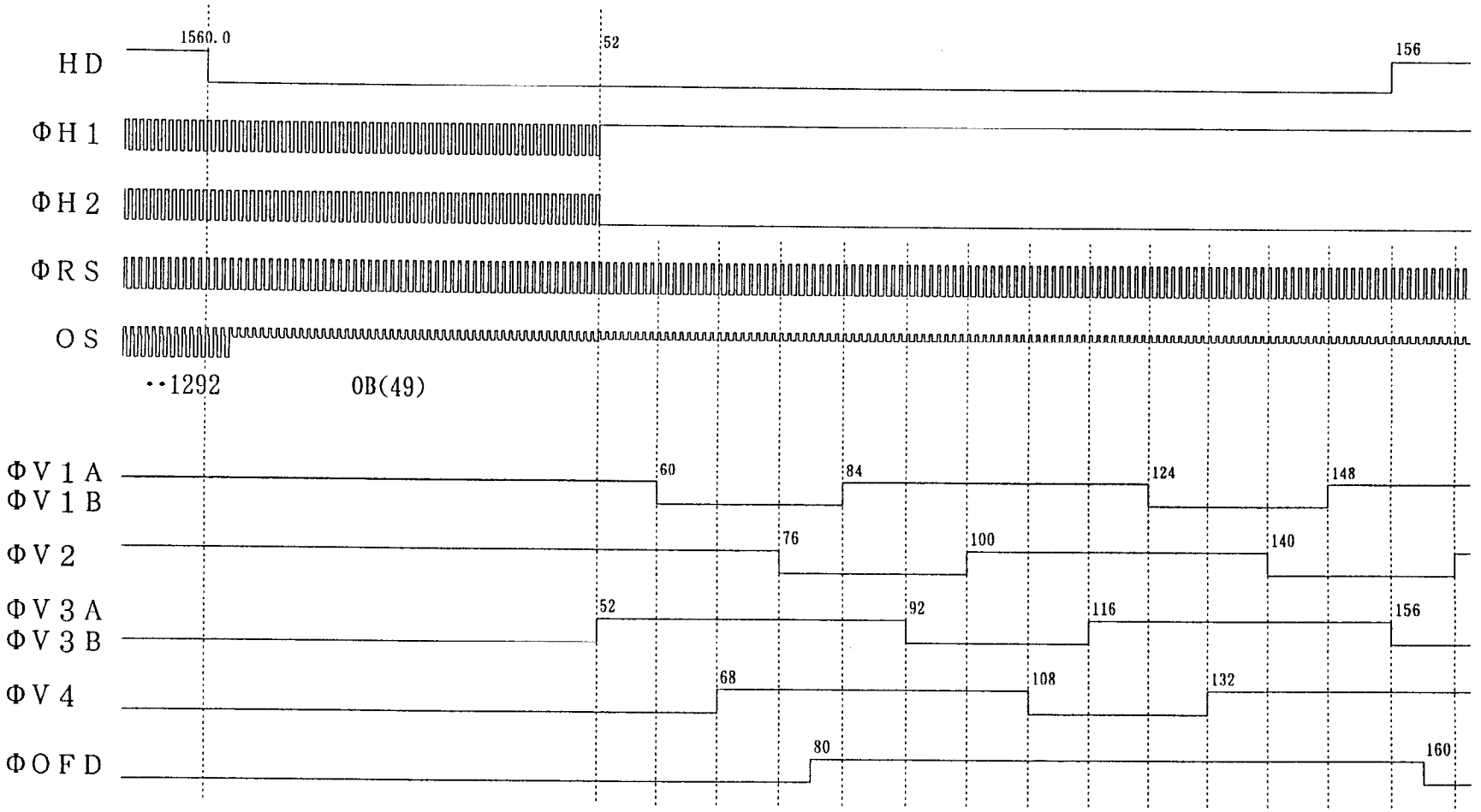
* Please do not use the field signals soon after frame accumulation mode is transfered to field accumulation mode.

Readout timing (Field accumulation mode)

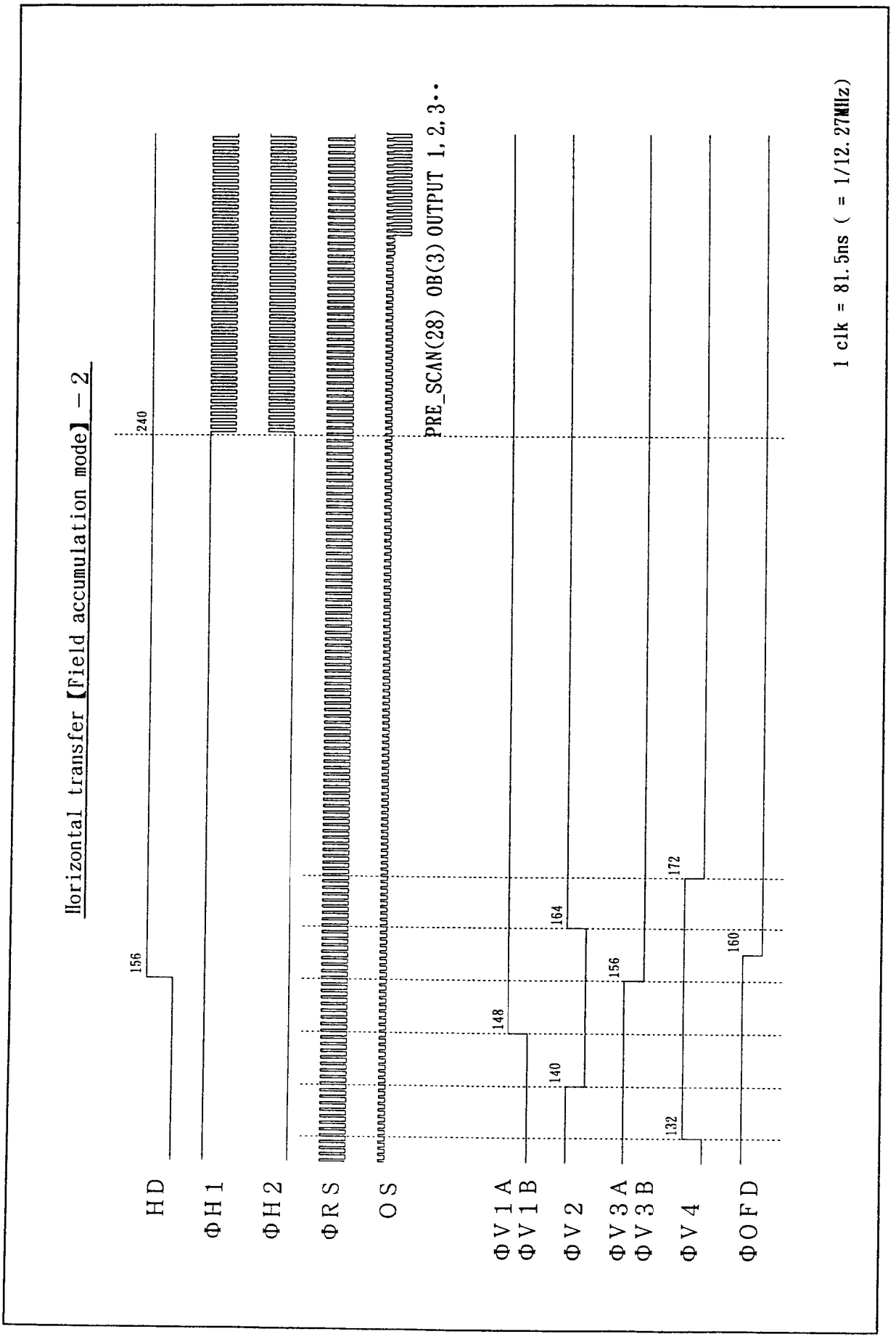


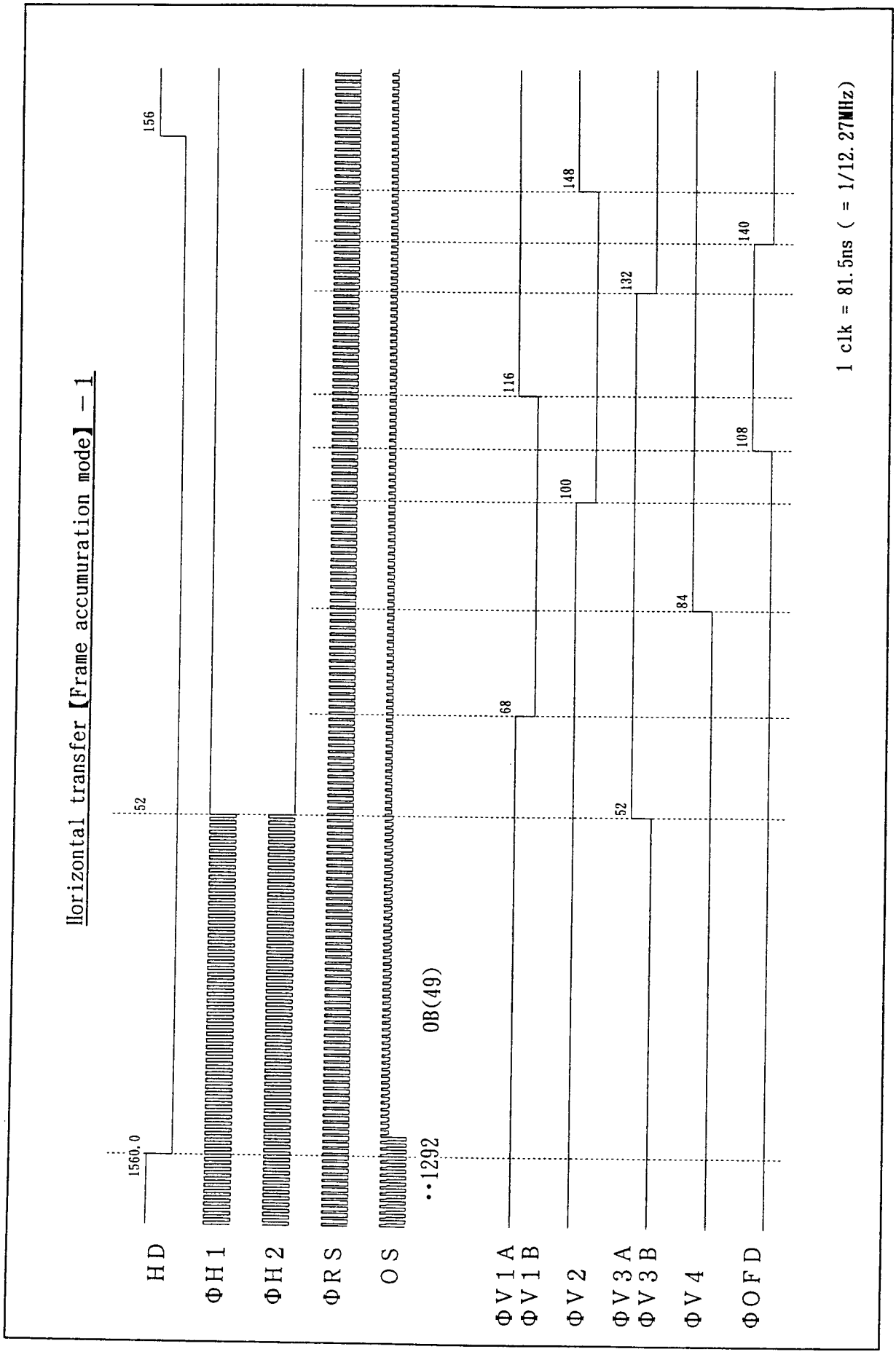

Readout timing【Frame accumulation mode】
③
HD
ΦV1A
ΦV1B
ΦV2
ΦV3A
ΦV3B
ΦV4
0
156
68
116
100
148
52
132
84
164
1560
500
564
612
644
596
628
116
148
132
164
5.22μs
40.7μs(500bits)
(64bits)
④
HD
ΦV1A
ΦV1B
ΦV2
ΦV3A
ΦV3B
ΦV4
0
156
68
116
100
148
52
132
84
164
1560
612
644
596
628
676
740
116
148
132
164
5.22μs
55.1μs(676bits)
(64bits)

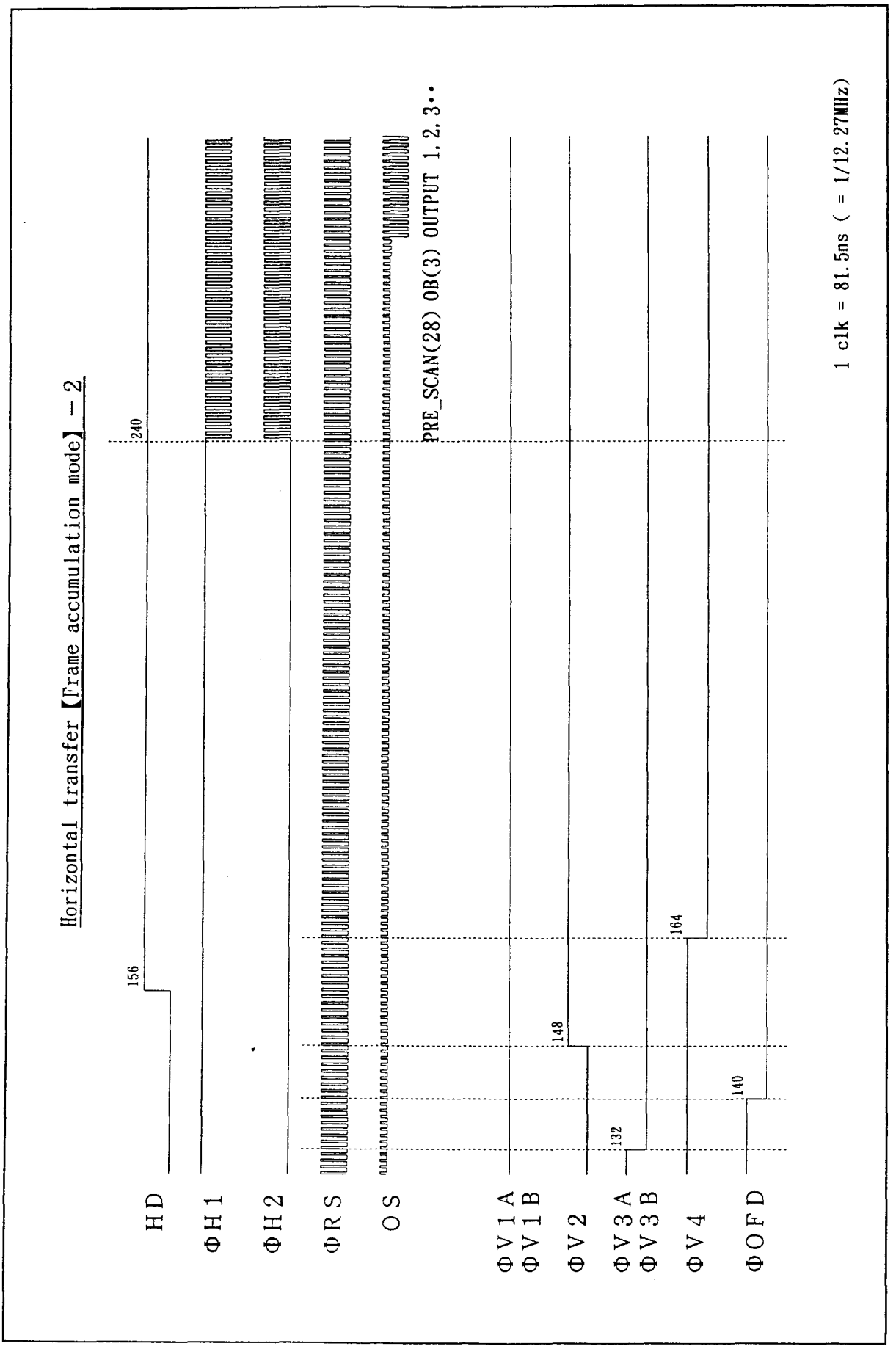
Horizontal transfer【Field accumulation mode】－1



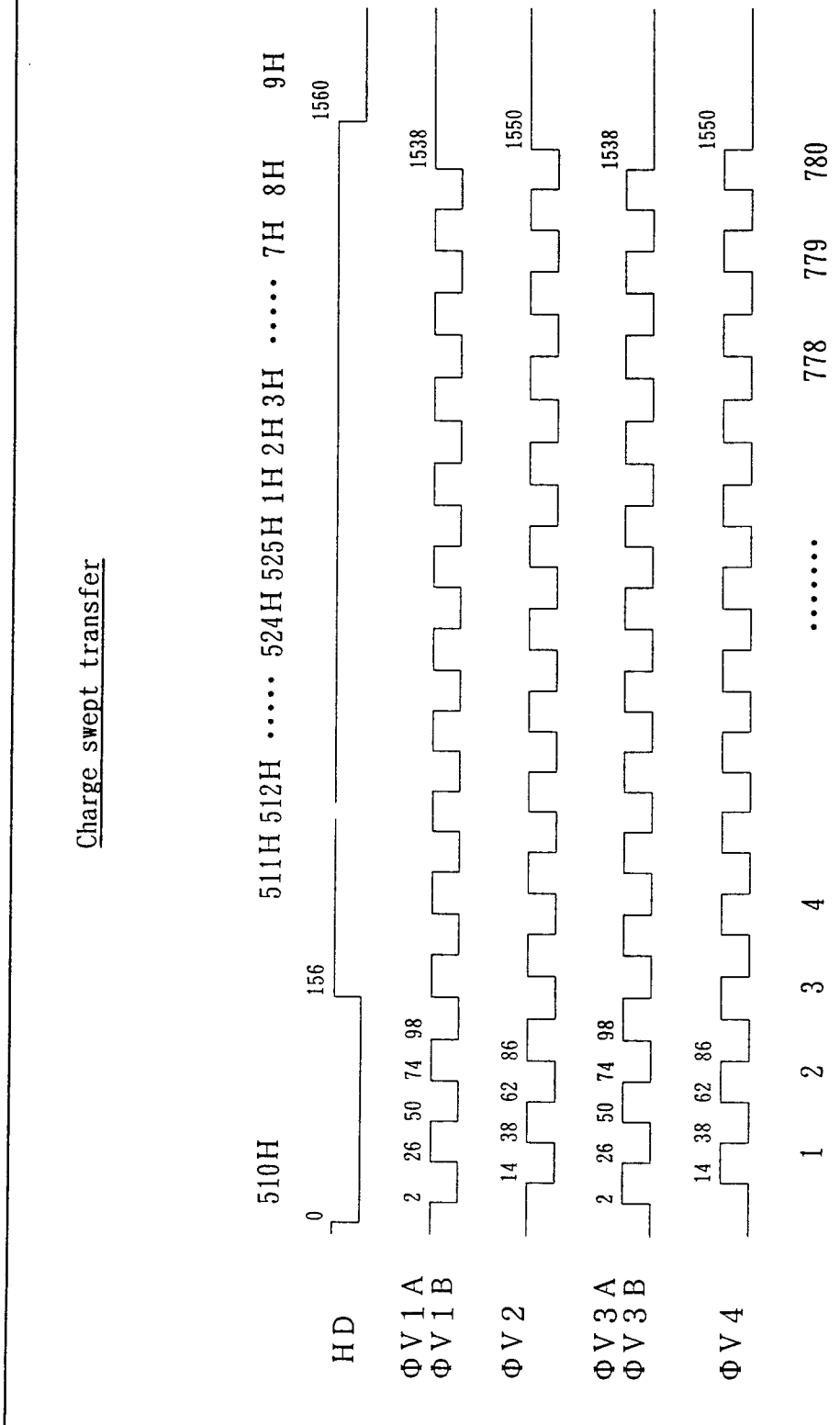
1 clk = 81.5ns (= 1/12.27MHz)


Horizontal transfer [Field accumulation mode] – 2
HD
ΦH1
ΦH2
ΦRS
OS
ΦV1A
ΦV1B
ΦV2
ΦV3A
ΦV3B
ΦV4
ΦOFD
156
240
148
140
164
156
172
132
160
PRE_SCAN(28) OB(3) OUTPUT 1, 2, 3··
1 clk = 81.5ns (= 1/12.27MHz)

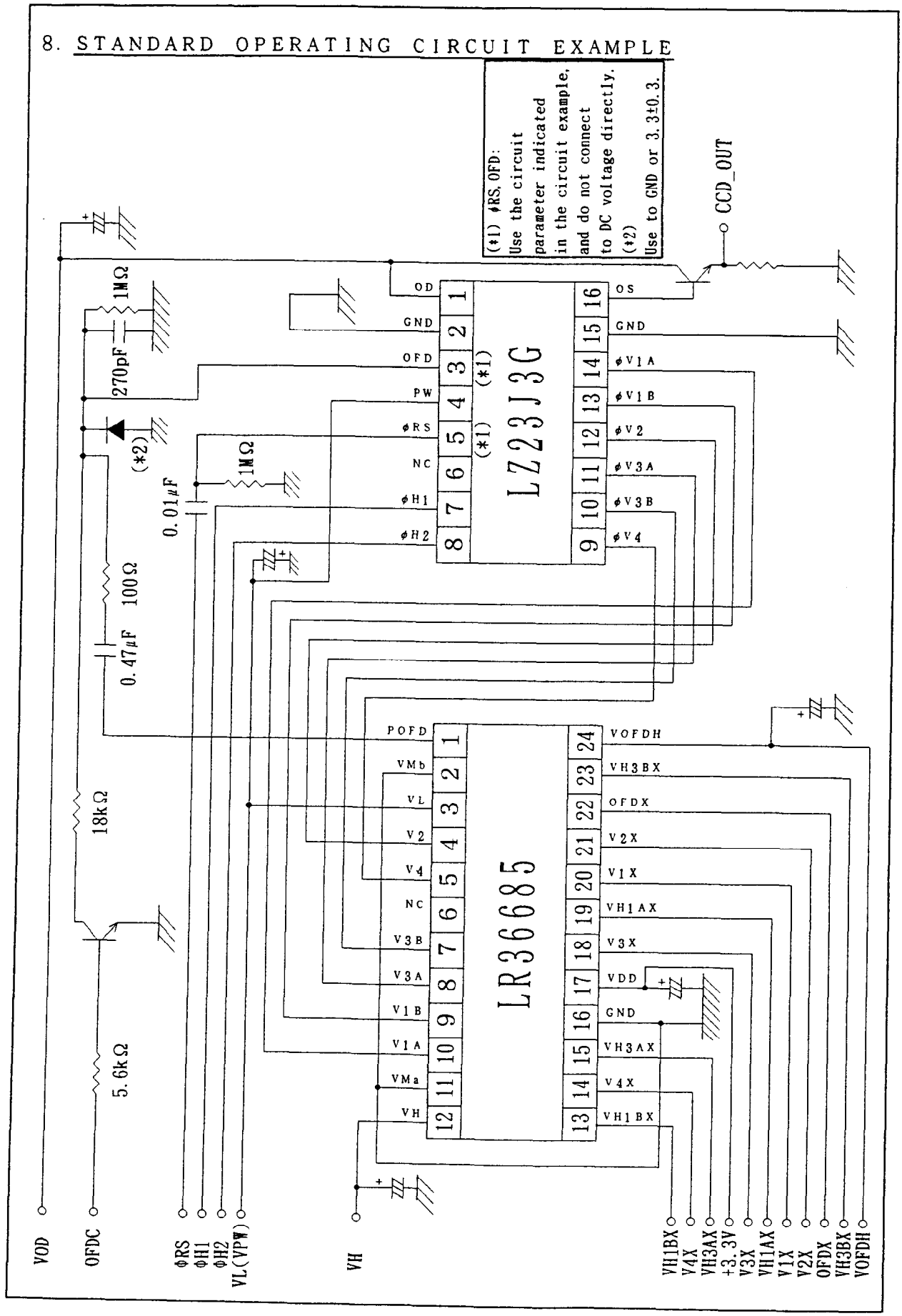

Horizontal transfer【Frame accumuration mode】－1
HD
ΦH1
ΦH2
ΦRS
OS
ΦV1A
ΦV1B
ΦV2
ΦV3A
ΦV3B
ΦV4
ΦOFD
1560.0
52
156
••1292
OB(49)
68
116
100
148
52
132
84
108
140
1 clk = 81.5ns (= 1/12.27MHz)


Horizontal transfer【Frame accumulation mode】－2
HD
ΦH1
ΦH2
ΦRS
OS
ΦV1A
ΦV1B
ΦV2
ΦV3A
ΦV3B
ΦV4
ΦOFD
156
240
148
132
164
140
PRE_SCAN(28) OB(3) OUTPUT 1, 2, 3・・
1 clk = 81.5ns (= 1/12.27MHz)

Charge swept transfer



8. STANDARD OPERATING CIRCUIT EXAMPLE



9. SPECIFICATION FOR BLEMISH (1/30sec. frame accumulation)

1) Definition of blemish

	Level of blemish (mV)	Permitted number of blemish	Comment
White blemish (Exposed)	40 ≦ B	0	・See fig. 9-1(a)、fig. 9-2. ・Vout = Vstd ・M + N = 12 Up to 8 blemishes are allowed in AREA Ⅰ
	20 ≦ B < 40	M	
	B < 20	no count	
Black blemish (Exposed)	40 ≦ B	0	
	20 ≦ B < 40	N	
	B < 20	no count	
White blemish (Non_exposed)		AREA Ⅰ / AREA Ⅱ	・See fig. 9-1(b)、fig. 9-2. Sum of the blemishes in AREA Ⅰ and Ⅱ are allowed up to 12.
	16 < B	0	
	12 < B ≦ 16	3	
	6 < B ≦ 12	8 / 10	
	B ≦ 6	no count	
White blemish (Shutter mode)	5.0 ≦ B	0	・See fig. 9-1(a)、fig. 9-2. ・Vout = Vstd/10 ・The electronic shutter speed is set at 1/10000 s
	B < 5.0	no count	
Black blemish (Shutter mode)	5.0 ≦ B	0	
	B < 5.0	no count	

※ Sum of the black and white blemishes except shutter mode into 8 x 8 pixels are allowed up to 1.

《note》

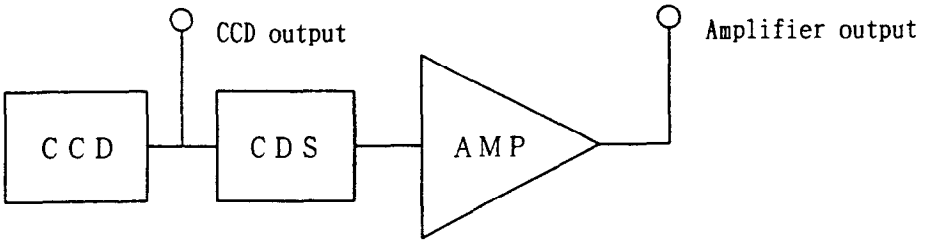
- B : Blemish level defined in fig. 9-1.
- Vout : Average output voltage
- Vstd : 150 mV. The standard output voltage defined in the specification of the characteristics.

2) Definition of stain.

The measuring area is devided into segments which include 20 x 20 pixels, respectively. The difference between the average output voltage of neighboring segments is permitted below 1.5 mV, under the condition that the average output voltage of all imaging pixels is 75 mV (= Vstd/2).

【MEASURING CONDITION】

- Ta : 60 ℃
- Measuring block diagram



The output voltage is measured at the CCD output.
The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

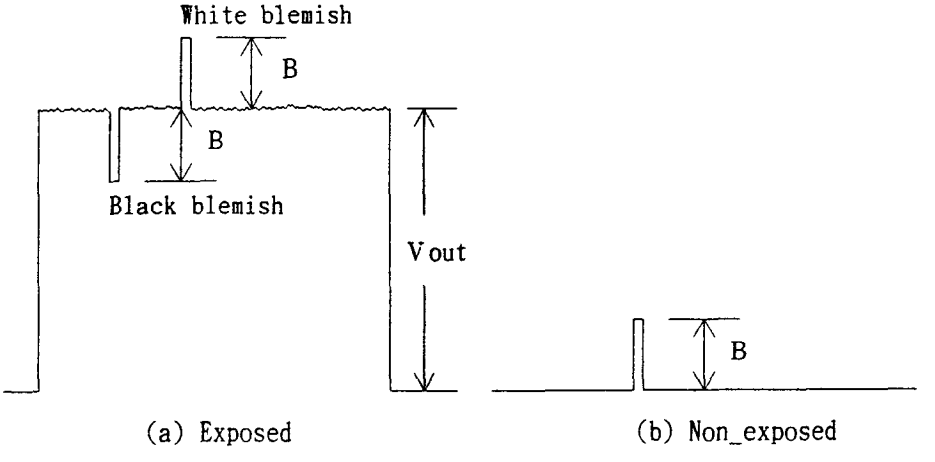


fig. 9-1 Definition of blemish level
(The wave form is the luminance signal measured at the Amplifier output.)

【MEASURING AREA】

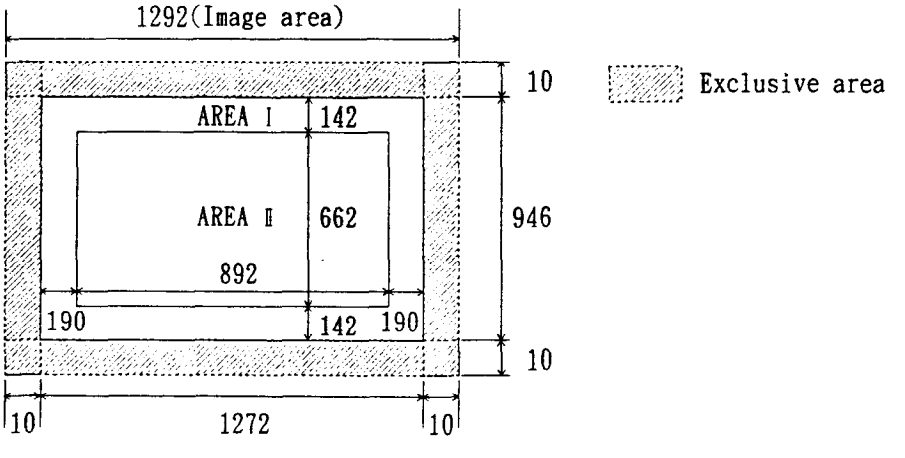


fig. 9-2 Definition of the measuring area

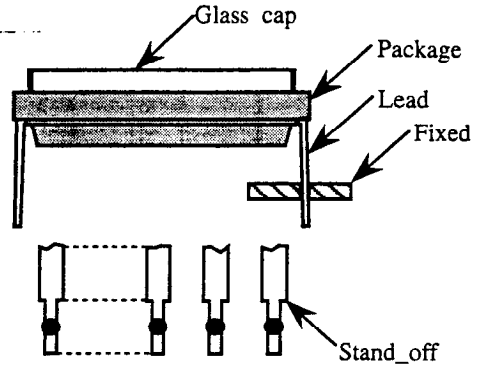
10. CAUTIONS FOR USE

1. Package breakage

In order to prevent the package from being broken, observe the following instructions:

1) The CCD is a precise optical component and the package material is plastic. Therefore.
   - Take care not to drop the device when mounting, handling, or transporting.
   - Avoid giving a shock to the package. Especially when leads are fixed to the shock and the circuit board, small shock could break the package more easily then when the package isn't fixed.

2) When applying force for mounting the device or any other purposes, fixed the leads between a joint and a stand_off, so that no stress will be given to the jointed part of the lead.
   In addition, when applying force, do it at a point below the stand_off part.
   ——— The leads of the package are fixed with package body (plastic) ,so stress added to a lead could cause a crack in the package body (plastic) in the jointed part of the lead.



3) When mounting the package on the housing, be sure that package is not bent.
   ——— If a bent package is forced into place between a hard plate or the like, the package may be broken.

4) If any damage or breakage occur on the surface of the glass cap, its characteristics could deteriorate.
   Therefore,
   - Do not hit the glass cap.
   - Do not give a shock large enough to cause distortion.
   - Do not scrub or scratch the glass surface.

   ——— Even a soft cloth or applicator, if dry, could cause dust to scratch the glass.

2. Electrostatic damage

As compared with general MOS-LSI, CCD has lower ESD.
Therefore, please take the following anti-static measures when handling the CCD:

1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide resistance of about 1 Meg ohm between the human body and the ground to be on the safe side.

2) When directly handling the device with fingers, hold the part without leads and do not touch any lead.

3) To avoid generating static electricity,
   a. do not scrub the glass surface with cloth or plastic
   b. do not attach any tape or labels
   c. do not clean the glass surface with dust-cleaning tape

4) When storing or transporting the device, put it in a container of conductive material.

3. Dust and contamination

Dust or contamination on the glass surface could deteriorate the output characteristic or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

1) Handle CCD in a clean environment such as a cleaned booth.
(The cleanliness level should be, if possible, class 1,000 at least.)

2) Do not touch the glass surface with fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:
- Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
- The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.

——— Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note: In more cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommend that the above procedures should be taken to wipe out dust and contamination before using the device.

4. Other

1) Soldering should be manually performed ~~within~~ 5 seconds at 350℃ maximum at soldering iron.

2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.

3) Do not expose the device to strong light. For the color devise, long exposure to strong light will fade the color of the color filters.

4) The exit pupil position of lens should be 15~50mm from the top surface of CCD.

11 PACKAGE OUTLINE AND PACKING SPECIFICATION

1. Package Outline Specification

Refer to attached drawing

(The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, white and transparency.)

2. Markings

Marking contents

(1) Product name : LZ23J3G

(2) Company name : SHARP

(3) Country of origin : JAPAN

(4) Date code : YY WW X XX

- XX: Denotes the production ref. code.(1 ~ 2 figures)
- X: Denotes the production day of the week.

1	2	3	4	5	6	7
SUN.	MON.	TUE.	WED.	THU.	FRI.	SAT.

- WW: Denotes the production week. (01,02,03, · · · · ,52,53)
- YY: Denotes the production year. (Lower two digits of the year.)

Positions of markings are shown in the package outline drawing .

But, markings shown in that drawing are not provided any measurements of their characters and their positions.

3. Packing Specification

3 − 1. Packing materiales

Material Name	Material Spec.	Purpose
Device case	Cardboard(150devices/case)	Device tray fixing
Device tray	Conductive plastic (50devices/tray)	Device packing(3trays/case)
Cover tray	Conductive plastic(1tray/case)	Device packing
PP band	Polypropylene	Device tray fixing
Buffer	Cardboard(2sheets/case)	Shock absorber of device tray
Plastic film bag	Plastic film	Device tray fixing
Tape	Paper	Sealing plastic film bag and device case
Label	Paper	Indicates part number, quantity and date of manufacture

3 − 2. External appearance of packing

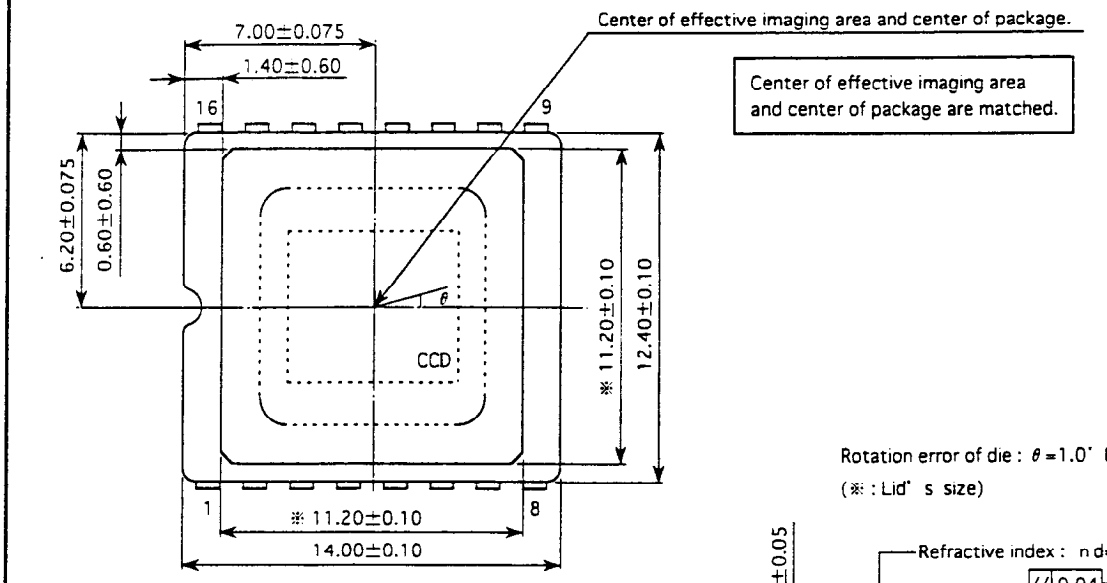
Refer to attached drawing

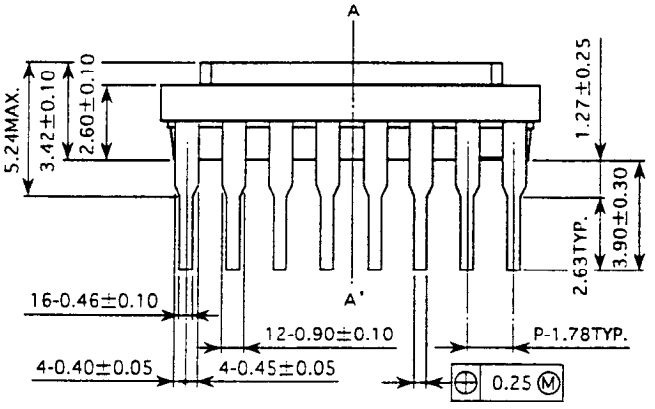
4. Precaution

1) Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specifications.

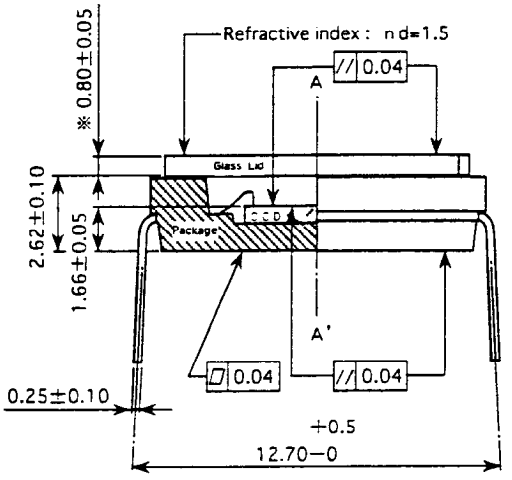
2) Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operater' s body, too.

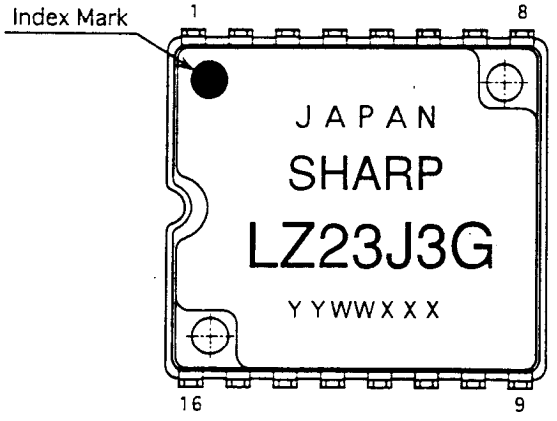
LZ23J3G





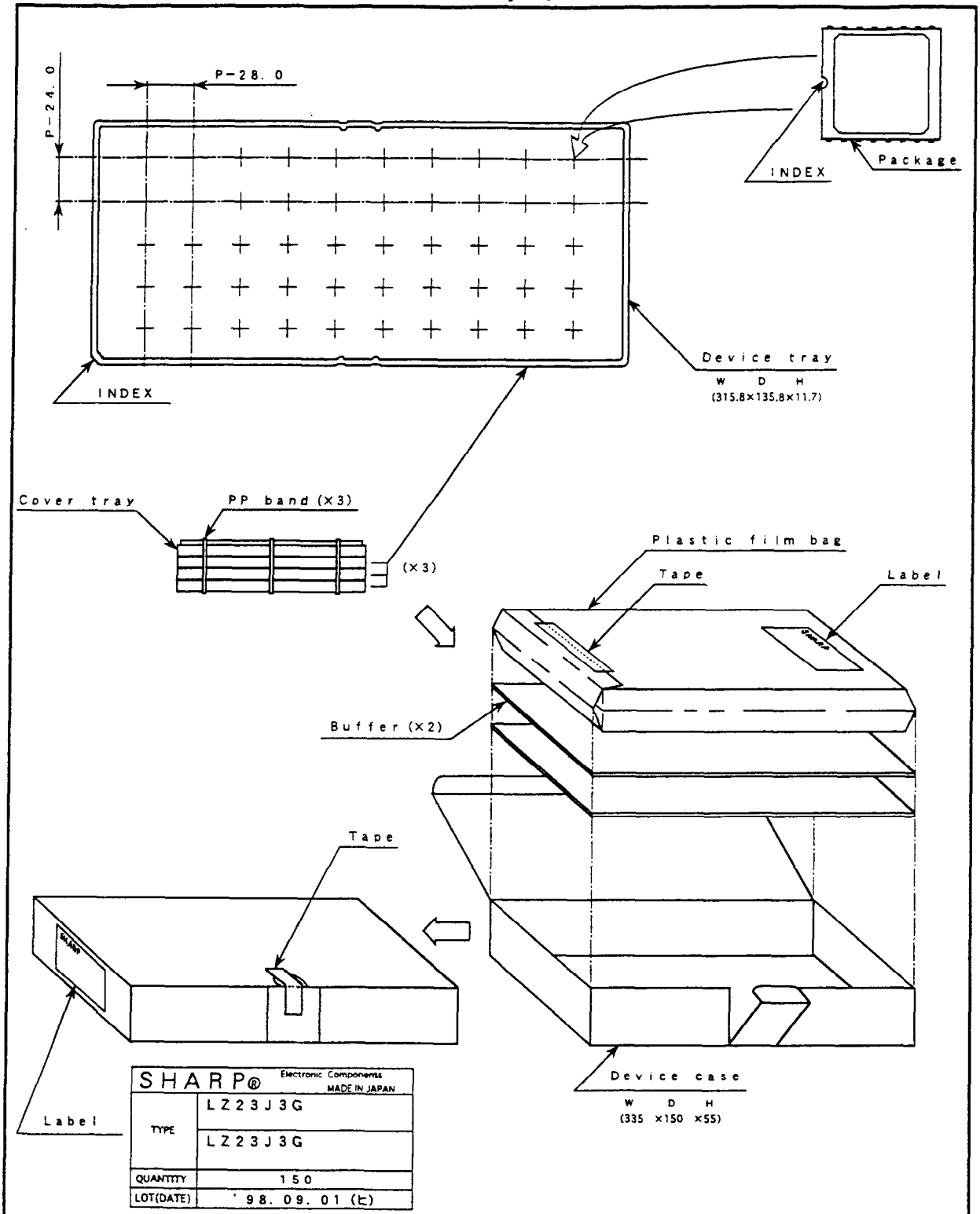
Rotation error of die : θ=1.0° MAX.
(※ : Lid's size)





(UNIT : mm)

材質 MATERIAL	仕 上 FINISH	名 称 NAME	WDIP16−P−500C Package Outline Specification
		コード CODE	
MODULE ASSEMBLY APPLICATION ENGINEERING DEPARTMENT			
INTEGRATED CIRCUITS (IC) GROUP		図 番 DRAWING No.	GDP016A−0DE2
SHARP CORPORATION			



(UNIT : mm)

材質 MATERIAL	仕 上 FINISH	名 称 NAME	External Appearance of Packing
		コード CODE	
MODULE ASSEMBLY APPLICATION ENGINEERING DEPARTMENT			
INTEGRATED CIRCUITS (IC) GROUP		図 番 DRAWING No.	KSEC-150T2-2
SHARP CORPORATION			