

	SPEC No.
То;	ISSUE : April 5, 1999
10 ,	
SPECIFICAT	ION ( PRELIMINARY )
Product Type <u>DIGITA</u>	L SIGNAL PROCESSOR FOR COLOR CAMERA
Model No LR	38602
	s ** pages including the cover and appendix. , please contact us before issuing purchasing order.
CUSTOMERS ACCEPTANCE	
DATE:	
BY:	<del></del>
	PRESENTED
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  - · Office electronics
  - · Instrumentation and measuring equipment
  - · Machine tools
  - · Audiovisual equipment
  - · Home appliances
  - · Communication equipment other than for trunk lines
  - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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  - · Mainframe computers
  - Traffic control systems
  - · Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - · Other safety devices and safety equipment, etc.
  - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
  - · Aerospace equipment
  - · Communications equipment for trunk lines
  - · Control equipment for the nuclear power industry
  - · Medical equipment related to life support, etc.
  - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.



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## 1. GENERAL

This is the digital signal processor for color USB camera system of 350K pixels CCD or CMOS imager with the primary color filter. This camera system can transfer images which is 30 frame/sec with VGA resolution through USB interface to PC.

	IMAGER	CDS/AGC/AD	V DRIVER	MICON	DSP
TYPE 1	CCD LZ24BP	IR3Y38M	LR36685	LU831603	LR38602
TYPE 2	CCD LZ24BP	IR3Y48M	LR36685	LU831603	LR38602
TYPE 3	CMOS LZ34B10	_		LU831603	LR38602
TYPE 4	CMOS LZ34C10	_	_	LU831603	LR38602

#### 1-1. FEATURES

- The process (structure) is CMOS.
- A P-type silicon circuit board is used.
- The package type is 100-pin QFP.
- The package material is plastic.
- Not designed or rated as radiation hardened.

## 1-2. FUNCTIONS

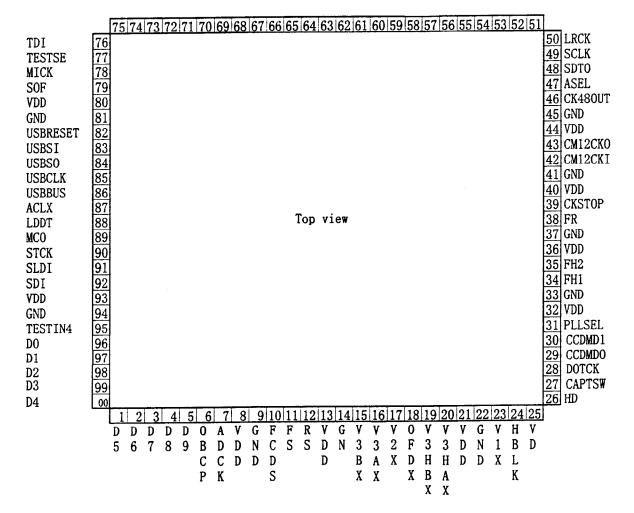
- Single +3.3V power supply
- · Available for either 350K CCD or 350K CMOS imager, with R,G and B color filter
- · Available for YUV digital output
- Built-in JPEG encorder
- · Built-in USB interface
- · Built-in Mirror image function
- · Built-in Pan, Tilt function
- · Auto Exposure control by external micom.
- · Auto White Balance control by external micom.
- Built-in Auto Carrier Balance control
- 10 bits digital input
- External control interface Input / Output



#### 2. PIN ASSIGNMENT

#### 2-1. PIN ASSIGNMENT

TTTTTGVGVKVVVROGVGVMPSSNM EEEENDNDEMPMCENDNDCACCCC S S S S D D D D 0 0 V D D D D S R M E L S A O N K T T TT T L D C I I I ML K N N N D Е 1 2 3





# 2-2. Pin table

PIN	SYMBOL	I/0	PIN	SYMBOL	I/0		PIN	SYMBOL	I/0	PIN	SYMBOL	I/0
1	D5	IBFC	26	HD	OBF2MA		51	MCLK	OBF2MA	76	TDI	IBFC
2	D6	IBFC	27	CAPTSW	IBFC		52	NC	_	77	TESTSET	IBFC
3	D7	IBFC	28	DOTCK	IBFC		53	SCEN	IBFC	78	MICK	OBF2MA
4	D8	IBFC	29	CCDMD0	IBFC		54	SCMOD	IBFC	79	SOF	OBF2MA
5	D9	IBFC	30	CCDMD1	IBFC		55	PARALEL	IBFC	80	VDD	
6	OBCP	OBF2MA	31	PLLSEL	IBFC		56	MCS	IBFC	81	GND	-
7	ADCK	OBF6MA	32	VDD	_		_57	VDD		82	USBRESET	OBF2MA
8	VDD	_	33	GND			58	GND		83	USBSI	OBF2MA
9	GND	-	34	FH1	OBF12MA		59	VDD		84	USBS0	OBF2MA
10	FCDS	OBF6MA	35	FH2	OBF12MA		60	GND		85	USBCLK	IOBFC2MA
11	FS	OBF6MA	36	VDD	-		61	0E	OBF2MA	86	USBBUS	OBF2MA
12	RS	OBF6MA	37	GND	_		62	RCV	IBFC	87	ACLX	IBFC
13	VDD	-	38	FR	OBF12MA		63	VMO	OBF2MA	88	LDDT	OBF2MA
14	GND	_	39_	CKSTOP	IBFC		64	VP0	OBF2MA	89	MCO	OBF2MA
15	V3BX	OBF2MA	40	VDD			65	VM	OBF2MA	90	STCK	IOBFC2MA
16	V3AX	OBF2MA	41	GND	-		66	VP	OBF2MA	91	SLDI	IOBFC2MA
17	V2X	OBF2MA	42	CM12CKI	IBFOA		67	VDD	-	92	SDI	IBFC
18	OFDX	OBF2MA	43	CM12CKO	OSCX		68	GND		93	VDD	
19	V3HBX	OBF2MA	44	VDD			69	VDD	-	94	GND	-
20	V3HAX	OBF2MA	45	GND			70	GND		95	TESTIN4	IBFC
21	VDD	_	46	CK480UT	OBF2MA		71	TESTMD	IBFC	96	D0	IBFC
22	GND	-	47	ASEL	IOBFC2MAU1		72	TESTIN3	IBFC	97	D1	IBFC
23		OBF2MA	48	SDT0	IOBFC2MAU1		73	TESTIN2	IBFC	98	D2	IBFC
24	HBLK	OBF2MA	49	SCLK	OBF2MA		74	TESTIN1	IBFC	99	D3	IBFC
25	VD	OBF2MA	50	LRCK	OBF2MA	Į	75	TESTCK	IBFC	100	D4	IBFC

IC : Input pin under the condition of CMOS 3.3 V

ICU : Input pin under the condition of CMOS 3.3 V with a pull-up register
 ICD : Input pin under the condition of CMOS 3.3 V with a pull-down register
 ICS : Input pin under the condition of Schmidt 3.3 V with a pull-down register

O : Output pin with 2 mA 3.3 V

TO : Tri-state output pin with 2 mA 3.3 V XTO : Tri-state output pin with 2 mA 3.3 V

# 4. PIN DESCRIPTION

NO.	SYMBOL	I/0	FUNCTION			
1	D5	I				
2	D6	I	Digital signal inputs.			
3	D7	I	D9 is MSB.			
4	D8	I				
5	D9	I				
6	OBCP	0	Optical black clamp pulse output			
7	ADCK	0	AD converter clock pulse output to IR3Y38M/IR3Y48M			
8	VDD	I	+3.3V input			
9	GND	_	Ground			
10	FCDS	0	Clamping pulse output for CDS of IR3Y38M/IR3Y48M			
11	FS	0	Samping pulse output for CDS of IR3Y38M/IR3Y48M			
12	RS	0	Samping pulse output for CDS of IR3Y38M/IR3Y48M			
13	VDD	I	+3.3V input			
14	GND	_	Ground			
15	V3BX	0	Vertical transfer pulse output to LR36685			
16	V3AX_	0	Vertical transfer pulse output to LR36685			
17	V2X	0	Vertical transfer pulse output to LR36685			
18	OFDX	0	Vertical transfer pulse output to LR36685			
19	V3HBX	0	Vertical transfer pulse output to LR36685			
20	V3HAX	0	Vertical transfer pulse output to LR36685			
21	VDD	I	+3.3V input			
22	GND	_	Ground			
23	V1X	0	Vertical transfer pulse output to LR36685			
24	HBLK	0	Horizontal blanking pulse output.			
25	VD	0	Vertical blanking pulse output.			
26	HD	0	Horizontal drive pulse output			
27	CAPTSW	I ·	<u>S</u> nap-shot mode control			
			L:Motion image H:Snap-shot (Still image capture)			
28	DOTCK	0	Clock input from CMOS imager LZ34B10/LZ34C10			
			LZ34B10:12MHz LZ34C10:9MHz			
29	CCDMD0	I	Imager choice			
30	CCDMD1	I	PIN 29=L PIN29=H			
			PIN30=L LZ24BP LZ34C10			
			PIN30=H   PROHIBITED   LZ34B10			
31	PLLSEL	I	Built-in PLL choice			
32	VDD	I	+3.3V input			
33	GND	_ :	Ground			

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# **SHARP**

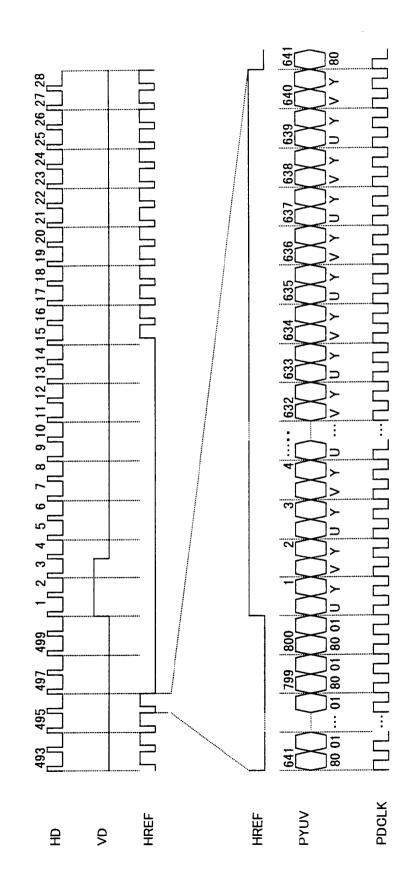
NO.	SYMBOL	I/0	FUNCTION		
34	FH1	0	Horizontal transfer pulse output to LZ24BP		
35	FH2	0	Horizontal transfer pulse output to LZ24BP		
36	VDD	I	+3.3V input		
37	GND	_	Ground		
38	FR	0	Horizontal reset pulse output to LZ24BP		
39	CKST0P	I	Clock oscillator control for the suspended mode		
40	VDD	I	+3.3V input		
41	GND		Ground		
42	CM12CKI	I	Clock input PIN31=L:12MHz PIN31=H:48MHz		
43	CM12CKO	0	Clock output PIN31=L:12MHz PIN31=H:48MHz		
44	VDD	I	+3.3V input		
45	GND	_	Ground		
46	CK480UT	0	Not used		
47	ASEL	I/0	Audio function L:Available H:Not available		
48	SDTO	I/0	Serial audio signal data input		
49	SCLK	0	Clock output of serial audio signal data (750KHz)		
50	LRCK	0	Audio signal sampling pulse output (11.71KHz)		
51	MCLK	0	Audio main clock output (3MHz)		
52	NC	_	Non connection		
53	SCEN	I	Test input. Connected to Ground		
54	SCMOD	I	Test input. Connected to Ground		
55	PARALLEL	I	Output mode L:USB H:8bit parallel(See PAGE 8)		
56	MCS	I	Hand-shake signal with CPU in USB		
57	VDD	I	+3.3V input		
58	GND		Ground .		
59	VDD	I	+3.3V input		
60	GND	_	Ground		
61	OE	0	Output enable pulse output in USB		
62	RCV	I	USB data input		
63	VMO	0	D- output in USB		
64	VP0	0	D+ output in USB		
65	VM	I	D- input in USB		
66	VP	I	D+ input in USB		
67	VDD	I	+3.3 V input		
68	GND	_	Ground		
69	VDD	I	+3.3 V input		
70	GND	-	Ground		

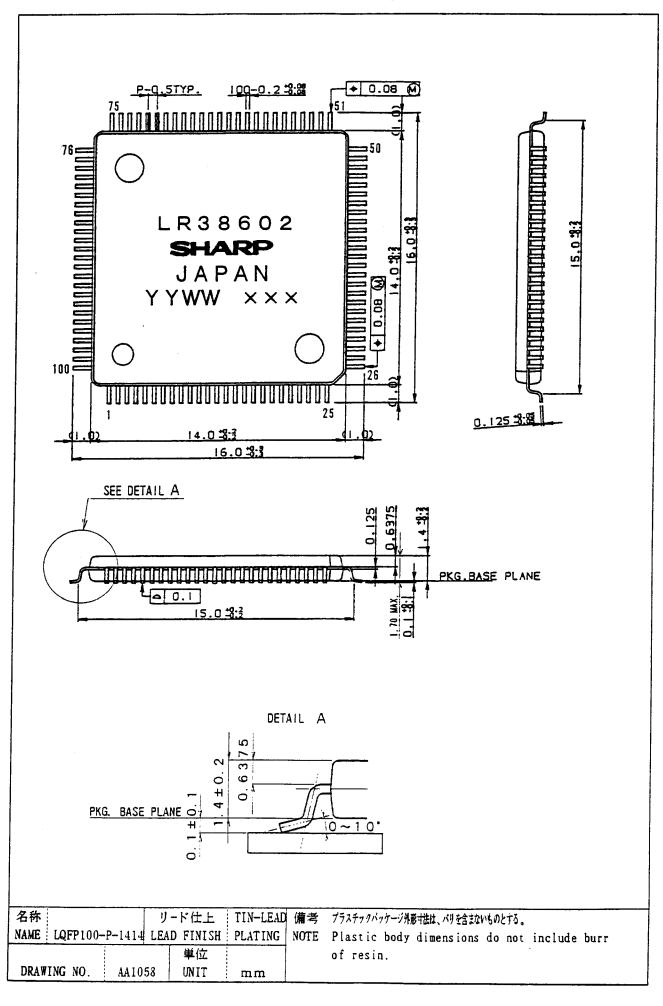
NO.	SYMBOL	I/0	FUNCTION	
71	TESTMD	I	Test input. Connected to Ground	
72	TESTIN3	I	Test input. Connected to Ground	
73	TESTIN2	I	DBURST2 input	
74	TESTIN1	I	Test input. Connected to Ground	
75	TESTCK	I	Test input. Connected to Ground	
76	TDI	I	Test input. Connected to Ground	
77	TESTSET	I	Test input. Connected to Ground	
78	MICK	0	Clock output to CPU (4.8MHz)	
79	SOF	0	Frame start signal in USB	
80	VDD	I	+3.3V input	
81	GND	_	Ground	
82	USBRESET	I	Reset input in USB	
83	USBSI	I	Serial control data input in USB	
84	USBS0	0	Serial control data output in USB	
85	USBCLK	I	Serial clock input in USB	
86	USBBUS	0	Busy signal output in USB	
87	ACLX	I	Reset input	
88	LDDT	0	Serial data output for AWB/EE control	
89	MCO	0	Serial data ready output	
90	STCK	I/0	Serial clock input for register	
91	SLDI		Serial strobe input for register	
92	SDI	I	Serial data input for register	
93	VDD	I	+3.3V input	
94	GND		Ground	
95	TESTIN4	I	Test input. Connected to Ground	
96	D0	I		
97	D1	I	Digital data inputs	
98	D2	I	DO:LSB	
99	D3	I		
100	D4	I		

8 hit parallel output at PIN 55=HIGH

bit para	llel output at PIN	55=HIGH	
PIN 47	UYVY bit 0	PIN 83	UYVY bit 6
PIN 48	UYVY bit 1	PIN 84	UYVY bit 7
	UYVY bit 2	PIN 86	Pixel clock output
PIN 50	UYVY bit 3	PIN 85	ID pulse for effective pixels
PIN 51	UYVY bit 4		
PIN 82	UYVY bit 5		

Digital Output Format







## 9 Package and packing specification

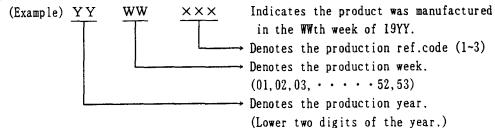
1. Package Outline Specification
Refer to drawing No. AA1058

## 2. Markings

2-1. Marking contents

(1) Product name : LR38602(2) Company name : SHARP

(3) Date code



(4) The marking of "JAPAN" indicates the country of origin.

2-2. Marking layout

Refer to drawing No.AA1058

(This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3-1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (60devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (ltray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (600devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

- 3-2. Outline dimension of tray
  Refer to attached drawing.
- 4. Storage and Opening of Dry Packing
  - 4-1. Store under conditions shown below before opening the dry packing

(1) Temperature range :  $5\sim40^{\circ}$ C

(2) Humidity : 80% RH or less

- 4-2. Notes on opening the dry packing
  - (1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
  - (2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.
- 4-3. Storage after opening the dry packing

Perform the following to prevent absorption of moisture after opening.

- (1) After opening the dry packing, store the ICs in an environment with a temperature of  $5\sim25^{\circ}$ C and a relative humidity of 60% or less and mount ICs within 4 days after opening dry packing.
- (2) To re-store the ICs for an extended period of time within 4 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5∼40°C and a relative humidity of 80% or less, and mount ICs within 2 weeks.
- (3) Total period of storage after first opening and re-opening is within 4 days, and store the ICs in the same environment as section 4-3.(1).

First opening  $X_1 \longrightarrow re$ —sealing  $Y \longrightarrow re$ —opening  $X_2 \longrightarrow mounting$ ICs in dry  $5\sim25\%$   $5\sim40\%$   $5\sim25\%$  packing 60% RH or less 80% RH or less 60% RH or less

 $X_1 + X_2$ : within 4 days Y: within 2 weeks

- 4-4. Baking (drying) before mounting
  - (1) Baking is necessary
    - (A) If the humidity indicator in the desiccant becomes pink
    - (B) If the procedure in section 4-3 could not be performed
  - (2) Recommended baking conditions If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16~24 hours at 120℃. Heat resistance tray is used for shipping tray.
  - (3) Storage after baking
    After baking ICs, store the ICs in the same environment as section
    4-3.(1).

5. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5-1. Soldering conditions (The following conditions are valid only for one time soldering.)

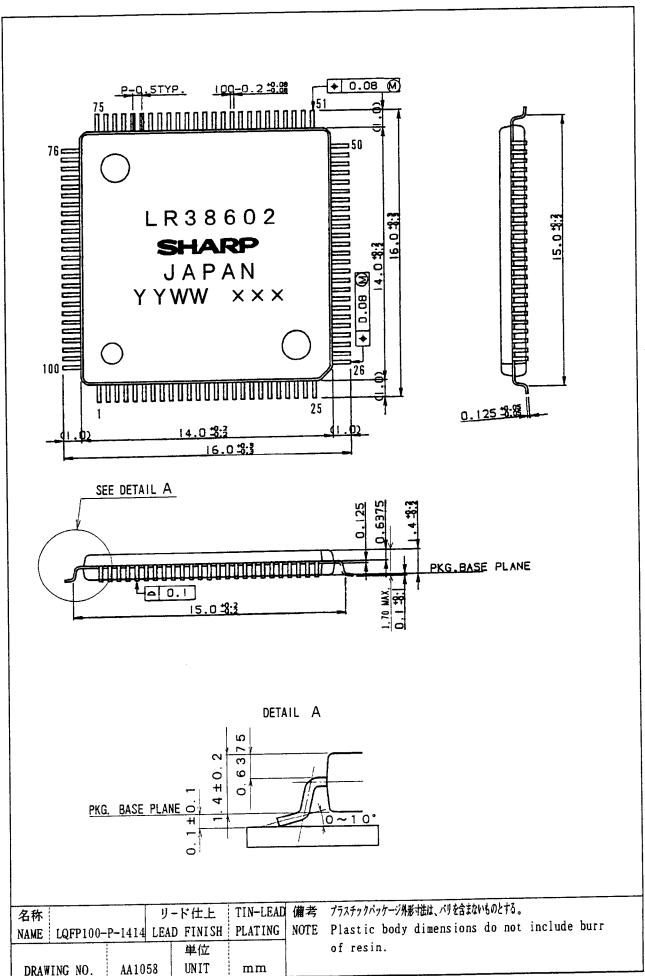
Mounting Method	Mounting Method Temperature and Duration	
Reflow soldering	Peak temperature of 230°C or less,	IC package
(air)	duration of less than 15 seconds.	surface
	200℃ or over, duration of less than 40 seconds.	
	Temperature increase rate of 1~4°C/second.	
Vapor phase	215℃ or less, duration of less	Steam
soldering	than 40 seconds above 200℃	
Manual soldering	260°C or less, duration of less	IC outer
(soldering iron)	than 10 seconds	lead surface

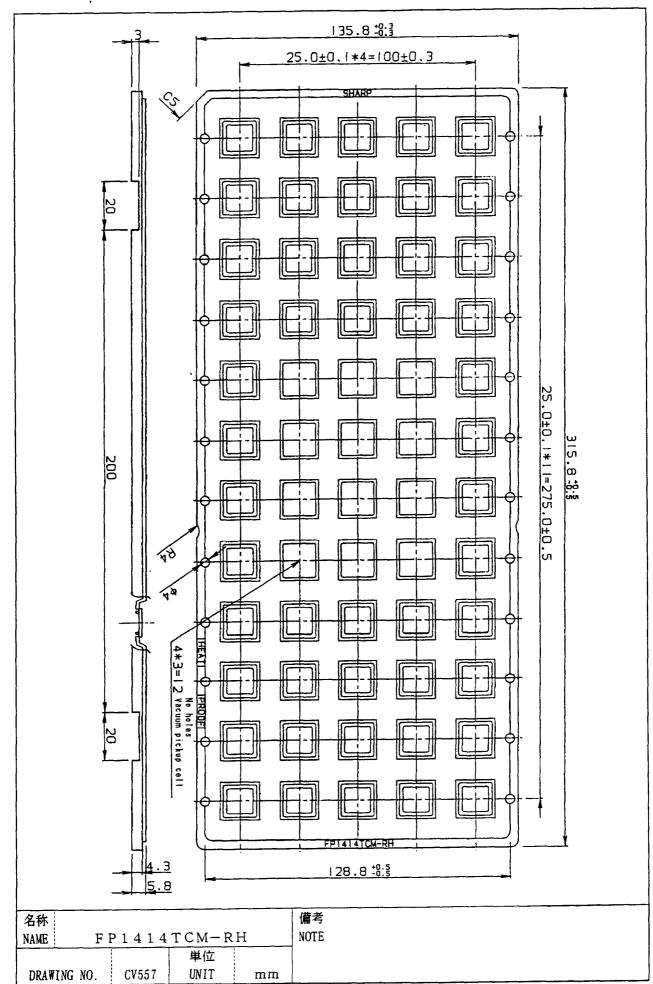
5-2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less

(2) Washing time : Total 1 minute maximum

(3) Solvent temperature : 15~40℃





《Supplementary data》

	LR38602
Recommended mounting	g conditions for two time reflow soldering .
Product name(Package)	LR38602(LQFP100-P-1414)
Packing specification	Tray (Dry packing)
Mounting method	Reflow soldering (Air)
Reflow soldering conditions	Peak temperature of 230℃ or less.
ļ	200℃ or over, duration of less than 40 seconds.
	Preheat temperature of 125∼150°C, duration of less
	than 180 seconds. Temperature increase rate of
	1~4°C/s econd.
Measurement point	IC package surface
Storage conditions	After opening the dry packing, store the ICs in an environment with a temperature of 5~25°C and a relative humidity of 60% or less. If doing reflow soldering twice, do the first reflow soldering within 36 hours after opening dry packing and do the second reflow soldering within 36 hours after the first reflow soldering.
Note	If the above storage conditions are not applicable, bake it before reflow soldering. The recommended conditions are 16~24 hours at 120°C.  (Heat resistance tray is used for shipping tray.)

# Recommended Reflow Soldering (Air) Temperature Profile

