LR38266

Digital Signal Processor for Color CCD Cameras

DESCRIPTION

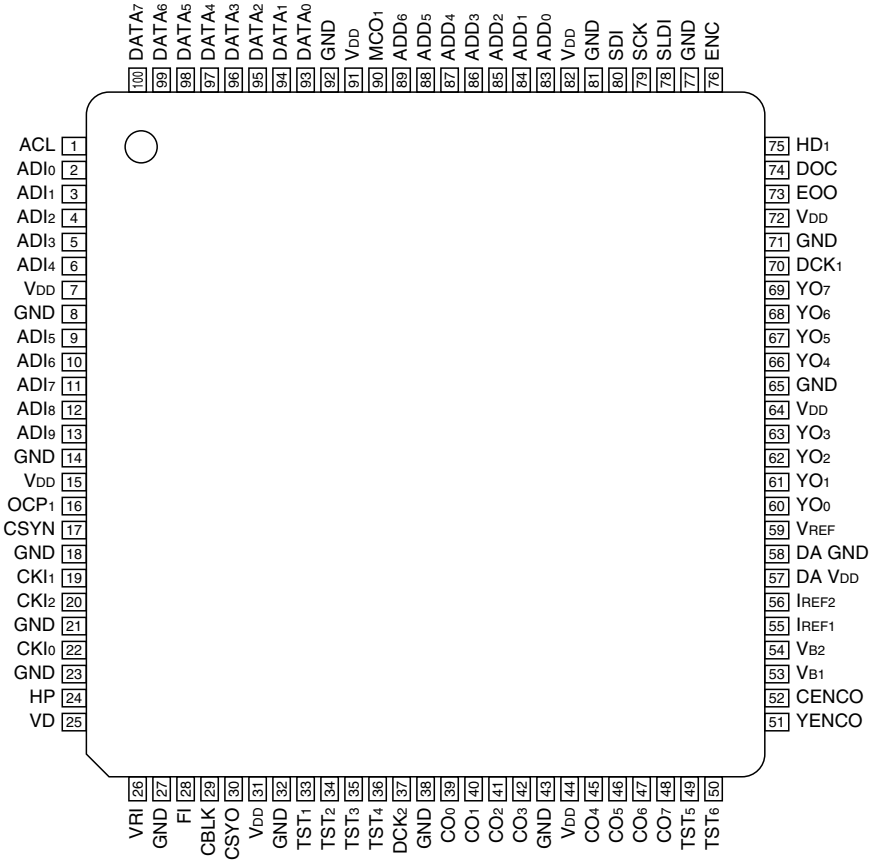
The LR38266 is a CMOS digital signal processor for color CCD camera systems of 270 k/320 k/410 k/470 k-pixel CCD with complementary color filters.

FEATURES

- Designed for 270 k/320 k/410 k/470 k color CCDs with Mg, G, Cy, and Ye complementary color filters
- Switchable between NTSC and PAL modes
- External performance control
- Variable GAMMA and KNEE response
- 8 to 10-bit digital input
- Analog Y&C output by built-in 8-bit 2 ch DA converter
- Switchable between Y, U/V (16 bits) and U/Y/V/Y (8 bits) digital video output
- Line-lock and external lock function
- CPU interface input/output
- Accumulator to control auto exposure and auto white balance
- Single +3.3 V power supply
- Package :
  100-pin LQFP (LQFP100-P-1414) 0.5 mm pin-pitch

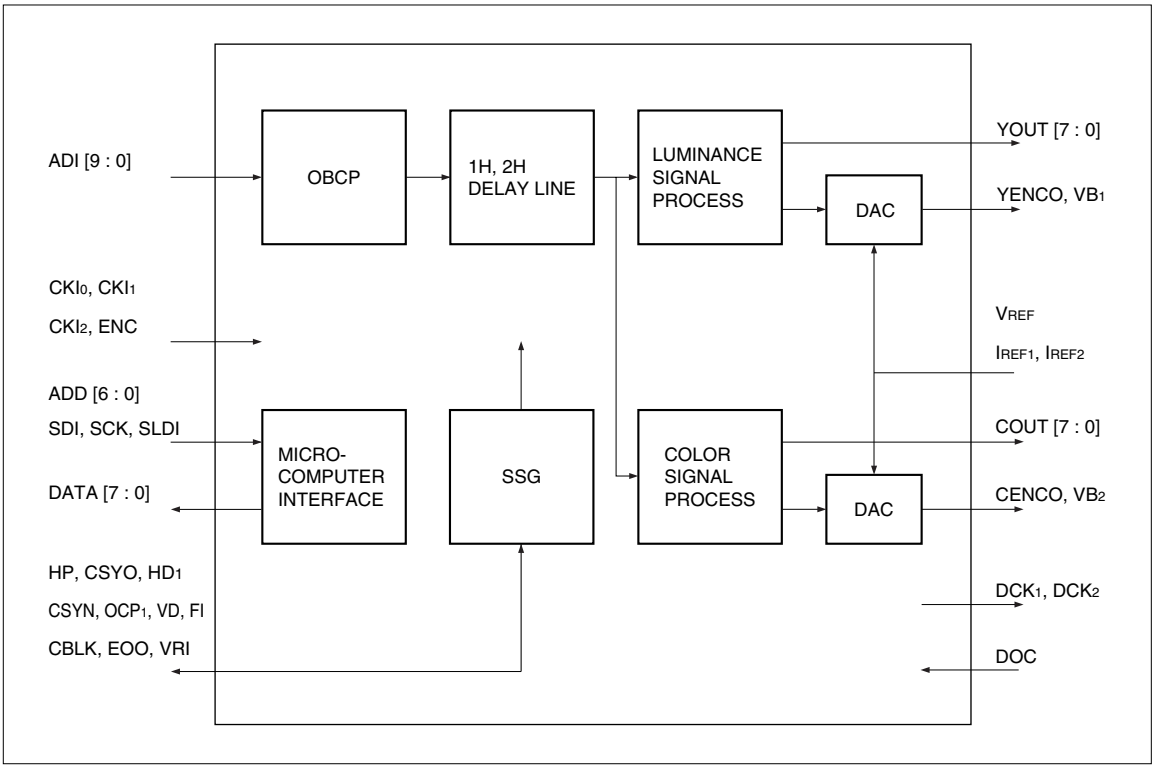
PIN CONNECTIONS

100-PIN LQFP TOP VIEW



(LQFP100-P-1414)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
1	ACL	ICU		All reset input. The internal circuit is initialized at power-on with a capacitor of 0.01 µF.
2	ADI_0	IC		ADI_0 to ADI_9 are digital signal inputs. ADI_0 is LSB. ADI_9 is MSB.
3	ADI_1	IC		
4	ADI_2	IC		
5	ADI_3	IC		
6	ADI_4	IC		
7	V_{DD}	–		Supply of +3.3 V power.
8	GND	–		A grounding pin.
9	ADI_5	IC		ADI_0 to ADI_9 are digital signal inputs. ADI_0 is LSB. ADI_9 is MSB.
10	ADI_6	IC		
11	ADI_7	IC		
12	ADI_8	IC		
13	ADI_9	IC		
14	GND	–		A grounding pin.
15	V_{DD}	–		Supply of +3.3 V power.
16	OCP_1	O		Optical black clamp pulse output.
17	CSYNC	O		Composite synchronous pulse output for analog video output.
18	GND	–		A grounding pin.
19	CKI_1	IC		Clock input. The frequency is below for each CCD. 270 k, 410 k CCD : 14.31818 MHz 320 k, 470 k CCD : 14.1875 MHz
20	CKI_2	IC		Clock input. The frequency is below for each CCD. 270 k CCD : 9.5454 MHz 320 k CCD : 9.4583 MHz 410 k CCD : 14.3181 MHz 470 k CCD : 14.1875 MHz
21	GND	–		A grounding pin.
22	CKI_0	IC		Clock input. The frequency is below for each CCD. 270 k, 410 k CCD : 28.6363 MHz 320 k, 470 k CCD : 28.3750 MHz
23	GND	–		A grounding pin.
24	HP	O		Horizontal drive pulse output.
25	VD	O		Vertical drive pulse output.
26	VRI	ICS		Vertical reset input. Built-in vertical counter is reset by a low-input of more than one horizontal period.
27	GND	–		A grounding pin.
28	FI	O		Field index pulse output.
29	CBLK	O		Composite blanking pulse output.
30	CSYO	O		Composite synchronous pulse output. Output timing is variable by output mode.
31	V_{DD}	–		Supply of +3.3 V power.
32	GND	–		A grounding pin.

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
33	TST_1	ICD		Test input. Connected to low or open.
34	TST_2	ICD		Test input. Connected to low or open.
35	TST_3	ICD		Test input. Connected to low or open.
36	TST_4	ICD		Test input. Connected to low or open.
37	DCK_2	O		Clock output for digital COUT.
38	GND	–		A grounding pin.
39	CO_0	TO		8-bit digital color signal output. CO_0 is LSB. CO_7 is MSB.
40	CO_1	TO		
41	CO_2	TO		
42	CO_3	TO		
43	GND	–		A grounding pin.
44	V_{DD}	–		Supply of +3.3 V power.
45	CO_4	TO		8-bit digital color signal output. CO_0 is LSB. CO_7 is MSB.
46	CO_5	TO		
47	CO_6	TO		
48	CO_7	TO		
49	TST_5	ICD		Test input. Connected to low or open.
50	TST_6	ICD		Test input. Connected to low or open.
51	YENCO	DAO		Analog Y signal output.
52	CENCO	DAO		Analog C signal output.
53	V_{B1}	DAO		Bias voltage output of built-in DA converter, connected to GND through a capacitor.
54	V_{B2}	DAO		Bias voltage output of built-in DA converter, connected to GND through a capacitor.
55	I_{REF1}	DAO		Bias current output of built-in DA converter, connected to GND through a resistor.
56	I_{REF2}	DAO		Bias current output of built-in DA converter, connected to GND through a resistor.
57	DA V_{DD}	–		Supply of +3.3 V power input for built-in DA converter.
58	DA GND	–		A grounding pin for built-in DA converter.
59	V_{REF}	DAI		Bias voltage input of built-in DA converter, connected to +1.0 V power supply.
60	YO_0	TO		Y digital outputs. YO_0 is LSB. YO_7 is MSB.
61	YO_1	TO		
62	YO_2	TO		
63	YO_3	TO		
64	V_{DD}	–		Supply of +3.3 V power.
65	GND	–		A grounding pin.
66	YO_4	TO		Y digital outputs. YO_0 is LSB. YO_7 is MSB.
67	YO_5	TO		
68	YO_6	TO		
69	YO_7	TO		

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
70	DCK_1	O		Clock output for YO output.
71	GND	–		A grounding pin.
72	V_{DD}	–		Supply of +3.3 V power.
73	EOO	XTO		Phase detector output comparing internal HD and HD_1.
74	DOC	ICD		Control input of YO and CO. H level sets both YO and CO high-impedance.
75	HD_1	O		Horizontal drive pulse generated from ENC (pin 76).
76	ENC	IC		Clock input to encode color signal. Internal Synchronous mode : CKI_2 Line Lock mode : same as CCD clock from outside or 4 f_{SC}.
77	GND	–		A grounding pin.
78	SLDI	IC		Data input to set each coefficient of DSP.
79	SCK	IC		Clock pulse input to set SLDI data to DSP.
80	SDI	IC		Timing pulse input to set SLDI data to DSP.
81	GND	–		A grounding pin.
82	V_{DD}	–		Supply of +3.3 V power.
83	ADD_0	IC		Address input to select an output data of DATA pins used in auto white balance and auto exposure. For details, see "**Data Interface Timing**".
84	ADD_1	IC		
85	ADD_2	IC		
86	ADD_3	IC		
87	ADD_4	IC		
88	ADD_5	IC		
89	ADD_6	IC		
90	MCO_1	O		Control output to update internal data stored in DSP register. Data is updated at the rising edge of MCO_1.
91	V_{DD}	–		Supply of +3.3 V power.
92	GND	–		A grounding pin.
93	$DATA_0$	O		Data output to control auto white balance and auto exposure. Data of address set by ADD inputs is output. For details, see "**Data Interface Timing**".
94	$DATA_1$	O		
95	$DATA_2$	O		
96	$DATA_3$	O		
97	$DATA_4$	O		
98	$DATA_5$	O		
99	$DATA_6$	O		
100	$DATA_7$	O		

IC : Input pin (CMOS level)
ICU : Input pin (CMOS level with pull-up resistor)
ICD : Input pin (CMOS level with pull-down resistor)
ICS : Input pin (CMOS schmitt-trigger level with pull-down resistor)
DAI : Input pin for DA converter
O : Output pin
TO : Tri-state output pin
XTO : Tri-state output pin
DAO : DA converter output pin

INTERNAL COEFFICIENT TABLE

ADDRESS	NAME	BIT	CONTENTS			
00h			Not used			
01h	STB_DA	6	Standby of DA converter			1 : Standby
	OUTPUT2	5	Output format option	bit 4 = 0 Y/C (bit 5 = 0)		U/Y/V/Y (bit 5 = 1)
	OUTPUT1	4	Output format option	bit 4 = 1 Y, U/V (bit 5 = 0)		Prohibited (bit 5 = 1)
	TVMD	3	TV format option		0 : NTSC	1 : PAL
	TYPE2	2	CCD option	bit 2 = 0		bit 2 = 1
	TYPE1	1	CCD option	bit 1 = 0 270 k/320 k with mirror		Prohibited
				bit 1 = 1 270 k/320 k		410 k/470 k
	MIR	0	Image type option		0 : Normal	1 : Mirror
02h	ADTI1	6	Input data is delayed by 1 clock cycle		0 : Not delayed	1 : Delayed
	ADTI2	5	The clock type to input the data		0 : Non-inverted	1 : Inverted
	APTVC	4	Vertical edge enhancement		0 : ON	1 : OFF
	APTHC	3	Horizontal edge enhancement		0 : ON	1 : OFF
	CKIL	2	Color killer function		0 : ON	1 : OFF
	MUTE_D	1	Muting digital signal outputs		0 : OFF	1 : ON
	MUTE_A	0	Muting analog signal outputs		0 : OFF	1 : ON
03h	EOOCTRL	4	The polarity of EOO output		0 : Normal	
	INVSP	3	The polarity of SP1, SP2		0 : Normal	
	HGCO	2	The polarity of HG		0 : Normal	
	INTL	1	Interlace/Non-Interlace		0 : Interlace	
	EX_SXB	0	Standby of EOO function		0 : Standby	
04h	TESYL	5	Set YL zero in color processing		0 : OFF	1 : ON
	K1	4	Prohibited to change		0 : Should be kept as is	
	RAM_ST	2	Standby of delay lines		0 : OFF	1 : ON
	SEL_UV	1	The option of U/V sequence		0 : Normal	
	SEL_RB	0	The option of R/B sequence		0 : Normal	
06h	CSYNCVARI	8 bits	Position tuning of CSYNC with the range from +8 clock to −7 clock of CKI_1. Upper 4 bits : CSYNC, Lower 4 bits : CSYO			
07h	CBLKBALI	8 bits	Position tuning of CBLK with the ditto range.			
08h	CBK_Y	7	The position tuning of Y-CBLK by CKI_2 clock		bit 7 = 0	bit 7 = 1
	CBK_Y	6		bit 6 = 0	No tune	−1 clock
				bit 6 = 1	1 clock	−1 clock
	CBLK_C	5	The position tuning of modulated C-CBLK by CKI_2 clock		bit 5 = 0	bit 5 = 1
	CBLK_C	4		bit 4 = 0	No tune	−1 clock
				bit 4 = 1	1 clock	−1 clock
	CBLK_UV	3	The position tuning of baseband C-CBLK by CKI_2 clock		bit 3 = 0	bit 3 = 1
	CBLK_UV	2		bit 2 = 0	No tune	−1 clock
				bit 2 = 1	1 clock	−1 clock
	BFVARI	1	The position tuning of color burst signal by CKI_2 clock		bit 1 = 0	bit 1 = 1
	BFVARI	0		bit 0 = 0	No tune	−1 clock
				bit 0 = 1	1 clock	−1 clock

ADDRESS	NAME	BIT	CONTENTS
11h	CSP_R1	8 bits	Coefficient to extract red color component
12h	CSP_B1	8 bits	Coefficient to extract blue color component
13h	CSP_R2	7 bits	Coefficient to tune the base level of red signal
14h	CSP_B2	7 bits	Coefficient to tune the base level of blue signal
15h 16h	CB_R1 CB_R2	6 bits 8 bits	Coefficient of the black balance of red signal (15h) MSB : sign, other 5 bits : upper 5 bits of coefficient (16h) lower 8 bits of coefficient
17h 18h	CB_B1 CB_B2	6 bits 8 bits	Coefficient of the black balance of blue signal (17h) MSB : sign, other 5 bits : upper 5 bits of coefficient (18h) lower 8 bits of coefficient
19h 1Ah	WB_R1 WB_R2	1 bit 8 bits	Upper coefficient to make white balance of red signal (19h) MSB of coefficient (1Ah) lower 8 bits
1Bh 1Ch	WB_B1 WB_B2	1 bit 8 bits	Upper coefficient to make white balance of blue signal (1Bh) MSB of coefficient (1Ch) lower 8 bits
1Dh	MAT R – Y	6 bits	Coefficient of R – Y matrix (MSB) sign bit
1Eh	MAT B – Y	6 bits	Coefficient of B – Y matrix (MSB) sign bit
1Fh	GA R – Y	6 bits	Coefficient of R – Y gain
20h	GA B – Y	6 bits	Coefficient of B – Y gain
21h	ENC_TI	3	The clock type of encoder input 0 : Non-Inverted 1 : Inverted
	L_fsc	2	Latched by fsc clock before encoding 0 : Latched 1 : Non-latched
	MO_ENC	1	Encoding phase of PAL 0 : 4 phases 1 : 16/5 phases
	MUTE_E	0	Muting color signal at encoder 0 : Normal 1 : Muting
22h	BAS R – Y	8 bits	Coefficient of color burst level at R – Y (MSB) sign bit
23h	BAS B – Y	8 bits	Coefficient of color burst level at B – Y (MSB) sign bit
24h	WBA_IP	8 bits	Positive range of white color signal at I-axis
25h	WBA_IM	8 bits	Negative range of white color signal at I-axis
26h	WBA_QP	8 bits	Positive range of white color signal at Q-axis
27h	WBA_QM	8 bits	Negative range of white color signal at Q-axis
28h	WBA_SEL	2 bits	Option of color signal type I/Q or R – Y/B – Y
29h	WB_HCL	8 bits	Limiter of AWB function at higher luminance level
2Ah	WB_LCL	8 bits	Limiter of AWB function at lower luminance level
2Bh	CKI_HCL	8 bits	Color suppression point at higher luminance level
2Ch	CKI_LCL	8 bits	Color suppression point at lower luminance level
2Dh	CKI_HLGA	8 bits	Luminance level to suppress color signal Upper 4 bits : higher luminance level Lower 4 bits : lower luminance level

ADDRESS	NAME	BIT	CONTENTS		
2Eh	HT_SIG	6	Color killer timing at higher luminance	bit 6, bit 5, bit 4	000 : No tuning
				001	1 clock cycle delay
	HT_1	5		010, 011	2 clock cycles delay
				100, 101, 110	2 clock cycles advance
	HT_0	4		111	1 clock cycle advance
	LT_SIG	2	Color killer timing at lower luminance	bit 2, bit 1, bit 0	000 : No tuning
				001	1 clock cycle delay
	LT_1	1		010, 011	2 clock cycles delay
				100, 101, 110	2 clock cycles advance
	LT_0	0		111	1 clock cycle advance
2Fh	CKI_HECL	8 bits	Horizontal aperture level to suppress color signal		
30h	CKI_VECL	8 bits	Vertical aperture level to suppress color signal		
31h	CKI_EGA	8 bits	Aperture level to suppress color signal Upper 4 bits : vertical aperture level Lower 4 bits : horizontal aperture level		
32h	SEL_ESFT	7	Level of edge signal	0 : 1/4 times	1 : 1 time
	VET_SIG	6	Color killer timing at vertical transient portion	bit 6, bit 5, bit 4	000 : No tuning
				001	1 clock cycle delay
	VET_1	5		010, 011	2 clock cycles delay
				100, 101, 110	2 clock cycles advance
	VET_0	4		111	1 clock cycle advance
	HET_SIG	2	Color killer timing at horizontal transient portion	bit 2, bit 1, bit 0	000 : No tuning
				001	1 clock cycle delay
	HET_1	1		010, 011	2 clock cycles delay
				100, 101, 110	2 clock cycles advance
	HET_0	0		111	1 clock cycle advance
33h	CKI_LEV	5 bits	Level to suppress color signal		
34h	NSUP_R – Y	8 bits	Coring level of R – Y signal		
35h	NSUP_B – Y	8 bits	Coring level of B – Y signal		
36h	C_NE1	2	The polarity of color signal	0 : Normal	1 : Inverted
	C_NE2	1	The polarity of color signal at gamma output	0 : Normal	1 : Inverted
	BLK_CTRL	0	CBLK availability at output	0 : ON	1 : OFF
37h	YL_SFT1	2 bits	Base level of YL signal (37h) Upper 2 bits of coefficient (38h) Lower 8 bits of coefficient		
38h	YL_SFT2	8 bits			
39h	YL_AMP	8 bits	YL signal level to make R – Y and B – Y		
40h	CGAM-A1	8 bits	1st input range of color gamma correction		
41h	CGAM-A2	8 bits	2nd input range of color gamma correction		
42h	CGAM-A3	8 bits	3rd input range of color gamma correction		
43h	CGAM-A4	8 bits	4th input range of color gamma correction		
44h	CGAM-A5	8 bits	5th input range of color gamma correction		

ADDRESS	NAME	BIT	CONTENTS
45h	CGAM-A6	8 bits	6th input range of color gamma correction
46h	CGAM-A7	8 bits	7th input range of color gamma correction
47h	CGAM-A8	8 bits	8th input range of color gamma correction
48h	CGAM-A9	8 bits	9th input range of color gamma correction
49h	CGAM-P1	8 bits	Offset of 1st straight line at color gamma correction
4Ah	CGAM-P2	8 bits	Offset of 2nd straight line at color gamma correction
4Bh	CGAM-P3	8 bits	Offset of 3rd straight line at color gamma correction
4Ch	CGAM-P4	8 bits	Offset of 4th straight line at color gamma correction
4Dh	CGAM-P5	8 bits	Offset of 5th straight line at color gamma correction
4Eh	CGAM-P6	8 bits	Offset of 6th straight line at color gamma correction
4Fh	CGAM-P7	8 bits	Offset of 7th straight line at color gamma correction
50h	CGAM-P8	8 bits	Offset of 8th straight line at color gamma correction
51h	CGAM-P9	8 bits	Offset of 9th straight line at color gamma correction
52h	CGAM-P10	8 bits	Offset of 10th straight line at color gamma correction
53h	CGAM-F	1 bit	Polarity of color gamma correction 0 : + 1 : –
54h	CGAM-S1	8 bits	Slope of 1st straight line at color gamma correction
55h	CGAM-S2	8 bits	Slope of 2nd straight line at color gamma correction
56h	CGAM-S3	8 bits	Slope of 3rd straight line at color gamma correction
57h	CGAM-S4	8 bits	Slope of 4th straight line at color gamma correction
58h	CGAM-S5	8 bits	Slope of 5th straight line at color gamma correction
59h	CGAM-S6	8 bits	Slope of 6th straight line at color gamma correction
5Ah	CGAM-S7	8 bits	Slope of 7th straight line at color gamma correction
5Bh	CGAM-S8	8 bits	Slope of 8th straight line at color gamma correction
5Ch	CGAM-S9	8 bits	Slope of 9th straight line at color gamma correction
5Dh	CGAM-S10	8 bits	Slope of 10th straight line at color gamma correction
60h	SETUP	6 bits	Set up level of luminance signal
61h	APT_HGA	5 bits	Horizontal aperture gain
62h	APT_HCL	7 bits	Coring level of horizontal aperture signal
63h	APT_VGA	5 bits	Vertical aperture gain
64h	APT_VCL	7 bits	Coring level of vertical aperture signal
65h			Not used
66h	VARI_MASK	4 bits	Position to erase color signal by luminance mask signal
67h	6ADV	4	1 : 6 clocks advance of luminance signal 0 : No variation
	8ADV	3	1 : 8 clocks advance of luminance signal 0 : No variation
	4DLY	2	1 : 4 clocks delay of luminance signal 0 : No variation
	2DLY	1	1 : 2 clocks delay of luminance signal 0 : No variation
	1DLY	0	1 : 1 clock delay of luminance signal 0 : No variation
68h	HVARI	2 bits	Position of horizontal aperture signal

ADDRESS	NAME	BIT	CONTENTS		
69h	Y_MUTE	3	Muting analog luminance signal output	0 : Normal	1 : Muting
	CBLK_OFF	2	CBLK availability for luminance signal	0 : ON	1 : OFF
	SEL_BLK	1	Pedestal level of luminance signal	0 : 16th step	1 : 0 step
	Y_NEGA	0	The polarity of luminance signal	0 : Normal	1 : Inverted
6Ah	Y_NESFT	8 bits	Base level of luminance signal		
6Bh	Y_NEAMP	8 bits	Luminance signal level		
6Ch	MASK_NE	8 bits	Masking level of luminance signal		
6Dh			Not used		
6Eh			Not used		
6Fh			Not used		
70h	CGAM-A1	8 bits	1st input range of color gamma correction		
71h	CGAM-A2	8 bits	2nd input range of color gamma correction		
72h	CGAM-A3	8 bits	3rd input range of color gamma correction		
73h	CGAM-A4	8 bits	4th input range of color gamma correction		
74h	CGAM-A5	8 bits	5th input range of color gamma correction		
75h	CGAM-A6	8 bits	6th input range of color gamma correction		
76h	CGAM-A7	8 bits	7th input range of color gamma correction		
77h	CGAM-A8	8 bits	8th input range of color gamma correction		
78h	CGAM-A9	8 bits	9th input range of color gamma correction		
79h	CGAM-P1	8 bits	Offset of 1st straight line at color gamma correction		
7Ah	CGAM-P2	8 bits	Offset of 2nd straight line at color gamma correction		
7Bh	CGAM-P3	8 bits	Offset of 3rd straight line at color gamma correction		
7Ch	CGAM-P4	8 bits	Offset of 4th straight line at color gamma correction		
7Dh	CGAM-P5	8 bits	Offset of 5th straight line at color gamma correction		
7Eh	CGAM-P6	8 bits	Offset of 6th straight line at color gamma correction		
7Fh	CGAM-P7	8 bits	Offset of 7th straight line at color gamma correction		
80h	CGAM-P8	8 bits	Offset of 8th straight line at color gamma correction		
81h	CGAM-P9	8 bits	Offset of 9th straight line at color gamma correction		
82h	CGAM-P10	8 bits	Offset of 10th straight line at color gamma correction		
83h	CGAM-F	1 bit	Polarity of color gamma correction	0 : +	1 : –
84h	CGAM-S1	8 bits	Slope of 1st straight line at color gamma correction		
85h	CGAM-S2	8 bits	Slope of 2nd straight line at color gamma correction		
86h	CGAM-S3	8 bits	Slope of 3rd straight line at color gamma correction		
87h	CGAM-S4	8 bits	Slope of 4th straight line at color gamma correction		
88h	CGAM-S5	8 bits	Slope of 5th straight line at color gamma correction		
89h	CGAM-S6	8 bits	Slope of 6th straight line at color gamma correction		
8Ah	CGAM-S7	8 bits	Slope of 7th straight line at color gamma correction		
8Bh	CGAM-S8	8 bits	Slope of 8th straight line at color gamma correction		
8Ch	CGAM-S9	8 bits	Slope of 9th straight line at color gamma correction		
8Dh	CGAM-S10	8 bits	Slope of 10th straight line at color gamma correction		
8Eh			Not used		

ADDRESS	NAME	BIT	CONTENTS
8Fh			Not used
A0h	SEL_WBD	7	The option of white balance data equation 0 : Accumulated data/Image area 1 : Accumulated data/Number of data
	PEAK4_8	6	The option to detect peak level to control the exposure 0 : Accumulated data of 4 pixels 1 : Accumulated data of 8 pixels
	PEAHA_H	5	The area in horizontal to detect peak level to control the exposure 0 : OFF 1 : ON
	PEAKA_V	4	The area in vertical to detect peak level to control the exposure 0 : OFF 1 : ON
	I_WBA_H	3	The area in horizontal to detect average level to control both the exposure and white balance 0 : OFF 1 : ON
	I_WBA_V	2	The area in vertical to detect average level to control both the exposure and white balance 0 : OFF 1 : ON
	MASK_H	1	Horizontal mask signal availability 0 : OFF 1 : ON
	MASK_V	0	Vertical mask signal availability 0 : OFF 1 : ON
A1h	HMSKF_U	2 bits	Upper 2 bits of starting point to mask in horizontal
A2h	HMSKF_L	8 bits	Lower 8 bits of starting point to mask in horizontal
A3h	HMSKR_U	2 bits	Upper 2 bits of ending point to mask in horizontal
A4h	HMSKR_L	8 bits	Lower 8 bits of ending point to mask in horizontal
A5h	VMSKF_U	1 bit	Upper 1 bit of starting point to mask in vertical
A7h	VMSKF_L	8 bits	Lower 8 bits of starting point to mask in vertical
A8h	VMSKR_U	1 bit	Upper 1 bit of ending point to mask in vertical
A9h	VMSKR_L	8 bits	Lower 8 bits of ending point to mask in vertical

OUTPUT DATA

Output Data Table

ADDRESS	NAME	BIT	CONTENTS
00 to 07h	IRIS-1-1 to 8	8 bits	Average data to control exposure
08 to 0Fh	IRIS-2-1 to 8	8 bits	Average data to control exposure
10 to 17h	IRIS-3-1 to 8	8 bits	Average data to control exposure
18 to 1Fh	IRIS-4-1 to 8	8 bits	Average data to control exposure
20 to 27h	IRIS-5-1 to 8	8 bits	Average data to control exposure
28 to 2Fh	IRIS-6-1 to 8	8 bits	Average data to control exposure
30 to 37h	IRIS-7-1 to 8	8 bits	Average data to control exposure
38 to 3Fh	IRIS-8-1 to 8	8 bits	Average data to control exposure
40 to 43h	AWBI-1-1 to 4	8 bits	Average data of I/R – Y axis to control auto white balance
44 to 47h	AWBI-2-1 to 4	8 bits	
48 to 4Bh	AWBI-3-1 to 4	8 bits	Average data of I/R – Y axis to control auto white balance
4C to 4Fh	AWBI-4-1 to 4	8 bits	
50 to 53h	AWBQ-1-1 to 4	8 bits	Average data of Q/B – Y axis to control auto white balance
54 to 57h	AWBQ-2-1 to 4	8 bits	
58 to 5Bh	AWBQ-3-1 to 4	8 bits	Average data of Q/B – Y axis to control auto white balance
5C to 5Fh	AWBQ-4-1 to 4	8 bits	
60h	H_PEAK	8 bits	Maximum luminance signal out of 64 blocks
61h	L_PEAK	8 bits	Minimum luminance signal out of 64 blocks
62h	OB_DATA	8 bits	Average data of optical pixels
63h	C1_OB_R	8 bits	Average data of optical pixels for Mg + Ye
64h	C3_OB_B	8 bits	Average data of optical pixels for Mg + Cy

Position of Each Output on Image Screen

(1) Luminance Signal Data to Control Exposure

Left-top Side of Image

IRIS-1-1	IRIS-1-2	IRIS-1-3	IRIS-1-4	IRIS-1-5	IRIS-1-6	IRIS-1-7	IRIS-1-8
IRIS-2-1	IRIS-2-2	IRIS-2-3	IRIS-2-4	IRIS-2-5	IRIS-2-6	IRIS-2-7	IRIS-2-8
IRIS-3-1	IRIS-3-2	IRIS-3-3	IRIS-3-4	IRIS-3-5	IRIS-3-6	IRIS-3-7	IRIS-3-8
IRIS-4-1	IRIS-4-2	IRIS-4-3	IRIS-4-4	IRIS-4-5	IRIS-4-6	IRIS-4-7	IRIS-4-8
IRIS-5-1	IRIS-5-2	IRIS-5-3	IRIS-5-4	IRIS-5-5	IRIS-5-6	IRIS-5-7	IRIS-5-8
IRIS-6-1	IRIS-6-2	IRIS-6-3	IRIS-6-4	IRIS-6-5	IRIS-6-6	IRIS-6-7	IRIS-6-8
IRIS-7-1	IRIS-7-2	IRIS-7-3	IRIS-7-4	IRIS-7-5	IRIS-7-6	IRIS-7-7	IRIS-7-8
IRIS-8-1	IRIS-8-2	IRIS-8-3	IRIS-8-4	IRIS-8-5	IRIS-8-6	IRIS-8-7	IRIS-8-8

(2) Color Signal Data to Control Auto White Balance

Left-top Side of Image

AWBI/AWBQ-1-1	AWBI/AWBQ-1-2	AWBI/AWBQ-1-2	AWBI/AWBQ-1-2
AWBI/AWBQ-2-1	AWBI/AWBQ-2-2	AWBI/AWBQ-2-2	AWBI/AWBQ-2-2
AWBI/AWBQ-3-1	AWBI/AWBQ-3-2	AWBI/AWBQ-3-2	AWBI/AWBQ-3-2
AWBI/AWBQ-4-1	AWBI/AWBQ-4-2	AWBI/AWBQ-4-2	AWBI/AWBQ-4-2

Either I or R − Y is selectable by address 28h.

Either Q or B − Y is selectable by address 28h.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power supply voltage	V_{DD}	−0.3 to +4.6	V
Input voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	−55 to +150	˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating temperature	T_{OPR}	−20	+25	+70	˚C
Input clock frequency	f_{CK}		28.6		MHz

ELECTRICAL CHARACTERISTICS

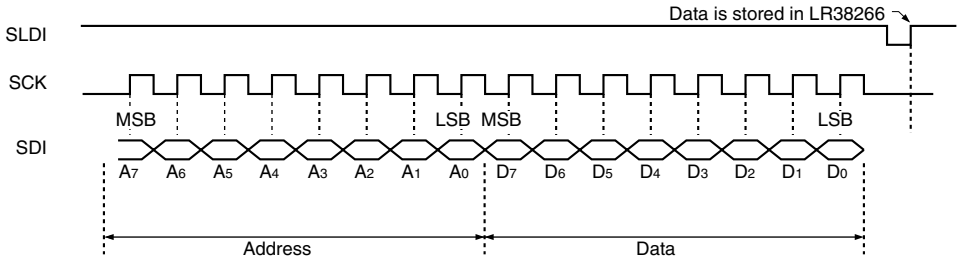
(V_{DD} = 3.3±0.33 V, T_{OPR} = −20 to +70 ˚C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}				0.2V_{DD}	V	1
Input "High" voltage	V_{IH}		0.8V_{DD}			V	
Input "Low" voltage	V_{T-}				0.2V_{DD}	V	2
Input "High" voltage	V_{T+}		0.8V_{DD}			V	
Hysteresis voltage	$V_{T+} - V_{T-}$		0.2			V	
Output "Low" voltage	V_{OL1}	I_{OL} = −1.6 mA			0.1V_{DD}	V	3
Output "High" voltage	V_{OH2}	I_{OH} = 0.8 mA	0.9V_{DD}			V	
Output leakage current	$\|I_{OZ}\|$	High-impedance	−1.0		1.0	µA	
Output "Low" voltage	V_{OL1}	I_{OL} = −1.6 mA			0.1V_{DD}	V	4
Output "High" voltage	V_{OH2}	I_{OH} = 0.8 mA	0.9V_{DD}			V	
Output leakage current	$\|I_{OZ}\|$	High-impedance	−1.0		1.0	µA	
Input "Low" current	$\|I_{IL1}\|$	V_{IN} = 0 V		10		µA	5
Input "High" current	$\|I_{IH2}\|$	V_{IN} = V_{DD}		10		µA	6
Output "Low" voltage	V_{OL1}	I_{OL} = −1.6 mA			0.1V_{DD}	V	7
Output "High" voltage	V_{OH2}	I_{OH} = 0.8 mA	0.9V_{DD}			V	
Resolution	RES			8		Bit	8
Linearity error	EL	V_{REF} = 1.0 V			±3.0	LSB	
Differential error	ED	R_{REF}= 4.8 kΩ			±1.0	LSB	
Full scale current	$\|I_{FS}\|$	R_{OUT} = 75 Ω		13		mA	
Reference voltage	V_{REF}			1.0		V	9
Reference resistance	R_{REF}			4.8		kΩ	10
Output load resistance	R_{OUT}			75		Ω	8

NOTES :

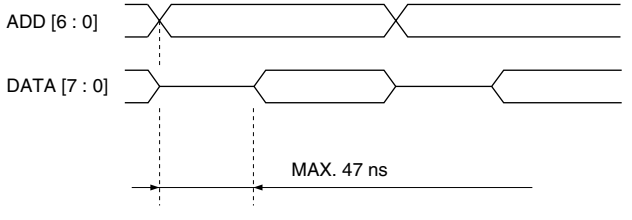
1. Applied to inputs (IC, ICD, ICU).
2. Applied to input (ICS).
3. Applied to output (TO).
4. Applied to output (XTO).
5. Applied to input (ICU).
6. Applied to input (ICD).
7. Applied to output (O).
8. Applied to outputs (YENCO, CENCO).
9. Applied to input (V_{REF}).
10. Applied to inputs (I_{REF1}, I_{REF2}).

Data Interface Timing



SCK should be slower than 20 MHz.

Data Input



Data output in 47 ns or more after address input is valid.

Data Output

DETAIL EXPLANATION

CCD

CCD type out of 270 k, 320 k, 410 k and 470 k pixels is selected by address 01h.

Output Signal Format

(1) Analog Video Signal Output

Built-in DA converters output luminance (Y) signal without CSYNC and modulated color signal of NTSC or PAL.

Standby mode of DA converter makes DA output pins high impedance.

(2) Digital Video Signal Output (address 01h)

One out of three formats below is selectable by address 01h. High level of pin 74 as DOC makes all digital output pins high impedance.

1. 8-bit Y and 8-bit C
2. 8-bit Y and 8-bit U/V
3. 8-bit U/Y/V/Y

Camera Control Data Output

(1) Exposure Control Data Output (64 data with 8 bits and 2 data with 8 bits)

The user-defined image area consists of 64 blocks divided into 8 x 8 blocks. Each average luminance level is output to DATA output pins by setting ADD input pins.

In the defined area, the maximum luminance level and the minimum luminance level are output to DATA output pins.

(2) White Balance Control Data Output (two kinds of 16 data with 8 bits)

The user-defined image area consists of 16 blocks divided into 4 x 4 blocks. Average color signal levels of either both I and Q or both R – Y and B – Y are output to DATA output pins by setting ADD input pins.

(3) Black Balance Control Data Output (3 data with 8 bits)

Three kinds of outputs below are at DATA output pins.

- An average signal of CCD optical black portion consisting of 4 pixels per horizontal line for 128 horizontal lines located in the image center.
- An average signal of CCD optical black portion consisting of 2 pixels per horizontal line for 128 horizontal lines located in the image center, which is available to tune the base level of Mg + Ye color signal component.
- An average signal of CCD optical black portion consisting of 2 pixels per horizontal line for 128 horizontal lines located in the image center, which is available to tune the base level of Mg + Cy color signal component.

Camera Signal Processing

(1) Optical Black Signal Clamping

The optical black signal portion is clamped so as to be 64h by using the average level of the input digital signal. The averaging is done for every field.

(2) Horizontal Period Delay Line

There are two horizontal delay lines in this IC for camera signal processing.

(3) Digital Filter for Luminance Signal

These are low-pass filters to make a Y signal from the color CCD signal.

(4) Gamma Correction for Luminance Signal

10-bit input signal is converted into an 8-bit signal with a gamma curve defined by 10 straight lines. Slope and position of every straight line can be set by address.

(5) Edge Enhancement of Luminance Signal

After gamma correction, the edge of the luminance signal is enhanced in both horizontal and vertical. How to enhance is tunable by address.

(6) Set-up Level of Luminance Signal
The set-up level is tunable by address.

(7) Polarity Option and Level Tuning of Luminance Signal
The polarity of the input signal from the AD converter can be inverted before filtering.
The DC offset level and the amplitude are tunable by address.

(8) Masking Luminance Signal
The restricted area in the whole image can be set by address.
The exposure function and the auto white balance function can be used only in the restricted area.

(9) Extract of Color Signal Component
Color signal components are extracted by following processing calculation.
$Red = (Mg + Ye) - K_1 (G + Cy)$
$Blue = (Mg + Cy) - K_2 (G + Ye)$
$YL = ((Mg + Ye) + (G + Cy) + (Mg + Cy) + (G + Ye))/4$
K_1 and K_2 are variable by address.

(10) Digital Filter of Color Signal Component
Red, blue and YL are passed to limit each bandwidth so as to be half of extracted signals by low-pass filters.

(11) Black Level Clamping of Color Signal Component
The black level of red and blue signals can be tuned by address 15h, 16h, 17h, and 18h.

(12) White Balance
The amplitude of red and blue signals can be tuned by address 19h, 1Ah, 1Bh, and 1Ch for white balance situation.

(13) Color Gamma Correction
10-bit input signal of red, blue and YL signals are converted into an 8-bit signal with gamma curve defined by 10 straight lines.
The slope and position of every straight line can be set by address.

(14) Color Matrix Correction
Color rendition can be tuned by address 1Dh and 1Eh under below equation.
$R - Y = (R - Y) + K_1 (B - Y)$
$B - Y = (B - Y) + K_2 (R - Y)$

(15) Color Level Adjustment
The amplitude of R – Y and B – Y can be tuned by address 1Fh and 20h.

(16) Color Level Suppression
A false color signal at both the transient portion of luminance signal and the high-light portion of luminance signal can be suppressed by address 2Bh, 2Ch, 2Dh, 2Eh, 30h, 31h, 32h, 33h, 34h and 35h.

(17) Polarity Option and Level Tuning of Color Signal
The polarity of the color component signal can be inverted before gamma correction.
The DC offset level and the amplitude are tunable by address 36h, 37h, 38h and 39h.

(18) NTSC/PAL Color Signal Encoder
R – Y and B – Y color signals are modulated under NTSC or PAL format.
Modulated clock frequency and TV format are selected by address 03h, 21h, 22h and 23h.
Line-lock system requires the clock generator outside LR38266.

(19) Accumulator to Control Exposure
Three kinds of output data below become available by address A0h, 00h to 3Fh, 60h and 61h.
- Average signal in either the whole image or restricted area.
- Maximum signal in either the whole image or restricted area.
- Minimum signal in either the whole image or restricted area.

(20) Accumulator to Control White Balance

Output data below become available by address 24h, 25h, 26h, 27h, 28h, 29h, 2Ah, A0h and 4Fh to 5Fh.

Average signal of I (R – Y) and Q (B – Y) in 16 areas of the whole image.

These data can be weighted by both the color zone of I-axis and/or Q-axis and the range of luminance.

(21) Accumulator to Control Color Black Balance

Average signal of the optical black portion to clamp the black level of color signal is available by address 62h, 63h and 64h.

(22) Others

- The output timing of synchronous signals are available by address 06h, 07h and 08h.
- Functions like standby, muting, etc. are available by address 01h, 03h, 04h and 21h.

PACKAGE

(Unit : mm)

100 LQFP (LQFP100-P-1414)