L29C818
8-bit Serial Scan Shadow Register

FEATURES

- Octal Register with Additional 8-bit Shiftable Shadow Register
- Serial Load / Verify of Writable Control Store RAM
- Serial Stimulus / Observation of Sequential Logic
- High-Speed, Low Power CMOS Technology
- Replaces AMD Am29818
- DECC SMD No. 5962-90515
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C818** is a high-speed octal register designed especially for applications using serial-scan diagnostics or writable control store. It is pin and functionally compatible with the AMD Am29818 bipolar device.

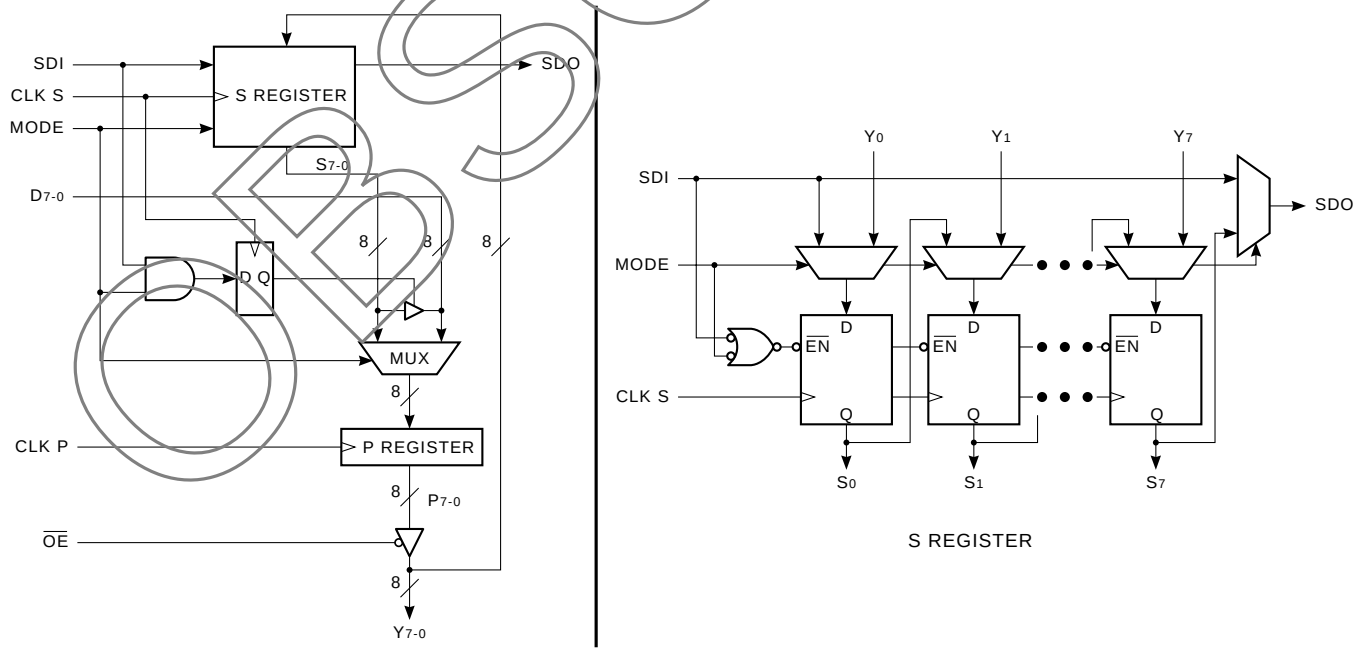
The L29C818 consists of an octal register, the P register, internally connected to an 8-bit shift register, the S register. Each has its own corresponding clock pin and the P register has a three-state output control.

An input control signal, MODE, in combination with the S register serial data input (SDI) pin controls data routing within the L29C818. When the MODE input is LOW, indicating normal operation, data present on the D_{7-0} pins is loaded into the P register on the rising edge of CLK P. The contents of the P register are visible on the output pins Y_{7-0} when the $\overline{OE}$ control line is LOW.

Also, data present on the SDI pin is loaded into the least significant position of the S register on the rising edge of CLK S. In this mode, the S register performs a right-shift operation with the contents of each bit position replaced by the value in the next least significant location. The value in S_7 is shifted out on the serial data output (SDO) pin. The SDI and SDO pins allow serial connection of multiple L29C818 devices into a diagnostic loop. When MODE is LOW, the operation of the P and S registers are completely independent and no timing relationship is enforced between CLK P and CLK S.

When MODE is HIGH, the internal multiplexers route data between the S and P registers and the Y port. The contents of the S register are loaded into the P register on the rising edge of

L29C818 BLOCK DIAGRAM



CLK P. In diagnostic applications, this allows a data value input via serial scan to be loaded into the active data path of the machine.

When the MODE pin is HIGH, CLK S causes a parallel, rather than serial, load of the S register. In this mode, the S register is loaded from the Y_{7-0} pins at the rising edge of CLK S. This is useful in writable control store applications for read-back of the control store via the serial path.

When MODE is HIGH, the SDI pin is used as a control input to enable or disable the loading of the S register. It also affects routing of the S register contents onto the D_{7-0} outputs. When SDI is LOW, the S register is enabled for loading as above. When SDI is HIGH however, CLK S is prevented from reaching the S register and no load occurs. In order to allow the SDI pin to serve as an enable signal for all L29C818 devices in a serial configuration, special handling of the SDI input is required. When MODE is HIGH, the SDI input drives the SDO output directly, bypassing the S register. This means that the SDI value will apply simultaneously to all L29C818s in a serial loop. However, to ensure proper operation of a given device, the user must ensure that the SDI setup time to CLK S is extended by the sum of the SDI to SDO delays of all previous devices in the serial path.

The D_{7-0} port is normally used as the input port to the D register. For writable control store applications however, this port is connected to the I/O pins of the RAM used as a control store. In order to load this RAM through the serial path, it is necessary to drive the S register contents onto the D_{7-0} pins. This is accomplished when MODE and SDI are HIGH and a CLK S rising edge occurs. Note from above that with SDI HIGH, no loading of the S register occurs. However, a flip-flop is set which synchronously enables the D port output buffer. The D output remains enabled until the first rising edge of CLK S during which either SDI or MODE is LOW. Thus to load a control store RAM, data would be shifted in with MODE LOW. When an entire control store word is present in the serial S registers, the SDI and MODE pins are brought HIGH for one or more cycles, preventing further shifting of the S registers and enabling the contents onto the D port for writing into the RAM.

To verify the contents of a control store RAM, the RAM is read into the D register in the normal fashion. Then, the D contents are transferred in parallel to the S register by driving MODE HIGH with SDI LOW. The S register contents are then scanned out serially by returning MODE LOW and applying CLK S pulses.

TABLE 1. FUNCTION TABLE

Inputs				Outputs		Action		
MODE	SDI	CLK S	CLK P	P REG	S REG	Y_{7-0}	D_{7-0}	SDO
0	X	↑	X	N/A	SHIFT	Normal	HI-Z	S_7
0	X	X	↑	LOAD D	N/A	Normal	Input	S_7
1	0	↑	X	N/A	LOAD Y	Input*	HI-Z	SDI
1	1	↑	X	N/A	HOLD	Normal	Output	SDI
1	X	X	↑	LOAD S	N/A	Normal	HI-Z	SDI

*If $\overline{OE}$ is LOW, the P register value will be loaded into the S register. If $\overline{OE}$ is HIGH, a value may be applied externally to the Y_{7-0} pins.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –12.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 24.0 mA			0.5	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±20	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±20	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)		10	15	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — NORMAL REGISTER OPERATION

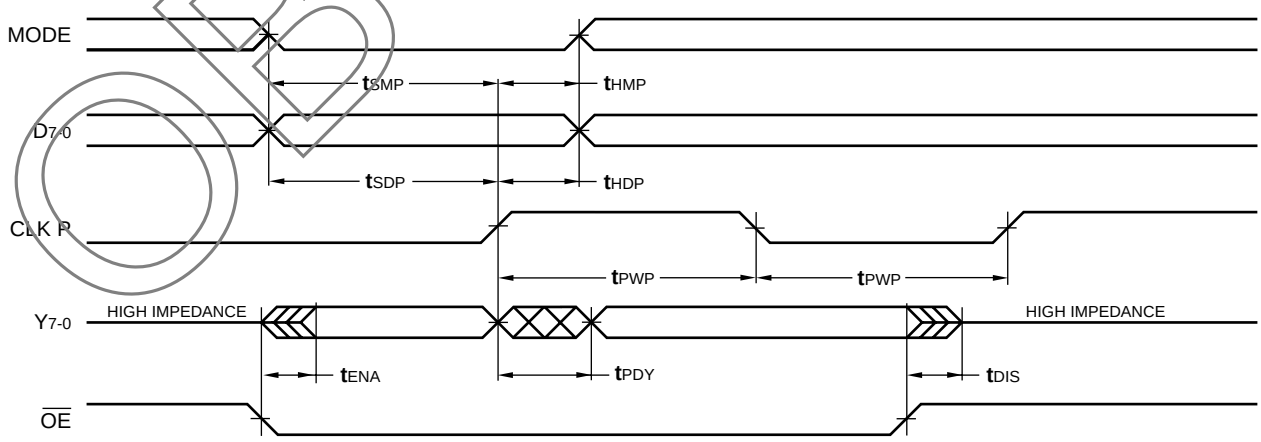
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–25 Min	L29C818–25 Max
t_{PWP}	CLK P Pulse Width	15	
t_{PDY}	CLK P to Y_{7-0}		13
t_{SDP}	D_{7-0} to CLK P Setup Time	8	
t_{HDP}	CLK P to D_{7-0} Hold Time	2	
t_{SMP}	MODE to CLK P Setup Time	15	
t_{HMP}	CLK P to MODE Hold Time	2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–30 Min	L29C818–30 Max
t_{PWP}	CLK P Pulse Width	15	
t_{PDY}	CLK P to Y_{7-0}		18
t_{SDP}	D_{7-0} to CLK P Setup Time	10	
t_{HDP}	CLK P to D_{7-0} Hold Time	2	
t_{SMP}	MODE to CLK P Setup Time	15	
t_{HMP}	CLK P to MODE Hold Time	2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		20

SWITCHING WAVEFORMS — NORMAL REGISTER OPERATION



SWITCHING CHARACTERISTICS — SERIAL SHIFT OPERATION

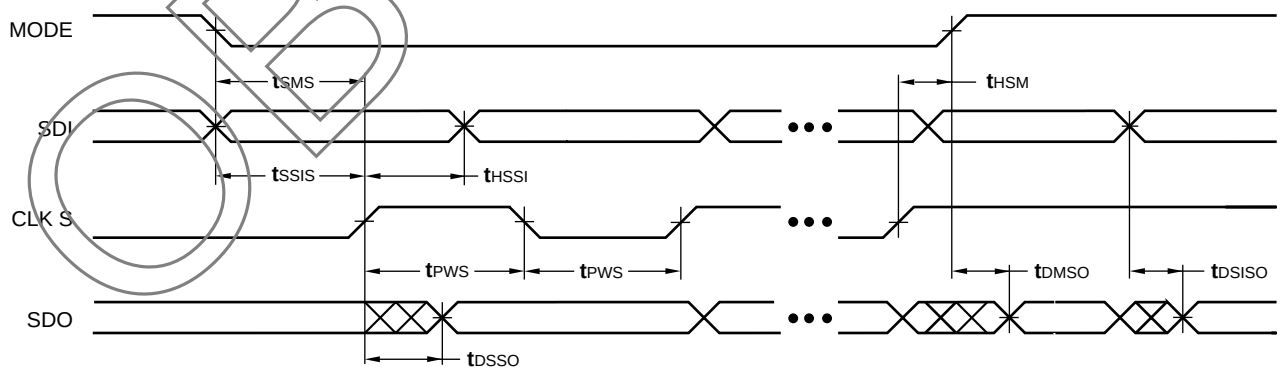
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–25 Min	L29C818–25 Max
t_{PWS}	CLK S Pulse Width	25	
t_{DSSO}	CLK S to SDO		25
t_{SSIS}	SDI to CLK S Setup Time	10	
t_{HSSI}	CLK S to SDI Hold Time	0	
t_{SMS}	MODE to CLK S Setup Time	12	
t_{HSM}	CLK S to MODE Hold Time	2	
t_{DMSO}	MODE to SDO	16	
t_{DSISO}	SDI to SDO	16	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–30 Min	L29C818–30 Max
t_{PWS}	CLK S Pulse Width	25	
t_{DSSO}	CLK S to SDO		30
t_{SSIS}	SDI to CLK S Setup Time	12	
t_{HSSI}	CLK S to SDI Hold Time	0	
t_{SMS}	MODE to CLK S Setup Time	12	
t_{HSM}	CLK S to MODE Hold Time	5	
t_{DMSO}	MODE to SDO	18	
t_{DSISO}	SDI to SDO	18	

SWITCHING WAVEFORMS — SERIAL SHIFT OPERATION



SWITCHING CHARACTERISTICS — PIPELINE LOAD FROM SHADOW

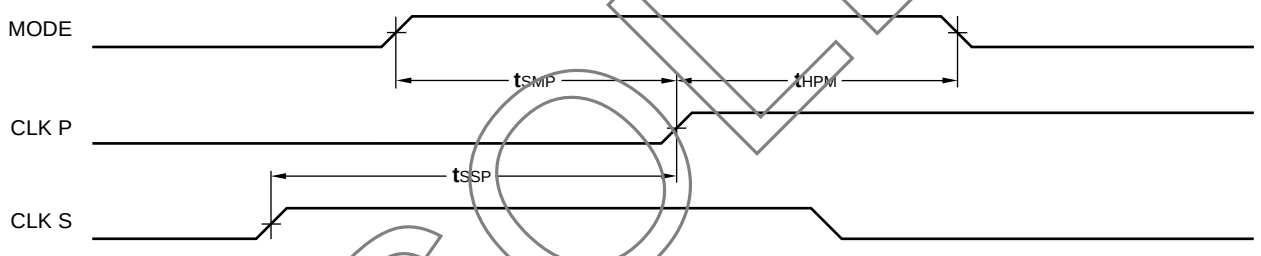
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–25 Min	L29C818–25 Max
t_{SMP}	MODE to CLK P	15	
t_{HPM}	CLK P to MODE Hold Time	2	
t_{SSP}	CLK S to CLK P	10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–30 Min	L29C818–30 Max
t_{SMP}	MODE to CLK P	15	
t_{HPM}	CLK P to MODE Hold Time	2	
t_{SSP}	CLK S to CLK P	15	

SWITCHING WAVEFORMS — PIPELINE LOAD FROM SHADOW



SWITCHING CHARACTERISTICS — SHADOW LOAD FROM Y PORT

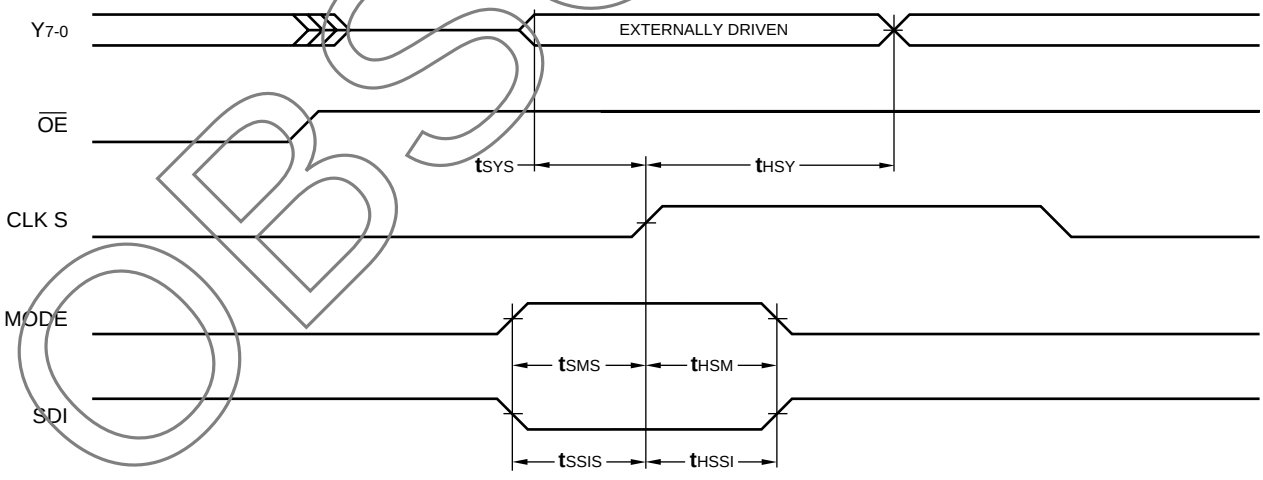
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–25 Min	L29C818–25 Max
t_{SYS}	Y_{7-0} to CLK S Setup Time	5	
t_{HSY}	CLK S to Y_{7-0} Hold Time	5	
t_{SMS}	MODE to CLK S Setup Time	12	
t_{HSM}	CLK S to MODE Hold Time	2	
t_{SSIS}	SDI to CLK S Setup Time	10	
t_{HSSI}	CLK S to SDI Hold Time	0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–30 Min	L29C818–30 Max
t_{SYS}	Y_{7-0} to CLK S Setup Time	8	
t_{HSY}	CLK S to Y_{7-0} Hold Time	5	
t_{SMS}	MODE to CLK S Setup Time	12	
t_{HSM}	CLK S to MODE Hold Time	5	
t_{SSIS}	SDI to CLK S Setup Time	12	
t_{HSSI}	CLK S to SDI Hold Time	0	

SWITCHING WAVEFORMS — SHADOW LOAD FROM Y PORT



SWITCHING CHARACTERISTICS — SHADOW READ VIA D PORT

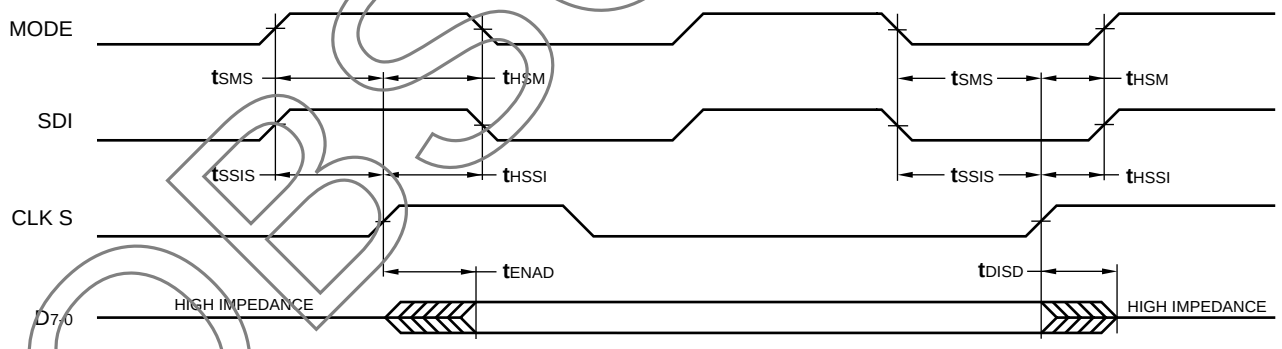
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–25 Min	L29C818–25 Max
t_{SMS}	MODE to CLK S Setup Time	12	
t_{HSM}	CLK S to MODE Hold Time	2	
t_{SSIS}	SDI to CLK S Setup Time	10	
t_{HSSI}	CLK S to SDI Hold Time	0	
t_{ENAD}	CLK S to D_{7-0} Enable Delay (Note 11)	85	
t_{DISD}	CLK S to D_{7-0} Disable Delay (Note 11)	30	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818–30 Min	L29C818–30 Max
t_{SMS}	MODE to CLK S Setup Time	12	
t_{HSM}	CLK S to MODE Hold Time	5	
t_{SSIS}	SDI to CLK S Setup Time	12	
t_{HSSI}	CLK S to SDI Hold Time	0	
t_{ENAD}	CLK S to D_{7-0} Enable Delay (Note 11)	90	
t_{DISD}	CLK S to D_{7-0} Disable Delay (Note 11)	35	

SWITCHING WAVEFORMS — SHADOW READ VIA D PORT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above **V**CC will be clamped beginning at –0.6 V and **V**CC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the **t**ENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the **t**DIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

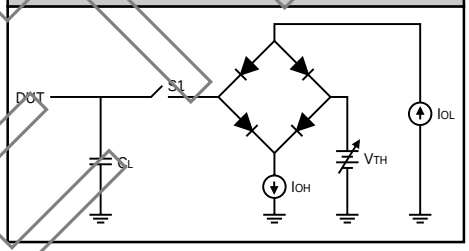
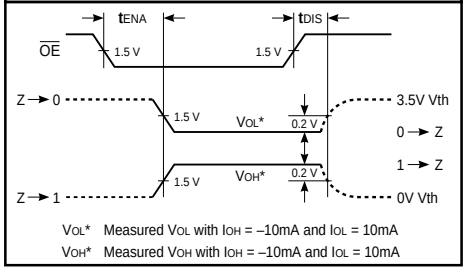
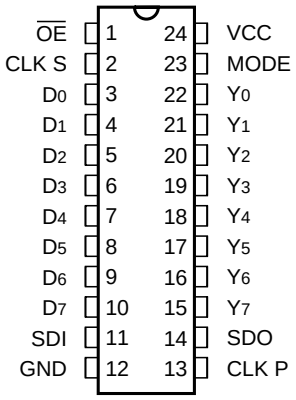


FIGURE B. THRESHOLD LEVELS

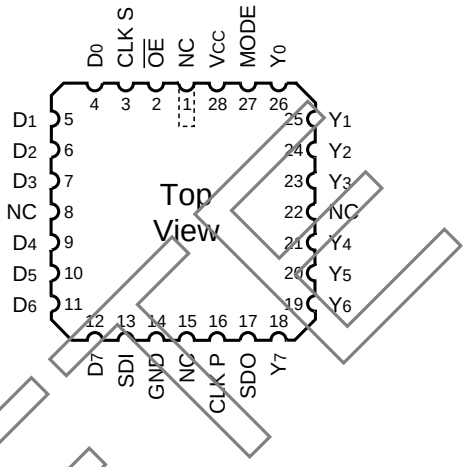


ORDERING INFORMATION

24-pin — 0.3" wide



28-pin



Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — COMMERCIAL SCREENING		
25 ns	L29C818PC25		
	–55°C to +125°C — COMMERCIAL SCREENING		
30 ns			
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
		L29C818DMB30	L29C818KMB30