LTC1644

CompactPCI Bus Hot Swap Controller

August 2001

FEATURES

- **Allows Safe Board Insertion and Removal from a Live, CompactPCI™ Bus**
- **Controls –12V, 3.3V, 5V and 12V Supplies**
- **Programmable Foldback Current Limit with Circuit Breaker**
- **Dual-Level Circuit Breakers Protect 5V and 3.3V Supplies from Overcurrent and Short-Circuit Faults**
- **LOCAL_PCI_RST# Logic On-Chip**
- **PRECHARGE Output Biases I/O Pins During Card Insertion and Extraction**
- User Programmable Supply Voltage Power-Up Rate

APPLICATIONS

- Hot Board Insertion into CompactPCI Bus

DESCRIPTION

The LTC®1644 is a Hot Swap™ controller that allows a board to be safely inserted and removed from a CompactPCI bus slot. External N-channel transistors control the 3.3V/5V supplies, while on-chip switches control the –12V and 12V supplies. The 3.3V and 5V supplies can be ramped up at a programmable rate. Electronic circuit breakers protect all four supplies against overcurrent faults. The $\overline{\text{PWRGD}}$ output indicates when all of the supply voltages are within tolerance. The OFF/$\overline{\text{ON}}$ pin is used to cycle the board power or reset the circuit breaker. The PRECHARGE output can be used to bias the bus I/O pins during card insertion and extraction. PCI_RST# is combined on-chip with HEALTHY# in order to generate LOCAL_PCI_RST#.

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CompactPCI is a trademark of the PCI Industrial Computer Manufacturers Group.

TYPICAL APPLICATION

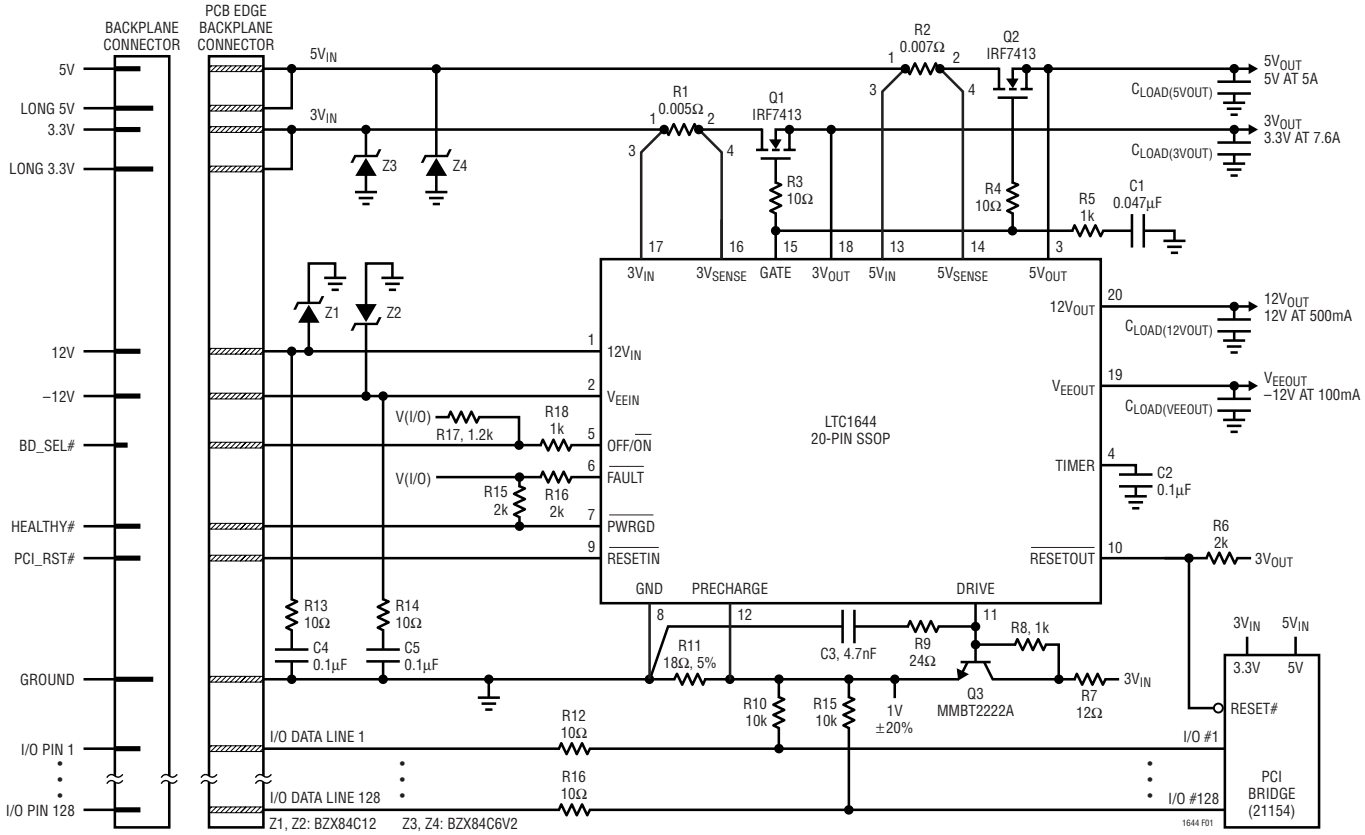


Figure 1

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- $12V_{IN}$ 14V
- V_{EEIN} ..... –14V

Input Voltages (Pins 5, 9) ..... –0.3V to ($12V_{IN}$ + 0.3V)

Output Voltages (Pins 6, 7, 10) –0.3V to ($12V_{IN}$ + 0.3V)

Analog Voltages
- Pins 3, 4, 11 to 18 ..... –0.3V to ($12V_{IN}$ + 0.3V)
- V_{EEOUT} ..... –14V to 0.3V
- $12V_{OUT}$ ..... –0.3V to 14V

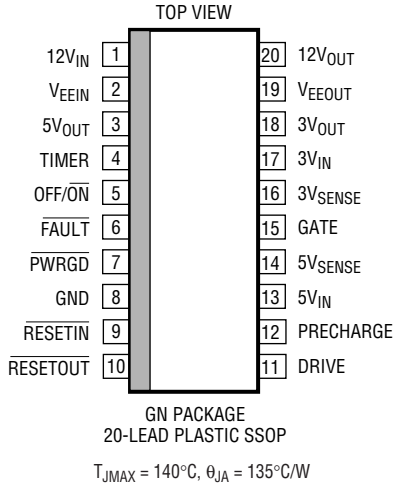
All Other Pins ..... –0.3V to ($12V_{IN}$ + 0.3V)

Operating Temperature Range
- LTC1644C ..... 0°C to 70°C
- LTC1644I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1644CGN
LTC1644IGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{EE} = –12V, V_{3VIN} = 3.3V, V_{5VIN} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD}	V_{12VIN} Supply Current	OFF/$\overline{ON}$ = 0V	●		4	8	mA
V_{LKO}	Undervoltage Lockout	$12V_{IN}$	●	6.00	9.00	10.80	V
		$3V_{IN}$, $5V_{IN}$	●	2.25	2.50	2.75	V
V_{FB}	Foldback Current Limit Voltage	V_{FB} = (V_{5VIN} – $V_{5VSENSE}$), V_{5VOUT} = 0V, TIMER = 0V	●	8	11	15	mV
		V_{FB} = (V_{5VIN} – $V_{5VSENSE}$), V_{5VOUT} = 3V, TIMER = 0V	●	40	55	70	mV
		V_{FB} = (V_{3VIN} – $V_{3VSENSE}$), V_{3VOUT} = 0V, TIMER = 0V	●	8	11	15	mV
		V_{FB} = (V_{3VIN} – $V_{3VSENSE}$), V_{3VOUT} = 2V, TIMER = 0V	●	40	55	70	mV
V_{CB}	Circuit Breaker Trip Voltage	V_{CB} = (V_{5VIN} – $V_{5VSENSE}$), TIMER = FLOAT	●	40	55	70	mV
		V_{CB} = (V_{3VIN} – $V_{3VSENSE}$), TIMER = FLOAT	●	40	55	70	mV
t_{OC}	Overcurrent Fault Response Time	(V_{5VIN} – $V_{5VSENSE}$) = 100mV, TIMER = FLOAT	●	10	30	50	µs
		(V_{3VIN} – $V_{3VSENSE}$) = 100mV, TIMER = FLOAT	●	10	30	50	µs
t_{SC}	Short-Circuit Response Time	(V_{5VIN} – $V_{5VSENSE}$) = 200mV, TIMER = FLOAT	●		0.5	1.0	µs
		(V_{3VIN} – $V_{3VSENSE}$) = 200mV, TIMER = FLOAT	●		0.5	1.0	µs
I_{CP}	GATE Pin Output Current	OFF/$\overline{ON}$ = 0V, V_{GATE} = 0V, TIMER = 0V	●	–20	–50	–100	µA
		V_{GATE} = 5V, OFF/$\overline{ON}$ = 4V		100	200	300	µA
		OFF/$\overline{ON}$ = 0V, V_{GATE} = 2V, TIMER = FLOAT, $\overline{FAULT}$ = 0V	●	3	10	20	mA
ΔV_{GATE}	External Gate Voltage	ΔV_{GATE} = (V_{12VIN} – V_{GATE}), I_{GATE} = –1µA	●		100	200	mV
V_{DROP}	Internal Switch Voltage Drop	V_{DROP} = (V_{12VIN} – V_{12VOUT}), I = 500mA	●		225	600	mV
		V_{DROP} = (V_{EEOUT} – V_{EEIN}), I_{EE} = 100mA	●		100	250	mV
I_{CL}	Current Foldback	$12V_{IN}$ = 12V, $12V_{OUT}$ = 0V, TIMER = 0V	●	–500	–250	–50	mA
		$12V_{IN}$ = 12V, $12V_{OUT}$ = 11V, TIMER = 0V	●	–1500	–850	–450	mA
		V_{EEIN} = –12V, V_{EEOUT} = 0V, TIMER = 0V	●	20	160	215	mA
		V_{EEIN} = –12V, V_{EEOUT} = –11V, TIMER = 0V	●	200	450	650	mA
T_{TS}	Thermal Shutdown Temperature				130		°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{EE} = –12V, V_{3VIN} = 3.3V, V_{5VIN} = 5V unless otherwise noted.

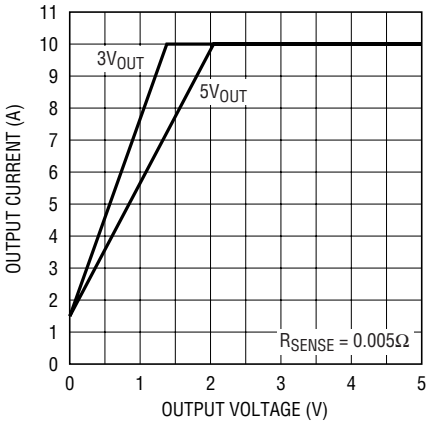
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Power Good Threshold Voltage	$12V_{OUT}$	●	10.8	11.1	11.4	V
		V_{EEOUT}	●	–10.4	–10.5	–11.1	V
		$3V_{OUT}$	●	2.8	2.9	3.0	V
		$5V_{OUT}$	●	4.50	4.65	4.75	V
V_{3VONLY}	3V Only Window Voltage	$V_{3VONLY} = \lvert V_{5VIN} - V_{3VIN} \rvert$, $V_{5VOUT} = V_{3VOUT} = 3V$	●	70	100	150	mV
$V_{NOVEEIN}$	No V_{EEIN} Threshold Voltage	V_{EEIN}	●	–6.3	–4.65	–4	V
V_{IL}	Input Low Voltage	OFF/$\overline{ON}$, $\overline{RESETIN}$, $\overline{FAULT}$	●			0.8	V
V_{IH}	Input High Voltage	OFF/$\overline{ON}$, $\overline{RESETIN}$, $\overline{FAULT}$	●	2			V
I_{IN}	OFF/$\overline{ON}$, $\overline{RESETIN}$ Input Current	OFF/$\overline{ON}$, $\overline{RESETIN}$ = 0V	●		±0.08	±10	µA
		OFF/$\overline{ON}$, $\overline{RESETIN}$ = $12V_{IN}$	●		±0.08	±10	µA
	$\overline{RESETOUT}$, $\overline{FAULT}$ Output Current	$\overline{RESETOUT}$, $\overline{FAULT}$ = 5V, OFF/$\overline{ON}$ = 0V, $\overline{RESETIN}$ = 3.3V	●		±0.08	±10	µA
	$\overline{PWRGD}$ Output Current	$\overline{PWRGD}$ = 5V, OFF/$\overline{ON}$ = 4V	●		±0.08	±10	µA
	$5V_{SENSE}$ Input Current	$5V_{SENSE}$ = 5V, $5V_{OUT}$ = 0V	●		50	100	µA
	$3V_{SENSE}$ Input Current	$3V_{SENSE}$ = 3.3V, $3V_{OUT}$ = 0V	●		50	100	µA
	$5V_{IN}$ Input Current	$5V_{IN}$ = 5V, TIMER = 0V	●		1	1.5	mA
	$3V_{IN}$ Input Current	$3V_{IN}$ = 3.3V, TIMER = FLOAT	●		450	625	µA
		$3V_{IN}$ = 3.3V, TIMER = 0V	●		350	550	µA
	$5V_{OUT}$ Input Current	$5V_{OUT}$ = 5V, OFF/$\overline{ON}$ = 0V, TIMER = 0V	●		225	400	µA
	$3V_{OUT}$ Input Current	$3V_{OUT}$ = 3.3V, OFF/$\overline{ON}$ = 0V, TIMER = 0V	●		375	500	µA
I_{TIMER}	TIMER Pin Current	OFF/$\overline{ON}$ = 0V, V_{TIMER} = 0V	●	–15	–20	–27	µA
		V_{TIMER} = 5V, OFF/$\overline{ON}$ = 4V	●	30	45	70	mA
V_{TIMER}	TIMER Threshold Voltages	(V_{12VIN} – V_{TIMER}), $\overline{FAULT}$ = 0V	●	0.2	0.4	1.3	V
R_{DIS}	$5V_{OUT}$ Discharge Impedance	OFF/$\overline{ON}$ = 4V	●		50	100	Ω
	$3V_{OUT}$ Discharge Impedance	OFF/$\overline{ON}$ = 4V	●		50	100	Ω
	$12V_{OUT}$ Discharge Impedance	OFF/$\overline{ON}$ = 4V	●		430	1000	Ω
	V_{EEOUT} Discharge Impedance	OFF/$\overline{ON}$ = 4V	●		625	1000	Ω
V_{OL}	Output Low Voltage	$\overline{PWRGD}$, $\overline{RESETOUT}$, $\overline{FAULT}$, I = 3mA	●		0.2	0.4	V
V_{PXG}	PRECHARGE Reference Voltage	V_{5VIN} = 5V	●	0.95	1.00	1.05	V
		V_{5VIN} = V_{3VIN} = 3.3V	●	0.95	1.00	1.05	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

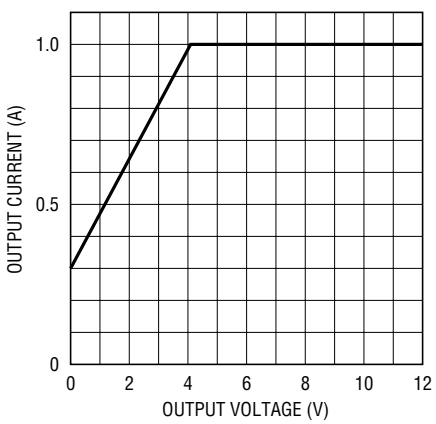
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS

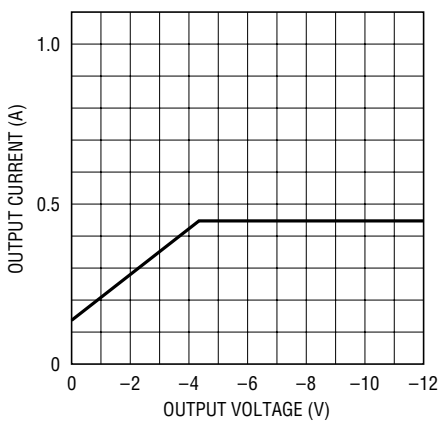
3.3V and 5V Current Foldback Profile



12V Current Foldback Profile

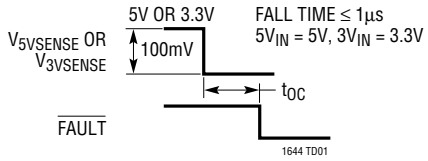


–12V Current Foldback Profile

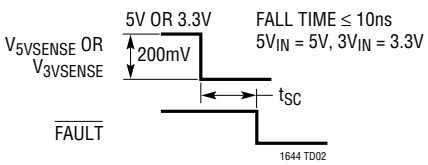


TIMING DIAGRAMS

t_{OC} Overcurrent Fault Detect



t_{SC} Short-Circuit Fault Detect



PIN FUNCTIONS

$12V_{IN}$ (Pin 1): 12V Supply Input. A 0.5Ω switch is connected between $12V_{IN}$ and $12V_{OUT}$ with a foldback current limit. An undervoltage lockout circuit prevents the switches from turning on while the $12V_{IN}$ pin voltage is less than 9V. $12V_{IN}$ also provides power to the LTC1644's internal circuitry.

V_{EEIN} (Pin 2): –12V Supply Input. A 1Ω switch is connected between V_{EEIN} and V_{EEOUT} with a foldback current limit. If no V_{EE} supply input is available, tie the V_{EEIN} pin to the GND pin in order to disable the V_{EEOUT} power good function.

$5V_{OUT}$ (Pin 3): 5V Output Sense. The $\overline{PWRGD}$ pin will not pull low until the $5V_{OUT}$ pin voltage exceeds 4.65V. If no 5V input supply is available, tie the $5V_{OUT}$ pin to the $3V_{OUT}$ pin in order to disable the $5V_{OUT}$ power good function.

TIMER (Pin 4): Current Fault Inhibit Timing Input. Connect a capacitor from TIMER to GND. With the chip turned off (OFF/$\overline{ON}$ = HIGH), the TIMER pin is internally held at GND. When the chip is turned on, a 20µA pull-up current source is connected to TIMER. Current limit faults will be ignored until the voltage at the TIMER pin rises to within 0.4V of $12V_{IN}$.

OFF/$\overline{ON}$ (Pin 5): Digital Input. Connect the CPCI BD_SEL# signal to the OFF/$\overline{ON}$ pin. When the OFF/$\overline{ON}$ pin is pulled low, the GATE pin is pulled high by a 50µA current source and the internal 12V and –12V switches are turned on. When the OFF/$\overline{ON}$ pin is pulled high, the GATE pin will be pulled to ground by a 200µA current source and the 12V and –12V switches turn off.

PIN FUNCTIONS

The OFF/$\overline{ON}$ pin is also used to reset the electronic circuit breaker. If the OFF/$\overline{ON}$ pin is cycled high and low following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur.

$\overline{FAULT}$ (Pin 6): Open-Drain Digital I/O. $\overline{FAULT}$ is pulled low when a current limit fault is detected. Current limit faults are ignored until the voltage at the TIMER pin is within 0.9V of $12V_{IN}$. Once the TIMER cycle is complete, $\overline{FAULT}$ will pull low and the chip latches off in the event of an overcurrent fault. The chip will remain latched in the off state until the OFF/$\overline{ON}$ pin is cycled high then low.

Forcing the $\overline{FAULT}$ pin low with an external pull-down will cause the chip to be latched into the off state after a 30µs deglitching time.

$\overline{PWRGD}$ (Pin 7): Open-Drain Digital Power Good Output. Connect the CPCI HEALTHY# signal to the $\overline{PWRGD}$ pin. $\overline{PWRGD}$ remains low while $V_{12VOUT} \geq 11.1V$, $V_{3VOUT} \geq 2.9V$, $V_{5VOUT} \geq 4.65V$ and $V_{EEOUT} \leq -10.5V$. When any of the supplies falls below its power good threshold voltage, $\overline{PWRGD}$ will go high after a 10µs deglitching time.

GND (Pin 8): Chip Ground.

$\overline{RESETIN}$ (Pin 9): Digital Input. Connect the CPCI PCI_RST# signal to the $\overline{RESETIN}$ pin. Pulling $\overline{RESETIN}$ low will cause $\overline{RESETOUT}$ to pull low.

$\overline{RESETOUT}$ (Pin 10): Open-Drain Digital Output. Connect the CPCI LOCAL_PCI_RST# signal to the $\overline{RESETOUT}$ pin. $\overline{RESETOUT}$ is the logical combination of $\overline{RESETIN}$ and $\overline{PWRGD}$.

DRIVE (Pin 11): Precharge Base Drive Output. Provides base drive for an external NPN emitter-follower which in turn biases the PRECHARGE node.

PRECHARGE (Pin 12): Precharge Monitor Input. An on-chip error amplifier servos the DRIVE pin voltage to keep the precharge node at 1V (see Figure 8).

$5V_{IN}$ (Pin 13): 5V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the $5V_{IN}$ pin is less than 2.5V. If no 5V input supply is available, tie the $5V_{IN}$ to the $3V_{IN}$ pin.

$5V_{SENSE}$ (Pin 14): 5V Current Limit Sense. With a sense resistor placed in the supply path between $5V_{IN}$ and $5V_{SENSE}$, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch while the TIMER pin is low. A foldback feature makes the current limit decrease as the voltage at the $5V_{OUT}$ pin approaches GND.

When the TIMER pin is high, the circuit breaker function is enabled. If the voltage across the sense resistor exceeds 55mV but is less than 150mV, the circuit breaker is tripped after a 30µs time delay. In the event the sense resistor voltage exceeds 150mV, the circuit breaker trips immediately and the chip latches off. To disable the current limit, $5V_{SENSE}$ and $5V_{IN}$ can be shorted together.

GATE (Pin 15): High Side Gate Drive for the External 3.3V and 5V N-Channels pass transistors. Requires an external series RC network for the current limit loop compensation and setting the minimum ramp-up rate. During power up, the slope of the voltage rise at the GATE is set by the 50µA current source connected to $12V_{IN}$ and the external capacitor connected to GND (C1, see Figure 1) or by the 3.3V or 5V current limit and the bulk capacitance on the $3V_{OUT}$ or $5V_{OUT}$ supply lines ($C_{LOAD(5VOUT)}$ or $C_{LOAD(3VOUT)}$, see Figure 1). During power down, the slew rate of the GATE voltage is set by the 200µA current source connected to GND and the external GATE capacitor (C1, see Figure 1).

The voltage at the GATE pin will be modulated to maintain a constant current when either the 3V or 5V supplies go into current limit while the TIMER pin is low. In the event of a fault or an undervoltage condition, the GATE pin is immediately pulled to GND.

$3V_{SENSE}$ (Pin 16): 3.3V Current Limit Set. With a sense resistor placed in the supply path between $3V_{IN}$ and $3V_{SENSE}$, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch while the TIMER pin is low. A foldback feature makes the current limit decrease as the voltage at the $3V_{OUT}$ pin approaches GND.

When the TIMER pin is high, the circuit breaker function is enabled. If the voltage across the sense resistor exceeds 55mV but is less than 150mV, the circuit breaker is tripped after a 30µs time delay. In the event the sense resistor voltage exceeds 150mV, the circuit breaker trips immediately and the chip latches off. To disable the current limit, $3V_{SENSE}$ and $3V_{IN}$ can be shorted together.

PIN FUNCTIONS

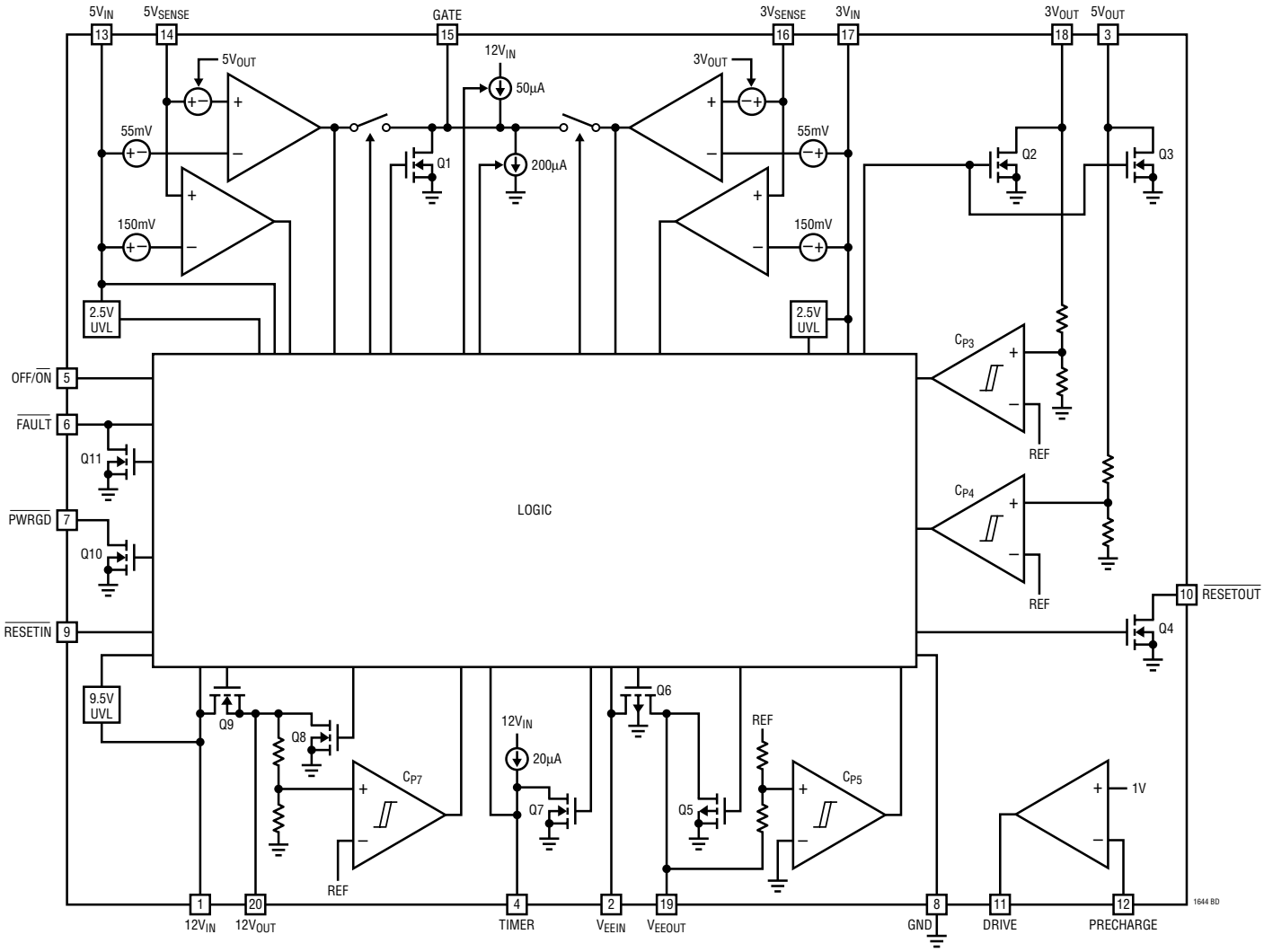
$3V_{IN}$ (Pin 17): 3.3V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the $3V_{IN}$ pin is less than 2.5V. If no 3.3V input supply is available, connect two series diodes between $5V_{IN}$ and $3V_{IN}$ (tie anode of first diode to $5V_{IN}$ and cathode of second diode to $3V_{IN}$, see Figure 11).

$3V_{OUT}$ (Pin 18): Analog Input used to monitor the 3.3V output supply voltage. The PWRGD pin cannot pull low until the $3V_{OUT}$ pin voltage exceeds 2.9V. If no 3.3V input supply is available, tie the $3V_{OUT}$ pin to the $5V_{OUT}$ pin.

V_{EEOUT} (Pin 19): –12V Supply Output. A 1Ω switch is connected between V_{EEIN} and V_{EEOUT}. V_{EEOUT} must exceed –10.5V before the $\overline{PWRGD}$ pin pulls low unless the V_{EE} $\overline{PWRGD}$ function is disabled by grounding the V_{EEIN} pin.

$12V_{OUT}$ (Pin 20): 12V Supply Output. A 0.5Ω switch is connected between $12V_{IN}$ and $12V_{OUT}$. $12V_{OUT}$ must exceed 11.1V before the $\overline{PWRGD}$ pin can pull low.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When a circuit board is inserted into a live CompactPCI (CPCI) slot, the supply bypass capacitors on the board can draw huge supply transient currents from the CPCI power bus as they charge up. The transient currents can cause glitches on the power bus, causing other boards in the system to reset.

The LTC1644 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live CPCI slot without glitching the system power supplies. The chip also protects the supplies from shorts, precharges the bus I/O pins during insertion and extraction and monitors the supply voltages.

The LTC1644 is specifically designed for CPCI applications where the chip resides on the plug-in board.

LTC1644 Feature Summary

- Allows safe board insertion and removal from a CPCI backplane.
- Controls all four CPCI supplies: –12V, 12V, 3.3V and 5V.
- Programmable foldback current limit: a programmable analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
- 12V and –12V circuit breakers: if either supply remains in current limit too long, the circuit breaker will trip, the supplies are turned off and the $\overline{\text{FAULT}}$ pin is pulled low.
- Dual-level, programmable 5V and 3.3V circuit breakers: if either supply exceeds current limit for too long, the circuit breaker will trip, the supplies will be turned off and the $\overline{\text{FAULT}}$ pin will be asserted. In the event that either supply exceeds 3 times the nominal current level, all supplies will be turned off and the $\overline{\text{FAULT}}$ pin will be asserted immediately.
- Current limit during power up: the supplies are allowed to power up in current limit. This allows the chip to power up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using the TIMER pin.
- 12V and –12V power switches on chip.
- $\overline{\text{PWRGD}}$ output: monitors the voltage status of the four supply voltages.
- PCI_RST# combined on-chip with HEALTHY# to create LOCAL_PCI_RST# output. If HEALTHY# deasserts, LOCAL_PCI_RST# is asserted independent of PCI_RST#.
- Precharge output: on-chip reference and amplifier provide 1V for biasing bus I/O connector pins during CPCI card insertion and extraction.
- Space saving 20-pin SSOP package.

PCI Power Requirements

CPCI systems usually require four power rails: 5V, 3.3V, 12V and –12V. The tolerance of the supplies as measured at the components on the plug-in card is summarized in Table 1.

Table 1. PCI Power Supply Requirements

SUPPLY	TOLERANCE	CAPACITIVE LOAD
5V	5V ±5%	<3000µF
3.3V	3.3V ±0.3V	<3000µF
12V	12V ±5%	<500µF
–12V	–12V ±10%	<120µF

APPLICATIONS INFORMATION

Power-Up Sequence

The LTC1644 is specifically designed for hot swapping CPCI boards. The typical application is shown in Figure 1. The 3.3V, 5V, 12V and –12V inputs to the LTC1644 come from the medium length power pins. The long 5V and 3.3V connector pins are shorted to the medium length 5V and 3.3V connector pins on the CPCI plug-in card and provide early power for the LTC1644's precharge circuit, the V(I/O) pull-up resistors and the PCI bridge chip. The BD_SEL# signal is connected to the OFF/$\overline{ON}$ pin while the $\overline{PWRGD}$ pin is connected to the HEALTHY# signal. The HEALTHY# signal is combined with the PCI_RST# signal on-chip to generate the LOCAL_PCI_RST# signal which is available at the $\overline{RESETOUT}$ pin.

The power supplies are controlled by placing external N-channel pass transistors in the 3.3V and 5V power paths and internal pass transistors for the 12V and –12V power paths (Figure 1).

Resistors R1 and R2 provide current fault detection and R5 and C1 provide current control loop compensation. Resistors R3 and R4 prevent high frequency oscillations in Q1 and Q2. Shunt RC snubbers R13-C4 and R14-C5 prevent the $12V_{IN}$ and V_{EEIN} pins, respectively, from ringing beyond the absolute maximum rated supply voltages during hot insertion.

When the CPCI card is inserted, the long 5V and 3.3V connector pins and GND pins make contact first. The LTC1644's precharge circuit biases the bus I/O pins to 1V during this stage of the insertion (Figure 2). The 12V, –12V and 5V and 3.3V medium length pins make contact during the next stage of insertion. At this point the LTC1644 powers on but slot power is disabled as long as the OFF/$\overline{ON}$ pin is pulled high by the 1.2k pull-up resistor to V(I/O). During the final stage of board insertion, the BD_SEL# short connector pin makes contact and the OFF/$\overline{ON}$ pin can be pulled low. This enables the pass transistors to turn on and a 20µA current source is connected to TIMER (Pin 4).

The current in each pass transistor increases until it reaches the current limit for each supply. The 5V and 3.3V supplies are then allowed to power up based on one of the following rates:

Power-up rate: (1)

$$\frac{dV}{dt} = \frac{50\mu A}{C1}, or = \frac{I_{LIMIT(5V)}}{C_{LOAD(5VOUT)}}, or = \frac{I_{LIMIT(3V)}}{C_{LOAD(3VOUT)}}$$

whichever is slower.

Current limit faults are ignored while the TIMER pin voltage is ramping up and is less than 0.4V below $12V_{IN}$ (Pin 1). Once all four supply voltages are within tolerance, HEALTHY# (Pin 7) will pull low and LOCAL_PCI_RST# is free to follow PCI_RST#.

Power-Down Sequence

When the BD_SEL# is pulled high, a power-down sequence begins (Figure 3).

Internal switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin is immediately pulled low. The GATE pin (Pin 15) is pulled down by a 200µA current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and glitching the power supply voltages. When any of the output voltages dips below its threshold, the HEALTHY# signal pulls high and LOCAL_PCI_RST# will be asserted low.

Once the power-down sequence is complete, the CPCI card may be removed from the slot. During extraction, the precharge circuit will continue to bias the bus I/O pins at 1V until the 5V and 3.3V long connector pin connections are broken.

APPLICATIONS INFORMATION

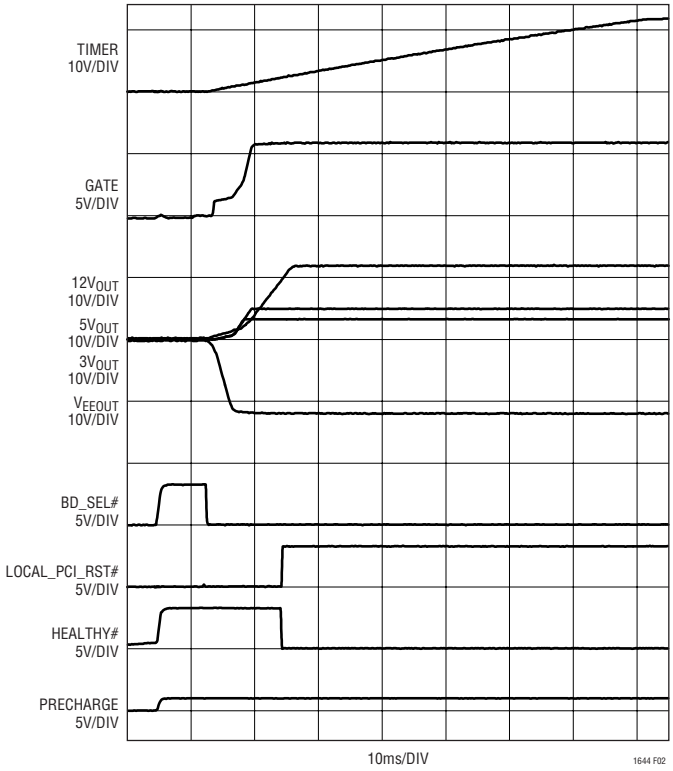


Figure 2. Normal Power-Up Sequence

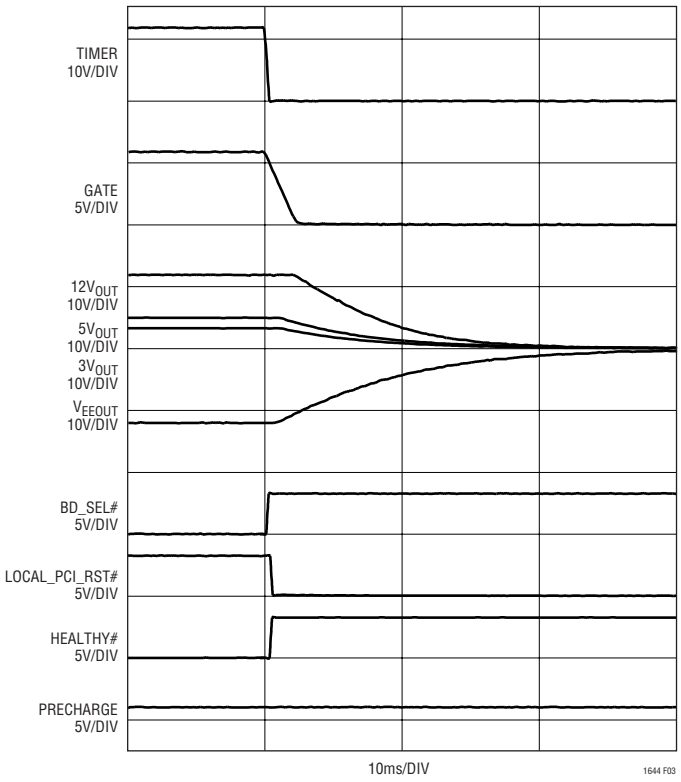


Figure 3. Normal Power-Down Sequence

TIMER

During a power-up sequence, a 20µA current source is connected to the TIMER pin (Pin 4) and current limit faults are ignored until the voltage ramps to within 0.4V of $12V_{IN}$ (Pin 1). This feature allows the chip to power up CPCI boards with widely varying capacitive loads on the supplies. The power-up time for any one of the four outputs is given by Equation 2:

$$t_{ON}(XV_{OUT}) = 2 \bullet \left(\frac{C_{LOAD(XVOUT)} \bullet XV_{OUT}}{I_{LIMIT(XVOUT)} - I_{LOAD(XVOUT)}} \right) \quad (2)$$

where XV_{OUT} = $5V_{OUT}$, $3V_{OUT}$, $12V_{OUT}$ or V_{EEOUT} (–12V). For example, for $C_{LOAD(5VOUT)}$ = 2000µF, $I_{LIMIT(5VOUT)}$ = 7A and $I_{LOAD(5VOUT)}$ = 5A, the $5V_{OUT}$ turn-on time will be ~10ms. By substituting the variables in Equation 2 with the appropriate values, the turn-on time for the other three outputs can be calculated.

The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operting area of the pass transistor during a short circuit. The timer period for the LTC1644 is given by:

$$t_{TIMER} = \frac{C_{TIMER} \bullet 11.6V}{20\mu A} \quad (3)$$

As a design aid, the timer period as a function of the timing capacitor using standard values from 0.01µF to 1µF is shown in Table 2.

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Table 2. t_{TIMER} vs C_{TIMER}

t_{TIMER}	C_{TIMER}	t_{TIMER}	C_{TIMER}
0.01µF	5.8ms	0.22µF	128ms
0.022µF	12.8ms	0.33µF	191ms
0.033µF	19.1ms	0.47µF	273ms
0.047µF	27.3ms	0.68µF	394ms
0.068µF	39.4ms	0.82µF	476ms
0.082µF	47.6ms	1µF	580ms
0.1µF	58.0ms		

The TIMER pin is immediately pulled low when the BD_SEL# signal goes high.

Thermal Shutdown

The internal switches for the 12V and –12V supplies are protected by an internal current limit and a thermal shutdown circuit. When the temperature of the chip reaches 130°C, all switches will be latched off and the $\overline{FAULT}$ pin (Pin 6) will be pulled low.

Short-Circuit Protection

During a normal power-up sequence, if the TIMER (Pin 4) is done ramping and any supply is still in current limit, all of the pass transistors will be immediately turned off and $\overline{FAULT}$ (Pin 6) will be pulled low as shown in Figure 4.

In order to prevent excessive power dissipation in the pass transistors and to prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function where large currents can flow before the breaker trips, the current foldback feature assures that the supply current will be kept at a safe level. In addition, current foldback prevents voltage glitches when powering up into a short.

If either the 12V or –12V supply exceeds current limit after power up, the shorted supply's current will drop immediately to its I_{LIMIT} value. If that supply remains in current limit for more that 30µs, all of the supplies will be latched off. The 30µs delay prevents quick current spikes—for example, from a fan turning on—from causing false trips of the circuit breaker.

After power-up, the 5V and 3.3V supplies are protected from overcurrent and short-circuit conditions by dual-level circuit breakers. In the event that either supply current exceeds the nominal limit but is less than 3 times the current limit, an internal timer is started. If the supply is still overcurrent after 30µs, the circuit breaker trips and all the supplies are turned off (Figure 5). If a short-circuit occurs and the supply current exceeds 3 times the set limit, the circuit breakers trip without any delay and the chip latches off (Figure 6). The chip will stay in the latched off state until OFF/$\overline{ON}$ (Pin 5) is cycled high then low or the $12V_{IN}$ (Pin 1) power supply is cycled off then on.

The current limit and the foldback current level for the 5V and 3.3V outputs are both a function of the external sense resistor (R1 for $3V_{OUT}$ and R2 for $5V_{OUT}$, see Figure 1). As shown in Figure 1, a sense resistor is connected between $5V_{IN}$ (Pin 13) and $5V_{SENSE}$ (Pin 12) for the 5V supply. For the 3V supply, a sense resistor is connected between $3V_{IN}$ (Pin 9) and $3V_{SENSE}$ (Pin 10). The current limit and the foldback current level are given by Equations 4 and 5:

$$I_{LIMIT(XVOUT)} = \frac{55mV}{R_{SENSE(XVOUT)}} \quad (4)$$

$$I_{FOLDBACK(XVOUT)} = \frac{11mV}{R_{SENSE(XVOUT)}} \quad (5)$$

where $XV_{OUT} = 5V_{OUT}$ or $3V_{OUT}$.

As a design aid, the current limit and foldback level for commonly used values for R_{SENSE} is shown in Table 3.

Table 3. $I_{LIMIT(XVOUT)}$ and $I_{FOLDBACK(XVOUT)}$ vs R_{SENSE}

R_{SENSE} (Ω)	$I_{LIMIT(XVOUT)}$	$I_{FOLDBACK(XVOUT)}$
0.005	11A	2.2A
0.006	9.2A	1.8A
0.007	7.9A	1.6A
0.008	6.9A	1.4A
0.009	6.1A	1.2A
0.01	5.5A	1.1A

where $XV_{OUT} = 3V_{OUT}$ or $5V_{OUT}$.

The current limit for the internal 12V switch is set at 850mA folding back to 250mA and the –12V switch at 450mA folding back to 160mA.

APPLICATIONS INFORMATION

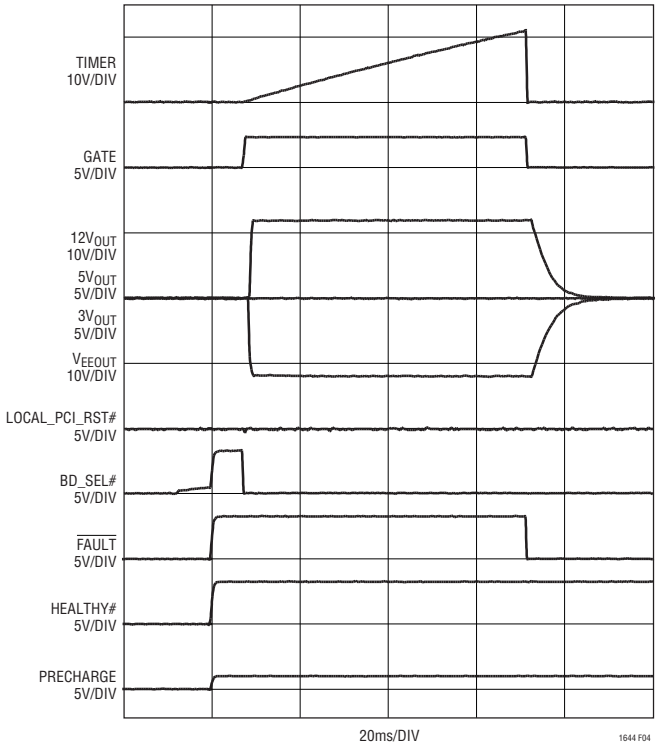

Figure 4. Power-Up into a Short on 3.3V Output

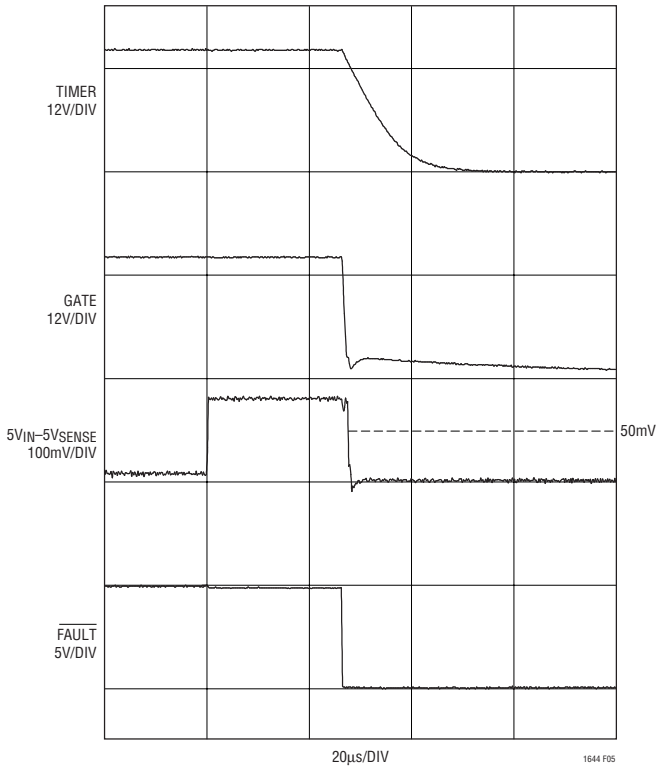

Figure 5. Overcurrent Fault on 5V

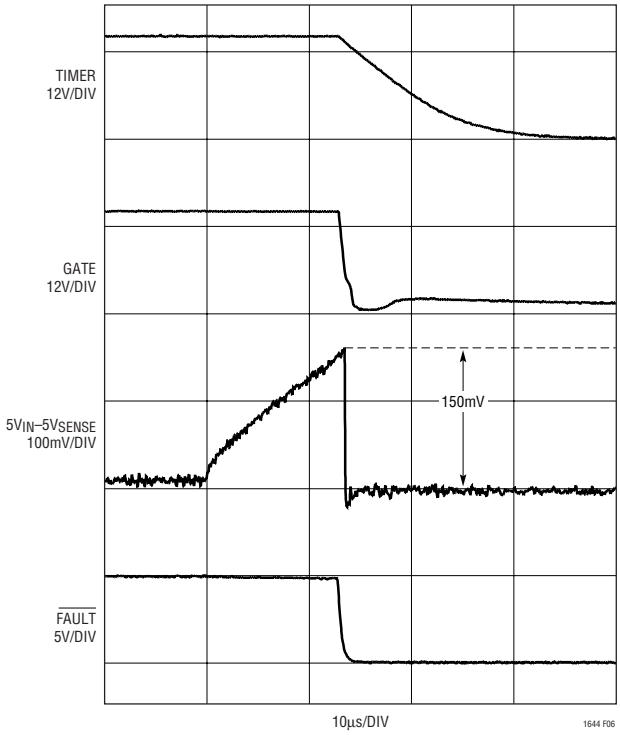

Figure 6. Short-Circuit Fault on 5V

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Calculating R_{SENSE}

An equivalent circuit for one of the LTC1644's circuit breakers useful in calculating the value of the sense resistor is shown in Figure 7. To determine the most appropriate value for the sense resistor first requires the maximum current required by the load under worst-case conditions.

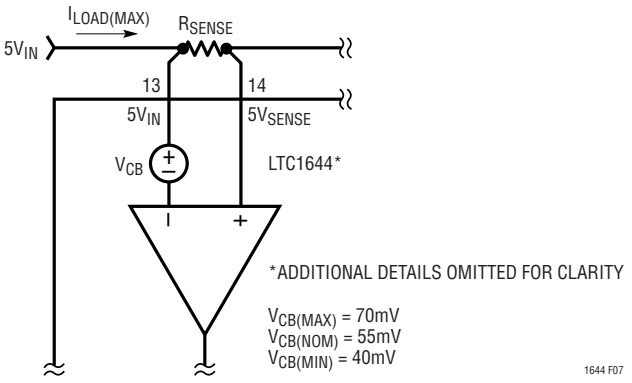

Figure 7. Circuit Breaker Equivalent Circuit for Calculating R_{SENSE}

Two other parameters affect the value of the sense resistor. First is the tolerance of the LTC1644's circuit breaker threshold. The LTC1644's nominal circuit breaker threshold is $V_{CB(NOM)}$ = 55mV; however, it exhibits ±15mV tolerance over temperature. Second is the tolerance (RTOL) in the sense resistor. Sense resistors are available in RTOLs of ±1%, ±2% and ±5% and exhibit temperature coefficients of resistance (TCRs) between ±75ppm/°C and ±100ppm/°C. How the sense resistor changes as a function of temperature depends on the I^2R power being dissipated by it. The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips.

The first step in calculating the value of R_{SENSE} is based on $I_{LOAD(MAX)}$ and the lower limit for the circuit breaker threshold, $V_{CB(MIN)}$. The maximum value for R_{SENSE} in this case is expressed by Equation 6:

$$R_{SENSE} = \frac{V_{CB(MIN)}}{I_{LOAD(MAX)}} \quad (6)$$

The second step is to determine the nominal value of the sense resistor which is dependent on its tolerance (RTOL = ±1%, ±2%, or ±5%) and standard sense resistor values. Equation 7 can be used to calculate the nominal value from the maximum value found by Equation 6:

$$R_{SENSE(NOM)} = \frac{R_{SENSE(MAX)}}{1+\left(\frac{RTOL}{100}\right)} \quad (7)$$

Often, the result of Equation 7 may not yield a standard sense resistor value. In this case, two sense resistors with the same RTOL can be connected in parallel to yield $R_{SENSE(NOM)}$.

The last step requires calculating a new value for $I_{TRIP(MAX)}$ ($I_{TRIP(MAX,NEW)}$) based on a minimum value for R_{SENSE} ($R_{SENSE(MIN)}$) and the upper limit for the circuit breaker threshold, $V_{CB(MAX)}$. Should the calculated value for $I_{TRIP(MAX,NEW)}$ be much greater than the design value for $I_{LOAD(MAX)}$, a larger sense resistor value should be selected and the process repeated. The new value for $I_{TRIP(MAX,NEW)}$ is given by Equation 8:

$$I_{TRIP(MAX,NEW)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}} \quad (8)$$

$$\text{where } R_{SENSE(MIN)} = R_{SENSE(NOM)} \bullet \left[1-\left(\frac{RTOL}{100}\right)\right]$$

Example: A 5V supply exhibits a nominal 5A load with a maximum load current of 6.1A ($I_{LOAD(MAX)}$ = 6.1A) and sense resistors with ±5% RTOL will be used. According to Equation 6, $V_{CB(MIN)}$ = 40mV and $R_{SENSE(MAX)}$ is given by:

$$R_{SENSE(MAX)} = \frac{V_{CB(MIN)}}{I_{LOAD(MAX)}} = \frac{40mV}{6.1A} = 0.0066\Omega$$

The nominal sense resistor value is (Equation 7):

$$R_{SENSE(NOM)} = \frac{R_{SENSE(MAX)}}{1+\left(\frac{RTOL}{100}\right)} = \frac{0.0066\Omega}{1+\left(\frac{5}{100}\right)} = 0.006\Omega$$

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And the new current-limit trip point is (Equation 8):

$$I_{TRIP(MAX,NEW)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}}$$

$$= \frac{V_{CB(MAX)}}{R_{SENSE(NOM)} \bullet \left[1 - \left(\frac{RTOL}{100}\right)\right]}$$

$$= \frac{70mV}{0.006} = 11.2A$$

Since $I_{TRIP(MAX,NEW)} > I_{LOAD(MAX)}$, a larger value for R_{SENSE} should be selected and the process repeated again to lower $I_{TRIP(MAX,NEW)}$ without substantially affecting $I_{LOAD(MAX)}$. Table 5 lists suggested sense resistors that can be used with the LTC1644's circuit breaker.

Output Voltage Monitor

The status of all four output voltages is monitored by the power good function. In addition, the PCI_RST# signal is logically combined on-chip with the HEALTHY# signal to create LOCAL_PCI_RST# (see Table 2). As a result, LOCAL_PCI_RST# will be pulled low whenever HEALTHY# is pulled high independent of the state of the PCI_RST# signal.

Table 4. LOCAL_PCI_RST# Truth Table

PCI_RST#	HEALTHY#	LOCAL_PCI_RST#
LO	LO	LO
LO	HI	LO
HI	LO	HI
HI	HI	LO

If any of the output voltages drop below the power good threshold for more than 10µs, the $\overline{PWRGD}$ pin will be pulled high and the LOCAL_PCI_RST# signal will be asserted low.

Precharge

The PRECHARGE input and DRIVE output pins are intended for use in generating the 1V precharge voltage that is used to bias the bus I/O connector pins during board insertion and extraction. The circuit in Figure 8 is capable of biasing up to 128 connector pins I/O connector pins simultaneously for V(I/O) voltages up to 5V.

Other CompactPCI Applications

The LTC1644 can be easily configured for applications where no V_{EE} supply is present by simply connecting the V_{EEIN} pin to GND and floating the V_{EEOUT} pin (Figure 9).

For CPCI applications where no 5V supply input is required, short both the $5V_{IN}$ and $5V_{SENSE}$ pins to the $3V_{IN}$ pin and short the $5V_{OUT}$ pin to the $3V_{OUT}$ pin (Figure 10).

If no 3.3V supply input is required, Figure 11 illustrates how the LTC1644 should be configured. First, $3V_{SENSE}$ (Pin 16) is connected to $3V_{IN}$ (Pin 17), $3V_{OUT}$ (Pin 18) is connected to $5V_{OUT}$ (Pin 3) and the LTC1644's $3V_{IN}$ pin is connected through a pair of signal diodes (BAV99) to $5V_{IN}$.

For applications where the BD_SEL# connector pin is typically grounded on the backplane, the circuit in Figure 12 allows the LTC1644 to be reset simply by pressing a pushbutton switch on the CPCI plugin board. This arrangement eliminates the requirement to extract and reinsert the CPCI board in order to reset the LTC1644's circuit breakers.

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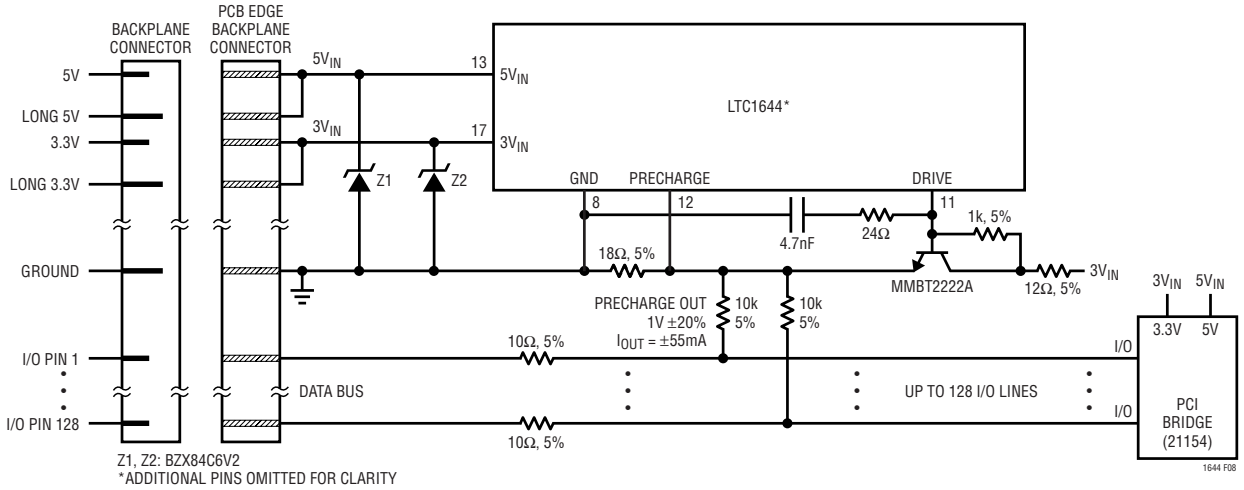

Figure 8. Precharge Application Circuit

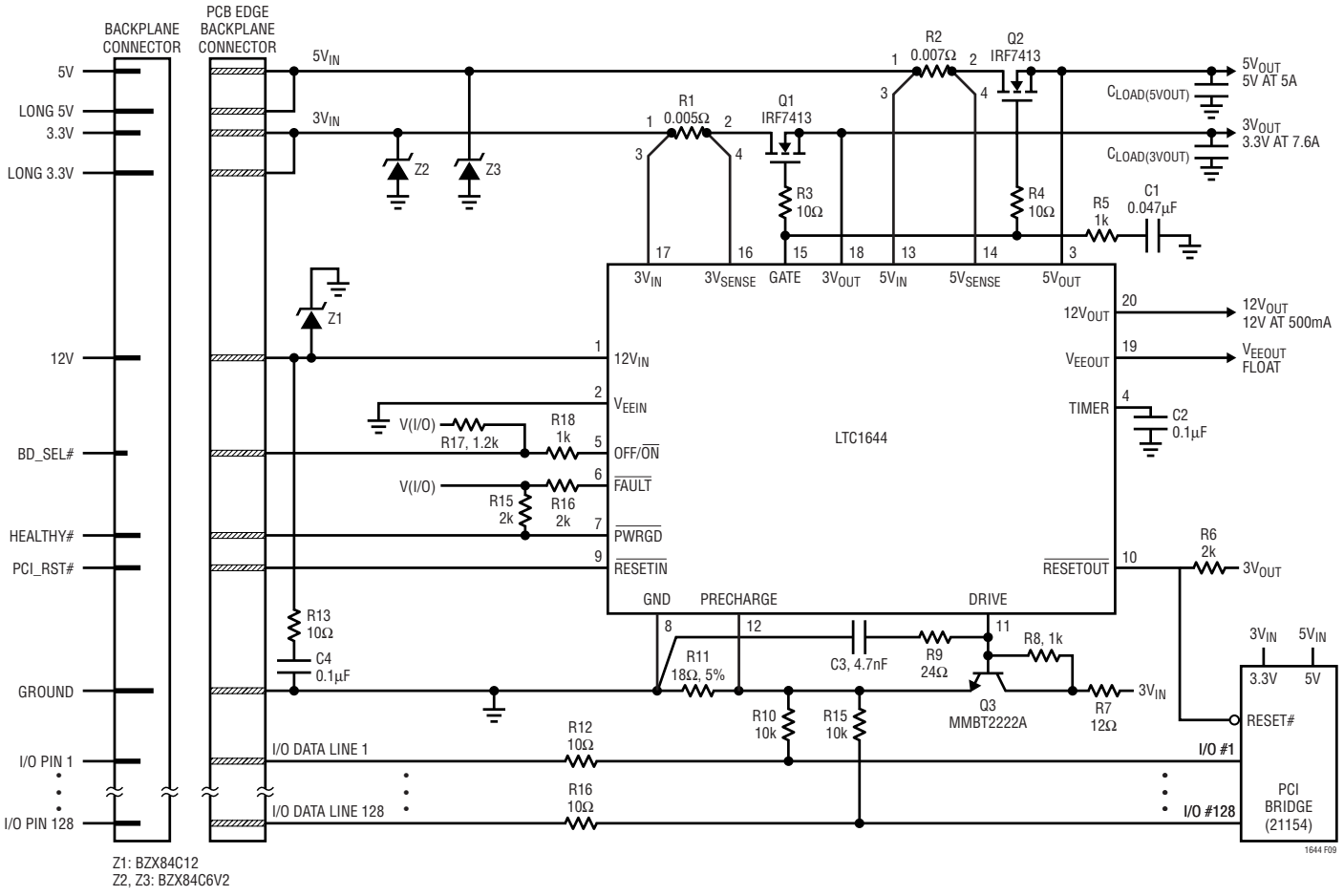

Figure 9. No V_{EE} (–12V) Supply Application Circuit

APPLICATIONS INFORMATION

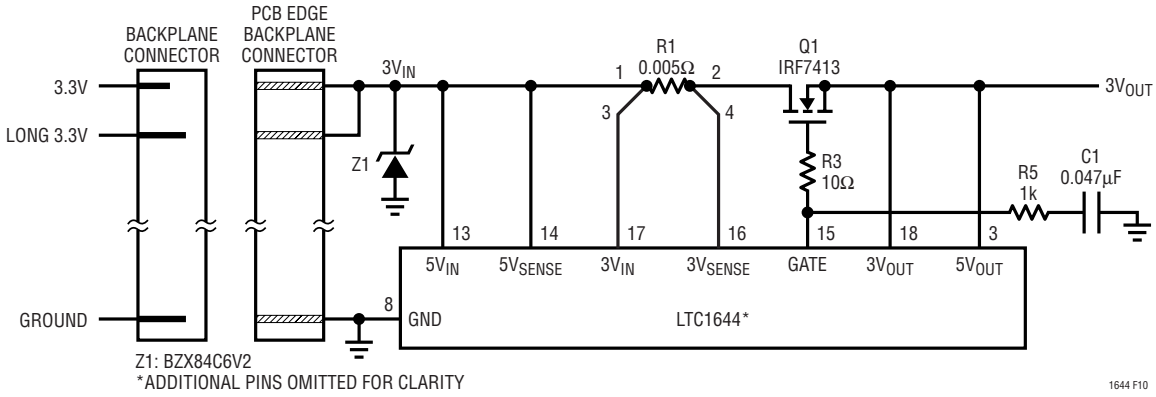

Figure 10. No 5V Supply Application Circuit

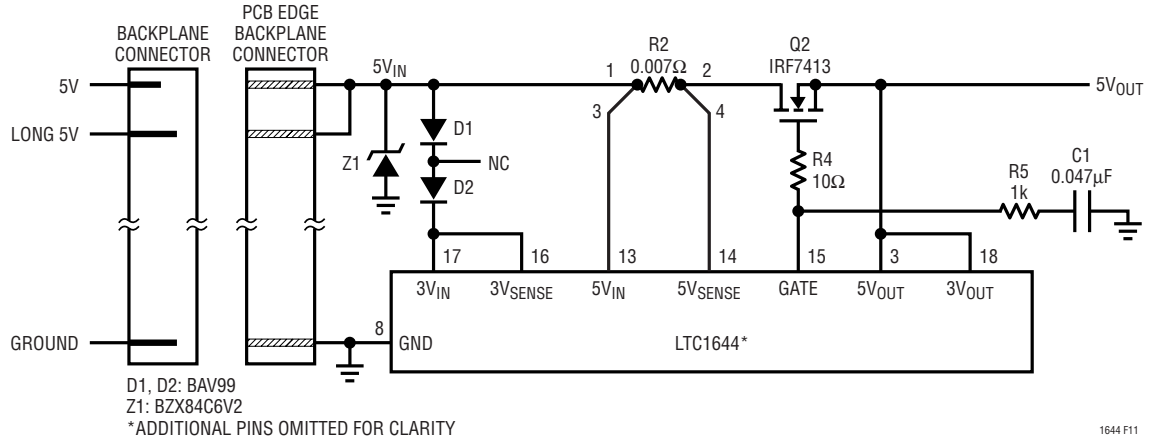

Figure 11. No 3.3V Supply Application Circuit

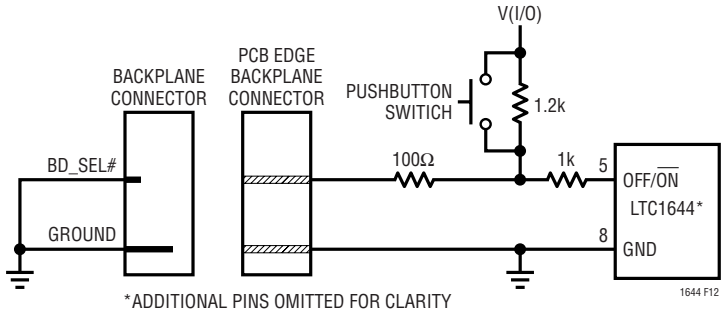

Figure 12. BD_SEL# Pushbutton Toggle Switch

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Power MOSFET Selection Criteria

Three device parameters are key in selecting the optimal power MOSFET for Hot Swap applications. The three parameters are: (1) device power dissipation (P_D); (2) device drain-source channel ON resistance, $R_{DS(ON)}$; and (3) the gate-source (V_{GS}) voltage drive for the specified $R_{DS(ON)}$. Power MOSFET power dissipation is dependent on four parameters: current delivered to the load, I_{LOAD}; device $R_{DS(ON)}$; device thermal resistance, junction-to-ambient, θ_{JA}; and the maximum ambient temperature to which the circuit will be exposed, $T_{A(MAX)}$. All four of these parameters determine the junction temperature of the MOSFET. For reliable circuit operation, the maximum junction temperature ($T_{J(MAX)}$) for a power MOSFET should not exceed the manufacturer's recommended value. For a given set of conditions, the junction temperature of a power MOSFET is given by Equation 9:

MOSFET Junction Temperature, (9)

$$T_{J(MAX)} \leq T_{A(MAX)} + \theta_{JA} \bullet P_D$$

where $P_D = I_{LOAD} \bullet R_{DS(ON)}$

PCB layout techniques for optimal thermal management of power MOSFET power dissipation help to keep device θ_{JA} as low as possible. See PCB Layout Considerations section for more information.

The $R_{DS(ON)}$ of the external pass transistor should be low to make its drain-source voltage (V_{DS}) a small percentage of $3V_{IN}$ or $5V_{IN}$. For example, at $3V_{IN}$ = 3.3V, $V_{DS} + V_{CB}$ = 0.1V yields a 3% error at maximum load current. This restricts the choice of power MOSFETs to those devices with very low $R_{DS(ON)}$. Table 6 lists some power MOSFETs that can be used with the LTC1644.

Power MOSFETs are classified into two categories: standard MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 10V) and logic-level MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 5V). Since external pass transistors are required for the 3.3V and 5V supply rails, logic-level power MOSFETs should be used with the LTC1644.

Overvoltage Transient Protection

Good engineering practice calls for bypassing the supply rail of any analog circuit. Bypass capacitors are often placed at the supply connection of every active device, in addition to one or more large-value bulk bypass capacitors per supply rail. If power is connected abruptly, the large bypass capacitors slow the rate of rise of the supply voltage and heavily damp any parasitic resonance of lead or PC track inductance working against the supply bypass capacitors.

The opposite is true for LTC1644 Hot Swap circuits mounted on plug-in cards. In most cases, there is no supply bypass capacitor present on the powered 12V ($12V_{IN}$), –12V (V_{EEIN}) of the PCB edge connector or on the 3.3V ($3V_{IN}$) or the 5V ($5V_{IN}$) side of the MOSFET switch. An abrupt connection, produced by inserting the board into a backplane connector, results in a fast rising edge applied on these input supply lines of the LTC1644.

Since there is no bulk capacitance to damp the parasitic track inductance, supply voltage transients excite parasitic resonant circuits formed by the power MOSFET capacitance and the combined parasitic inductance from the wiring harness, the backplane and the circuit board traces. These ringing transients appear as a fast edge on the input supply lines, exhibiting a peak overshoot to 2.5 times the steady-state value followed by a damped sinusoidal response whose duration and period is dependent on the resonant circuit parameters. Since the absolute maximum supply voltage of the LTC1644 is 14V, transient protection against $12V_{IN}$ and V_{EEIN} supply voltage spikes and ringing is highly recommended.

In these applications, there are two methods for eliminating these supply voltage transients: using Zener diodes to clip the transient to a safe level and snubber networks. Snubber networks are series RC networks whose time constants are experimentally determined based on the board's parasitic resonance circuits. As a starting point, the capacitors in these networks are chosen to be 10× to 100× the power MOSFET's C_{OSS} underbias. The series resistor is a value determined experimentally and ranges from 1Ω to 50Ω, depending on the parasitic resonance circuit. Note that in all LTC1644 circuit schematics, Zener diodes and snubber networks have been added to the

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$12V_{IN}$ and V_{EEIN} (–12V) supply rail and should be used always. Since the absolute maximum supply voltage of the LTC1644 is 14V, snubber networks are not necessary on the $3V_{IN}$ or the $5V_{IN}$ supply lines. Zener diodes, however, are recommended as these devices provide large-scale transient protection for the LTC1644 against PCI backplane fault occurrences. All protection networks should be mounted very close to the LTC1644's supply voltage using short lead lengths to minimize lead inductance. This is shown schematically in Figures 13 and 14 and a recommended layout of the transient protection devices around the LTC1644 is shown in Figure 15.

PCB Layout Considerations

For proper operation of the LTC1644's circuit breaker operation, 4-wire Kelvin-sense connections between the sense resistor and the LTC1644's $5V_{IN}$ and $5V_{SENSE}$ pins and $3V_{IN}$ and $3V_{SENSE}$ pins are strongly recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation.

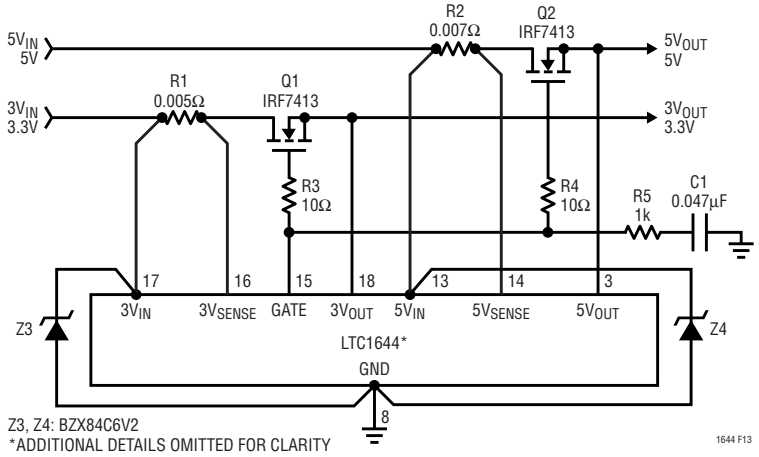

Figure 13. Place Transient Protection Devices Close to LTC1644's $5V_{IN}$ and $3V_{IN}$ Pins

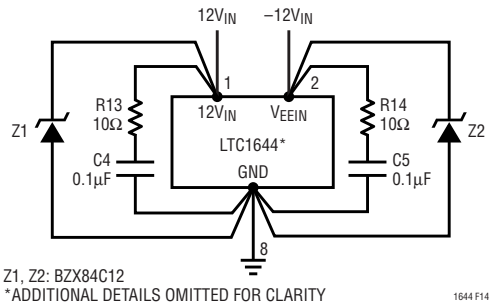

Figure 14. Place Transient Protection Devices Close to LTC1644's $12V_{IN}$ and V_{EEIN} Pins

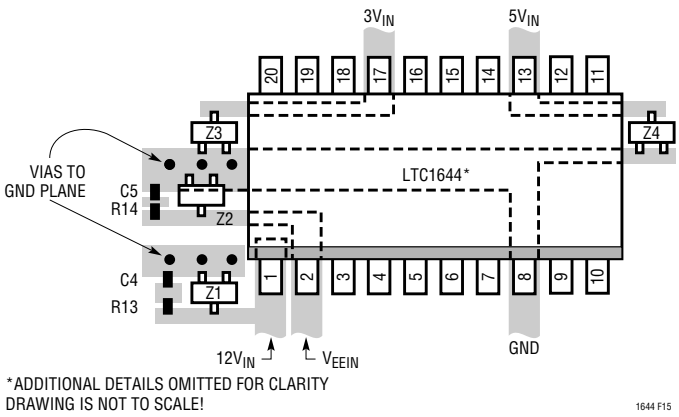

Figure 15. Recommended Layout for Transient Protection Components

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A recommended PCB layout for the sense resistor, the power MOSFET and the GATE drive components around the LTC1644 is illustrated in Figure 16. In Hot Swap applications where load currents can be 10A, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately 0.45mΩ/□, track resistances add up quickly in high current applications. Thus, to keep PCB track resistance and temperature rise to a minimum, the suggested trace width in these applications for 1 ounce copper foil is 0.03" for each ampere of DC current.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1 ounce copper foil plating, a good rule of thumb is 1 ampere of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

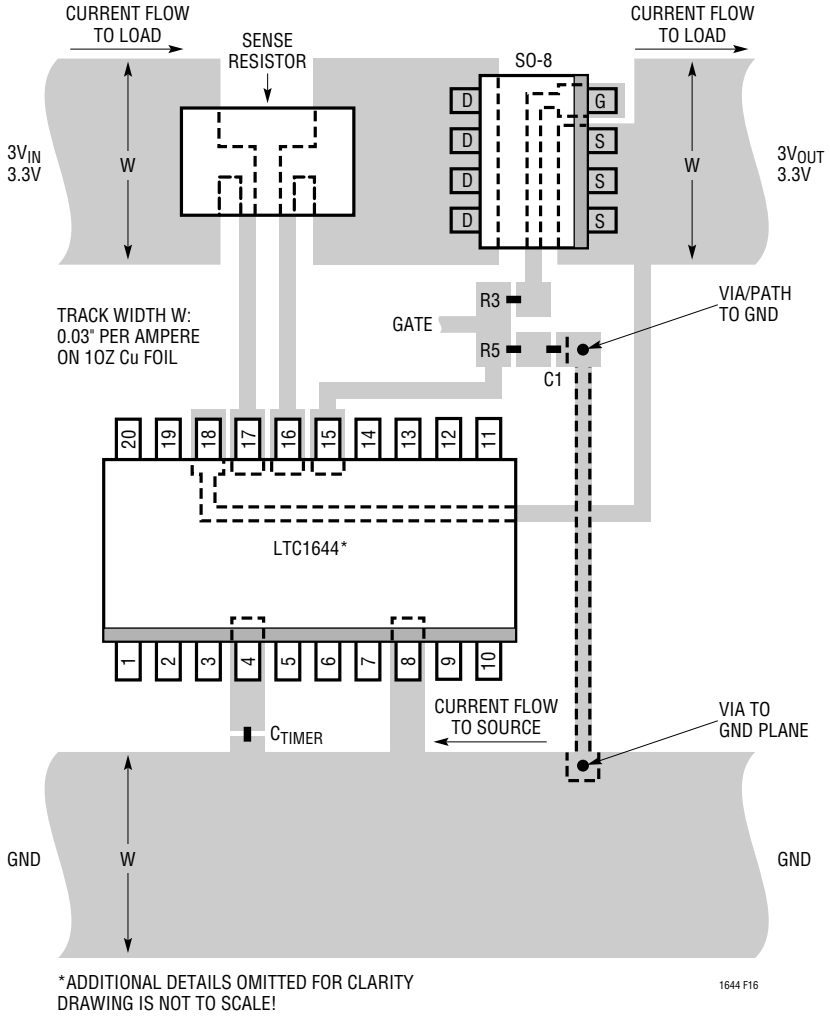

Figure 16. Recommended Layout for Power MOSFET, Sense Resistor and GATE Components for the 3.3V Rail

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Power MOSFET and Sense Resistor Selection

Table 5 lists some current sense resistors that can be used the LTC1644's circuit breakers and Table 6 list some power MOSFET transistors that are available. Table 7 lists supplier web site addresses for discrete component mentioned throughout the LTC1644 data sheet.

Table 7. Manufacturers' Web Site

MANUFACTURER	WEB SITE
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
IRC-TT	www.irctt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

Obtaining Information on Specific Parts

For more information regarding or to request a copy of the CompactPCI specification, contact the PCI Industrial Computer Manufacturers Group at:

PCI Industrial Computer Manufacturers Group
Wakefield, MA 01880 USA
Phone: 01 (617) 224-1100
Web Site: http://www.picmg.com

TransZorb SMAJ12A and diodes BAV99 are supplied by:

Diodes, Incorporated
Westlake Village, CA 91362 USA
Phone: 01 (805) 446-4800
Web Site: http://www.vishay-liteon.com or
http://www.diodes.com

Transistor MMBT2222A is supplied by:

Semiconductor Components Industries, LLC
Phoenix, AZ 85008 USA
Phone: 01 (602) 244-6600
Web Site: http://www.onsemi.com

Table 5. Sense Resistor Selection Guide

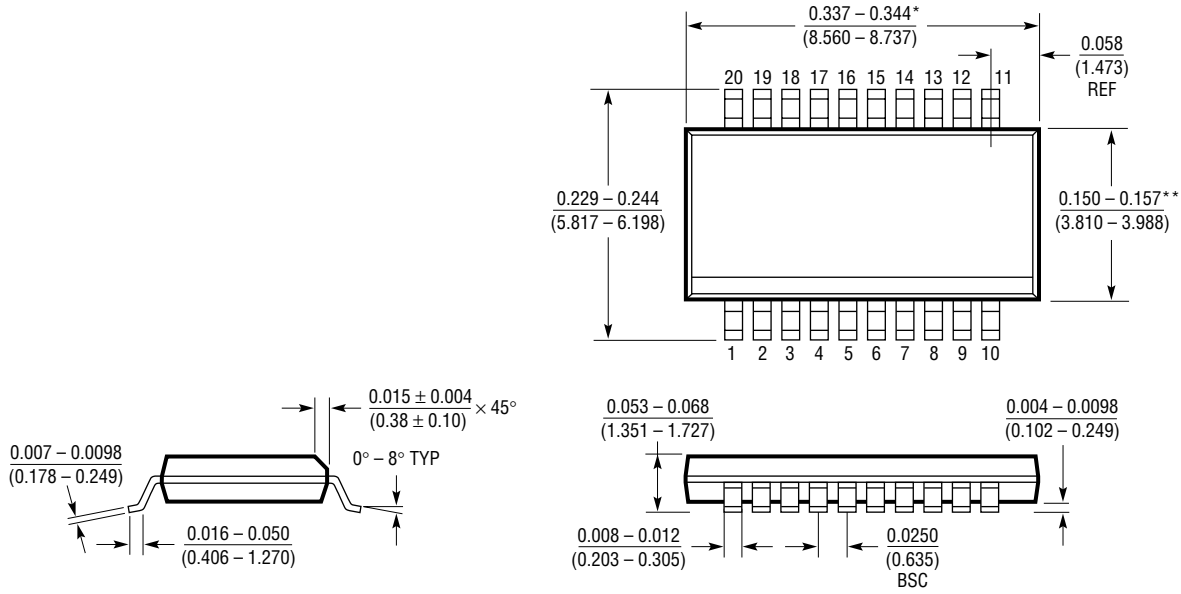
CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R055F WSL1206R055	0.055Ω, 0.5W, 1% Resistor	IRC-TT Vishay-Dale
2A	LR120601R028F WSL1206R028	0.028Ω, 0.5W, 1% Resistor	IRC-TT Vishay-Dale
5A	LR120601R011F WSL2010R011	0.011Ω, 0.5W, 1% Resistor	IRC-TT Vishay-Dale
7.6A	WSL2512R007	0.007Ω, 1W, 1% Resistor	Vishay-Dale
10A	WSL2512R005	0.005Ω, 1W, 1% Resistor	Vishay-Dale

Table 6. N-Channel Power MOSFET Selection Guide

CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.1Ω	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.025Ω	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.028Ω	ON Semiconductor
5 to 10	IRF7413	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.01Ω	International Rectifier
5 to 10	Si4410DY	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.01Ω	Vishay-Siliconix

PACKAGE DESCRIPTION

GN Package
20-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	Dual Supplies from 3V to 12V, Additionally –12V
LTC1422	Hot Swap Controller	Single Supply Hot Swap in SO-8 from 3V to 12V
LT1640AL/LT1640AH	Negative Voltage Hot Swap Controllers in SO-8	Negative High Voltage Supplies from –10V to –80V
LT1641/LT1641-1	Positive Voltage Hot Swap Controller in SO-8	Supplies from 9V to 80V, Autoretry/Latch Off
LTC1642	Fault Protected Hot Swap Controller	3V to 15V, Overvoltage Protection Up to 33V
LTC1643L/LTC1643L-1/LTC1643H	PCI Bus Hot Swap Controllers	3.3V, 5V, 12V, –12V Supplies for PCI Bus
LTC1645	2-Channel Hot Swap Controller	Operates from 1.2V to 12V, Power Sequencing
LTC1646	Dual CompactPCI Hot Swap Controller	3.3V, 5V Supplies Only
LTC1647	Dual Hot Swap Controller	Dual ON Pins for Supplies from 3V to 15V
LTC4211	Hot Swap Controller with Multifunction Current Control	Single Supply, 2.5V to 16.5V, MSOP
LT4250	–48V Hot Swap Controller in SO-8	–20V to –80V, Active Current Limiting
LTC4251	–48V Hot Swap Controller in SOT-23	Floating Supply, Active Current Limiting and Fast Circuit Breaker

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LT/TP 0801 1.5K • PRINTED IN USA

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