

Document Title

256Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	December 26, 2001	Preliminary

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256K x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 256K x16 bit
- Power Supply Voltage: 1.65~2.20V
- Low Data Retention Voltage: 1.0V(Min)
- Three State Outputs
- Package Type: 48-TBGA-6.00x7.00

GENERAL DESCRIPTION

The K6F4016R6F families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The family also supports low data retention voltage for battery back-up operation with low data retention current.

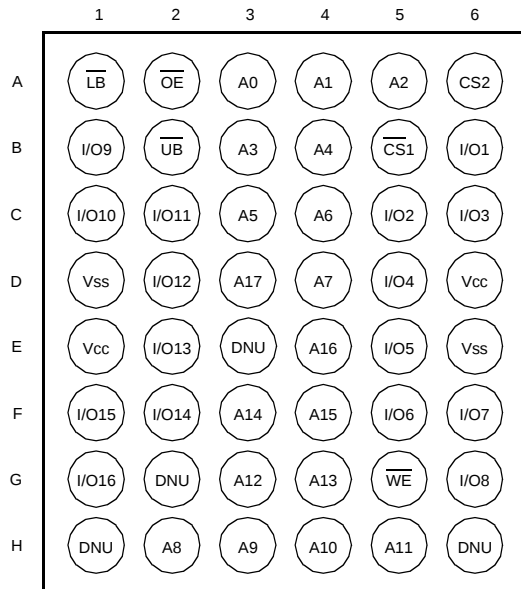
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Typ.)	Operating (I _{CC1} , Max)	
K6F4016R6F-F	Industrial(-40~85°C)	1.65~2.20V	70 ¹⁾ /85ns	0.5μA ²⁾	2mA	48-TBGA-6.00x7.00

1. The parameter is measured with 30pF test load.

2. Typical values are measured at V_{CC}=2.0V, T_A=25°C and not 100% tested.

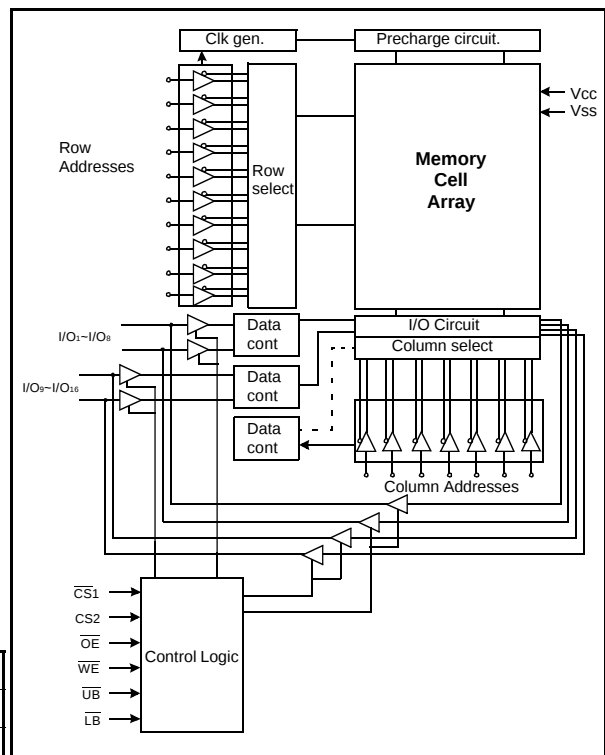
PIN DESCRIPTION



48-TBGA: Top View (Ball Down)

Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	Vcc	Power
OE	Output Enable Input	Vss	Ground
WE	Write Enable Input	UB	Upper Byte(I/O9~16)
A0~A17	Address Inputs	LB	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F4016R6F-EF70	48-TBGA, 70ns, 1.8/2.0V
K6F4016R6F-EF85	48-TBGA, 85ns, 1.8/2.0V

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.3V(Max. 2.5V)	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.3 to 2.5	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	1.65	1.8/2.0	2.2	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	1.4	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	-0.3 ³⁾	-	0.4	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, $\overline{LB} \leq 0.2V$ or/and $\overline{UB} \leq 0.2V$, $CS_2 \geq V_{CC} - 0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	2	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1 = V_{IL}$, CS ₂ =V _{IH} , $\overline{LB} = V_{IL}$ or/and $\overline{UB} = V_{IL}$, V _{IN} =V _{IL} or V _{IH}	85ns	-	-	15	mA
		70ns	-	-	17		
Output low voltage	V _{OL}	I _{OL} = 0.1mA	-	-	0.2	V	
Output high voltage	V _{OH}	I _{OH} = -0.1mA	1.4	-	-	V	
Standby Current (CMOS)	I _{SB1}	Other input =0-V _{CC} 1) $\overline{CS}_1 \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ ($\overline{CS}_1$ controlled) or 2) $0V \leq CS_2 \leq 0.2V$ (CS ₂ controlled)	-	0.5	8	μA	

1. Typical values are measured at V_{CC}=2.0V, T_A=25°C and not 100% tested.

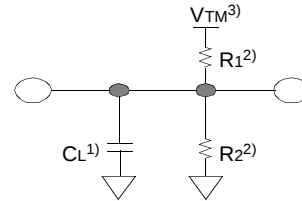
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to $V_{CC}-0.2V$

Input rising and falling time: 5ns

Input and output reference voltage: 0.9V

Output load (See right): $C_L = 100pF + 1TTL$ $C_L = 30pF + 1TTL$ 

1. Including scope and jig capacitance
2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$
3. $V_{TM} = 1.8V$

AC CHARACTERISTICS ($T_A = -40$ to $85^\circ C$, $V_{CC} = 1.65 \sim 2.2V$)

Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	ns
	Address access time	t _{AA}	-	70	-	85	ns
	Chip select to output	t _{CO}	-	70	-	85	ns
	Output enable to valid output	t _{OE}	-	35	-	40	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t _{BA}	-	70	-	85	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t _{BLZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t _{BHZ}	0	25	0	25	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	25	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
Write	Write cycle time	t _{WC}	70	-	85	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t _{BW}	60	-	70	-	ns
	Write pulse width	t _{WP}	50	-	60	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	30	-	35	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

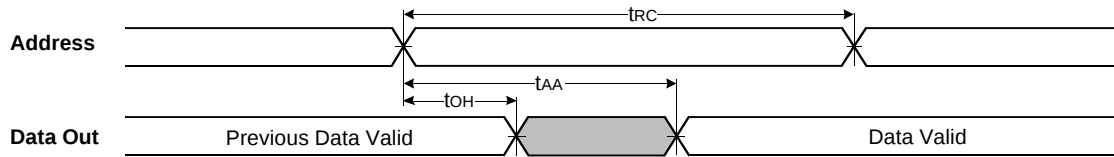
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	VDR	$\overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$, $V_{IN} \geq 0V$	1.0	-	2.2	V
Data retention current	IDR	$V_{CC} = 1.2V$, $\overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$, $V_{IN} \geq 0V$	-	0.5 ⁽²⁾	3	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t _{RDR}		t _{RC}	-	-	

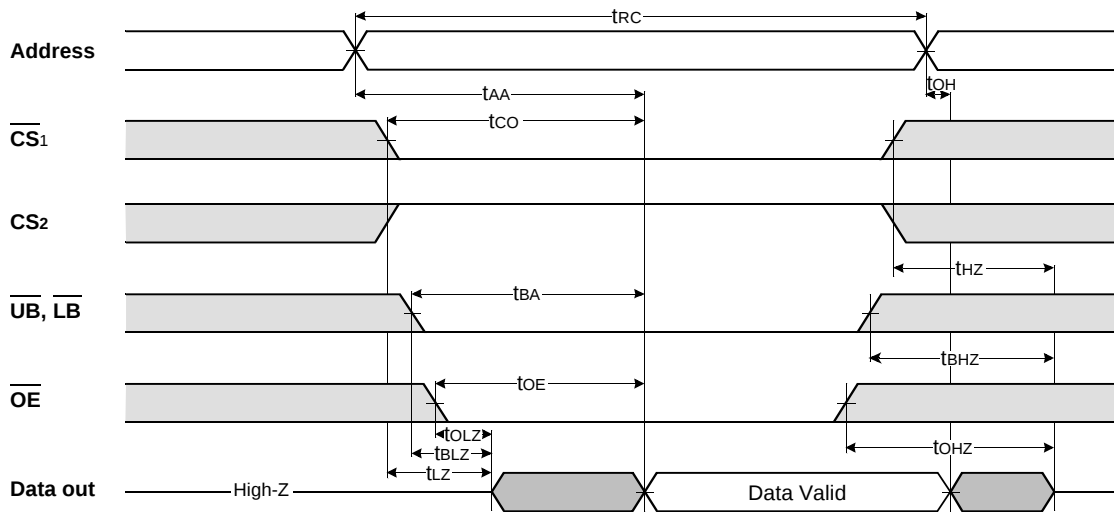
1. 1) $\overline{CS}_1 \geq V_{CC}-0.2V$, $\overline{CS}_2 \geq V_{CC}-0.2V$ ($\overline{CS}_1$ controlled) or2) $0 \leq \overline{CS}_2 \leq 0.2V$ ($\overline{CS}_2$ controlled)2. Typical values are measured at $T_A = 25^\circ C$ and not 100% tested.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{CS2}=\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)



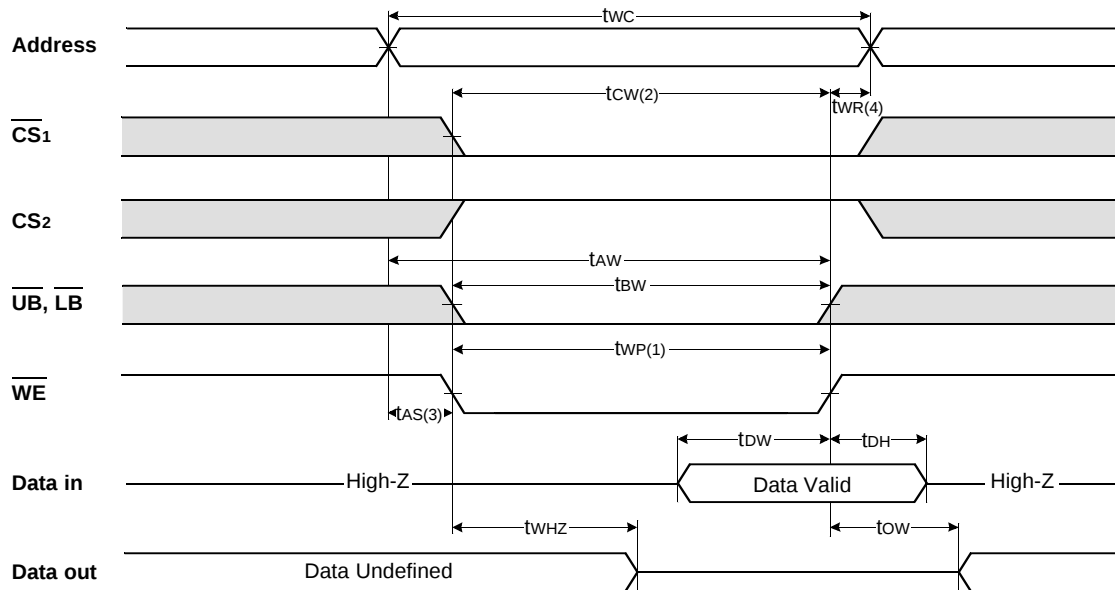
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



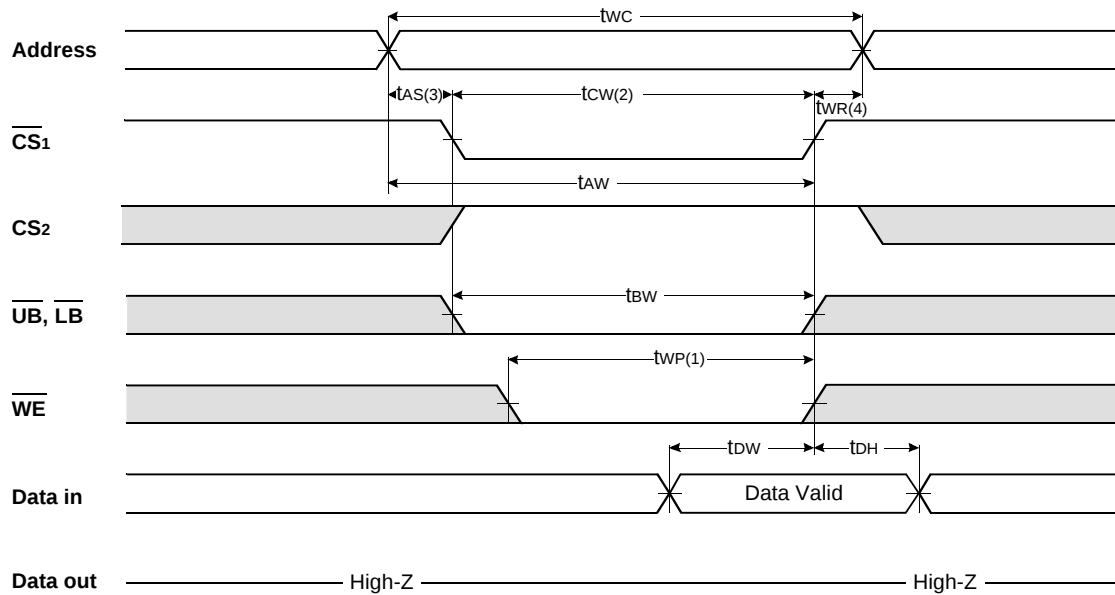
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

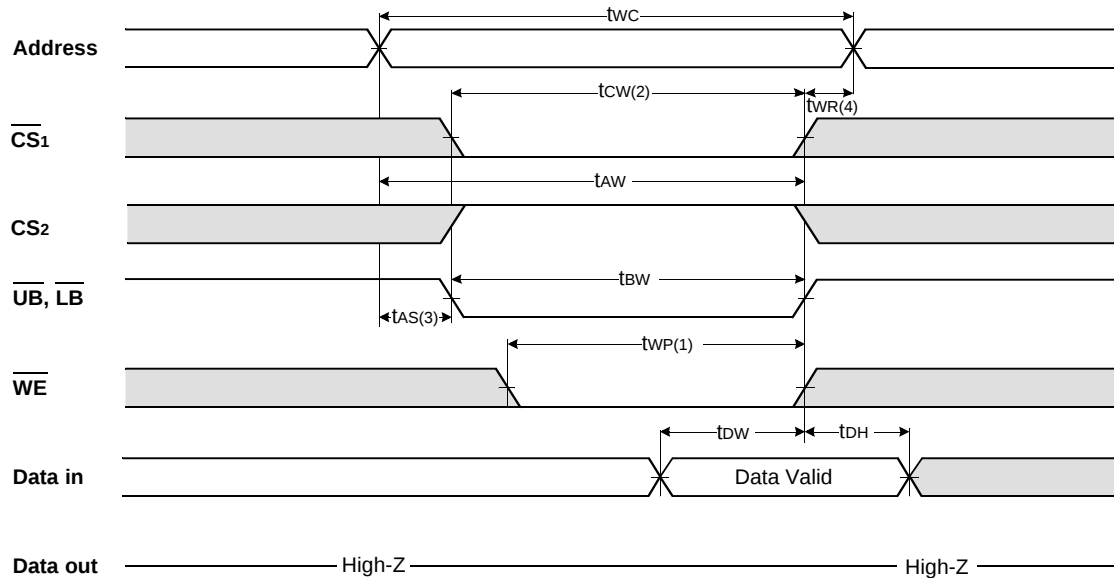
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

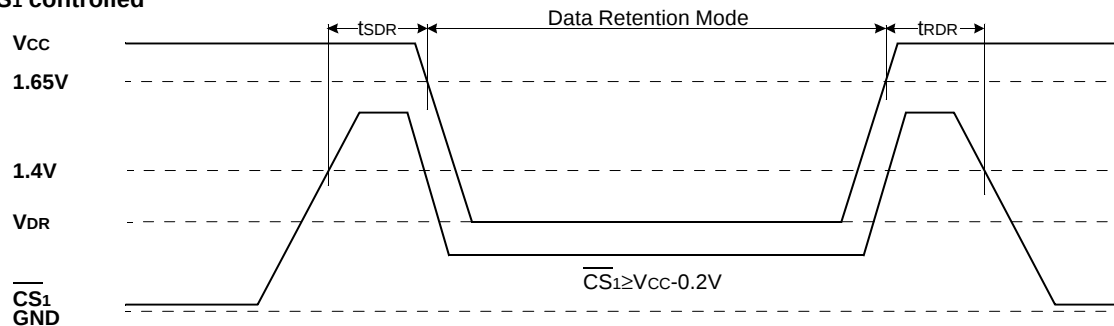


NOTES (WRITE CYCLE)

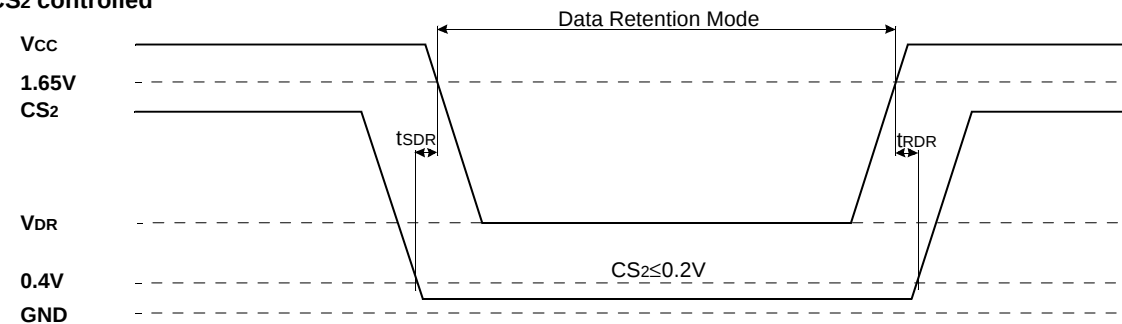
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low $\overline{WE}$. A write begins when $\overline{CS1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$ controlled



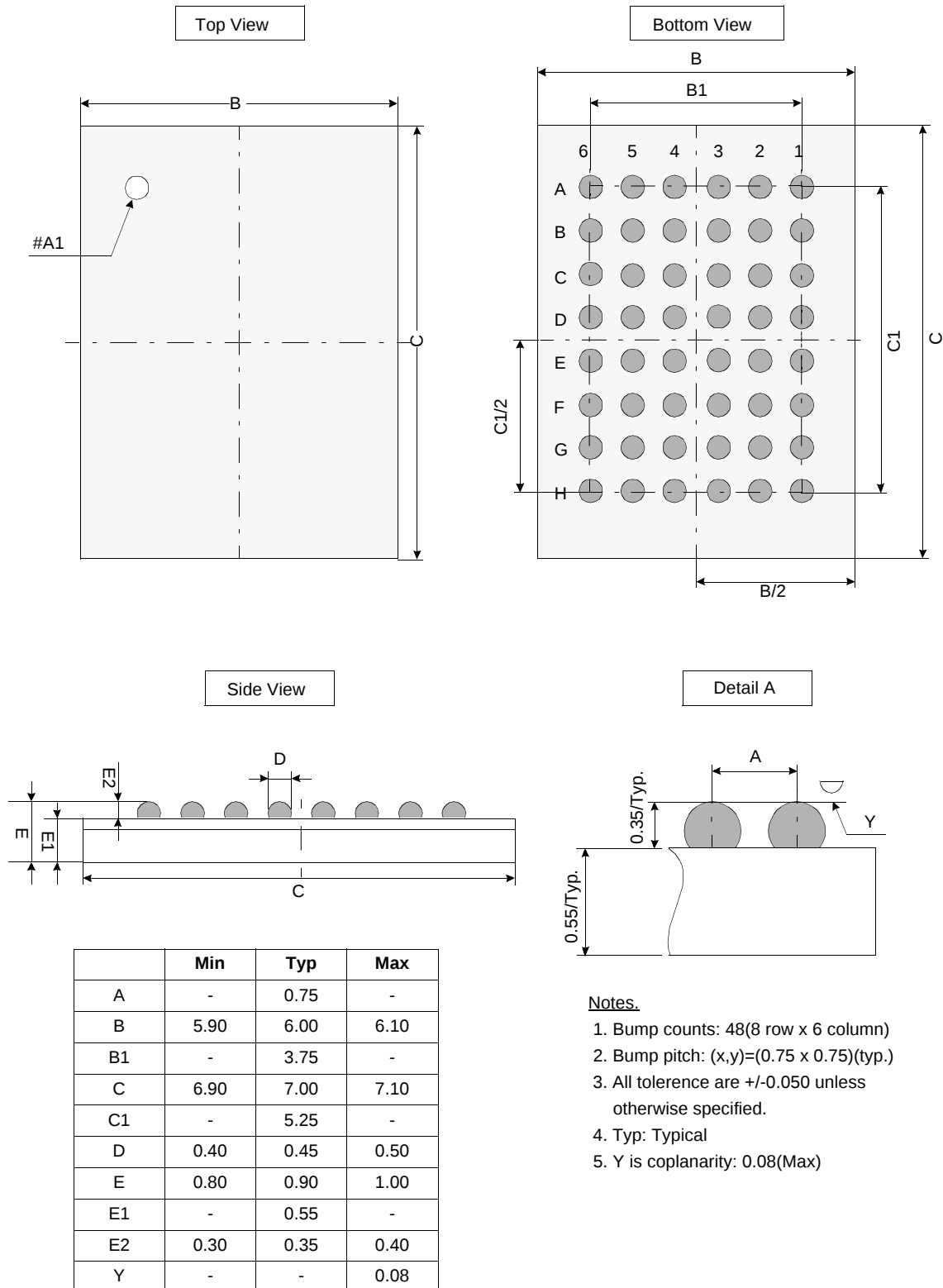
$\overline{CS2}$ controlled



PACKAGE DIMENSION

Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)



Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)