Document Title

1Mx36 & 2Mx18-Bit Pipelined N*t*RAM™

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	May. 10. 2001	Preliminary
0.1	1. Add 165FBGA package	Aug. 29. 2001	Preliminary
0.2	1.Update JTAG scan order 2. Speed bin merge. From K7N3236(18)49M to K7N3236(18)45M 3. AC parameter change. tOH(min)/tLZC(min) from 0.8 to 1.5 at -25 tOH(min)/tLZC(min) from 1.0 to 1.5 at -22 tOH(min)/tLZC(min) from 1.0 to 1.5 at -20	Dec. 31. 2001	Preliminary
0.3	1. Change pin out for 165FBGA - x18/x36 ; 11B => from A to NC , 2R ==> from NC to A	Feb. 14. 2002	Preliminary
0.4	1. Insert pin at JTAG scan order of 165FBGA in connection with pin out change - x18/x36 ; insert Pin ID of 2R to $\overline{BIT}$ number of 69	Apr. 20. 2002	Preliminary
0.5	1. Add Icc, Isb, Isb1 and Isb2 values.	May. 10. 2002	Preliminary
1.0	1. Final datasheet release.	Sep. 26. 2002	Final
1.1	1. Change the Stand-by current (Isb) Before After Isb - 25 : 120 170 - 22 : 110 160 - 20 : 100 150 - 16 : 90 140 - 15 : 90 140 - 13 : 90 140 Isb1 : 90 110 Isb2 : 80 100	Oct. 17, 2003	Final
2.0	1. Delete the 119BGA package 2. Delete the 225MHz and 150MHz speed bin	Nov. 18, 2003	Final

32Mb NtRAM(Flow Through / Pipelined) Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
2Mx18	K7M321825M-QC75	FlowThrough	3.3	7.5ns	Q:100TQFP F:165FBGA	C (Commercial Temperature Range)
	K7N321801M-Q(F)C25/20/16/13	Pipelined	3.3	250/200/167/133MHz		
	K7N321845M-Q(F)C25/20/16/13	Pipelined	2.5	250/200/167/133MHz		
1Mx36	K7M323625M-QC75	FlowThrough	3.3	7.5ns		
	K7N323601M-Q(F)C25/20/16/13	Pipelined	3.3	250/200/167/133MHz		
	K7N323645M-Q(F)C25/20/16/13	Pipelined	2.5	250/200/167/133MHz		

1Mx36 & 2Mx18-Bit Pipelined N*t*RAM™

FEATURES

- 2.5V ±5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single $\overline{\text{R}}$EAD/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A.
- 165FBGA(11x15 ball aray) with body size of 15mmx17mm.

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-20	-16	-13	Unit
Cycle Time	tCYC	4.0	5.0	6.0	7.5	ns
Clock Access Time	tCD	2.6	3.2	3.5	4.2	ns
Output Enable Access Time	tOE	2.6	3.2	3.5	4.2	ns

GENERAL DESCRIPTION

The K7N323645M and K7N321845M are 37,748,736-bits Synchronous Static SRAMs.

The N*t*RAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles.

Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock.

Burst order control must be tied "High or Low".

Asynchronous inputs include the sleep mode enable(ZZ).

Output Enable controls the outputs at any given time.

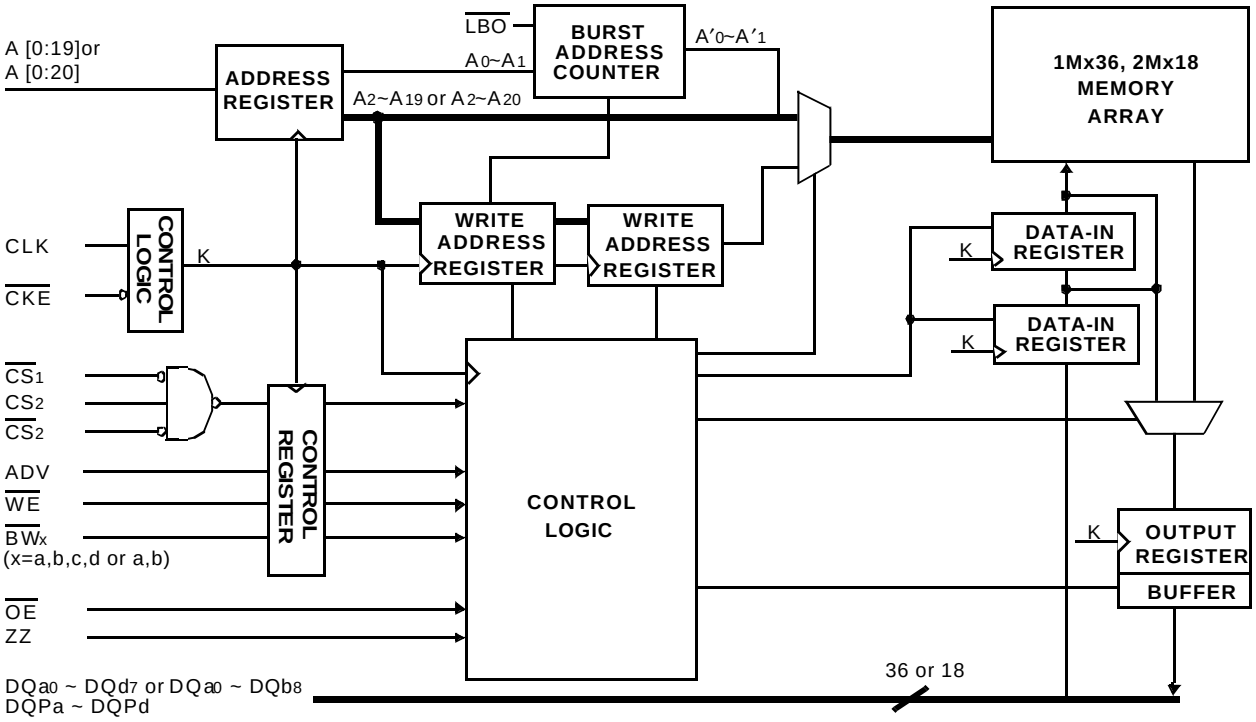
Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation

and provides increased timing flexibility for incoming signals.

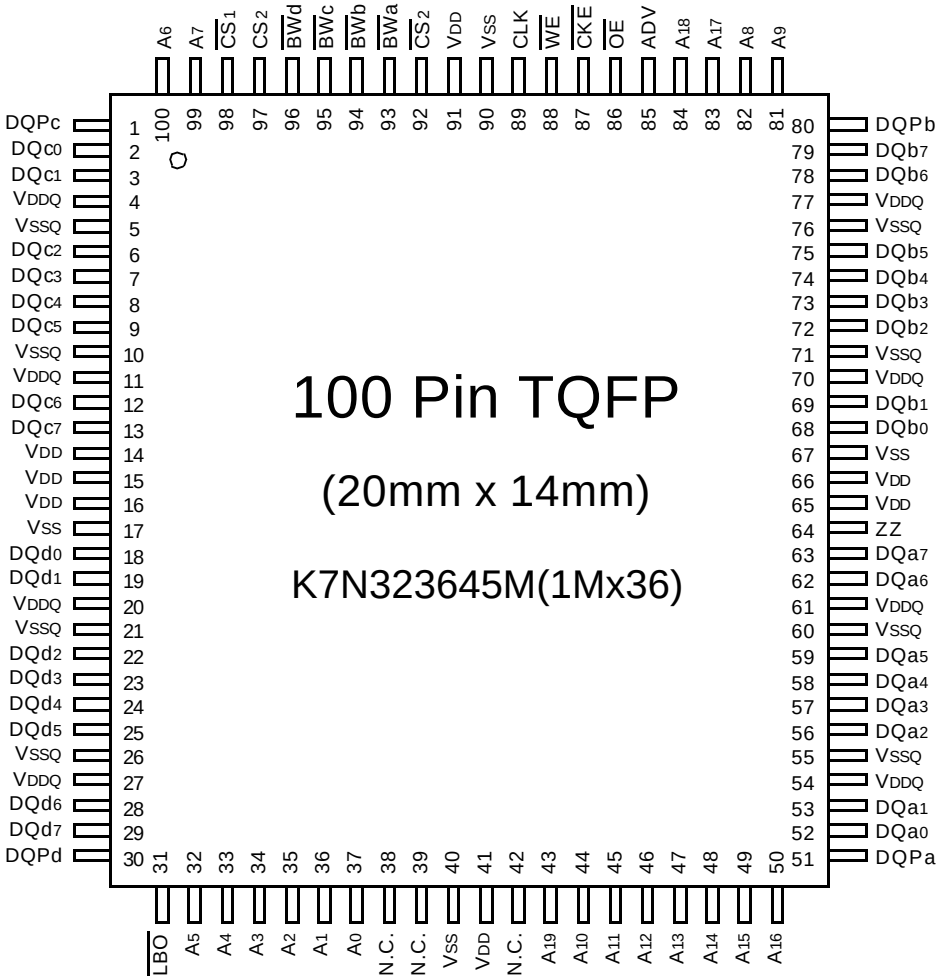
For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The K7N323645M and K7N321845M are implemented with SAMSUNG′s high performance CMOS technology and is available in 100pin TQFP and 165FBGA packages. Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

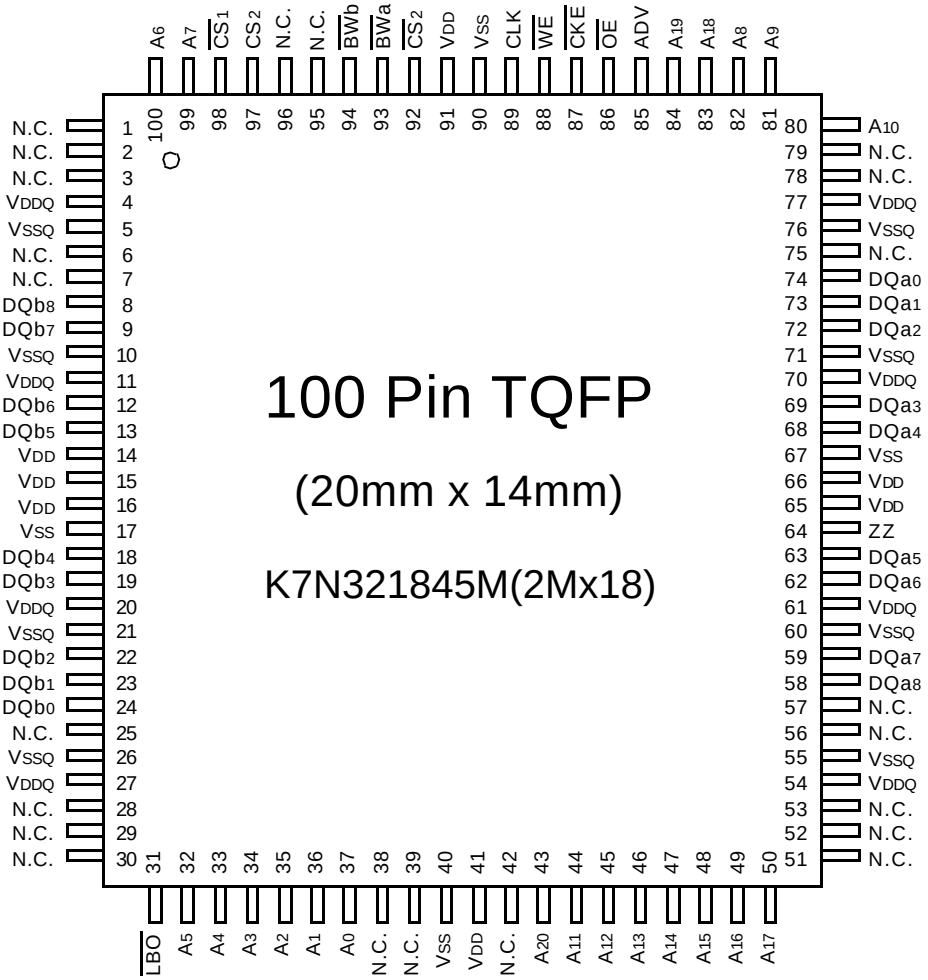


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,43, 44,45,46,47,48,49,50, 81,82,83,84,99,100	V_{DD}	Power Supply(2.5V)	14,15,16,41,65,66,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Address Advance/Load	85	N.C.	No Connect	38,39,42
$\overline{WE}$	Read/Write Control Input	88			
$\overline{CLK}$	Clock	89	$DQa_{0\sim a7}$	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{CKE}$	Clock Enable	87	$DQb_{0\sim b7}$	Data Inputs/Outputs	68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	$DQc_{0\sim c7}$	Data Inputs/Outputs	2,3,6,7,8,9,12,13
CS_2	Chip Select	97	$DQd_{0\sim d7}$	Data Inputs/Outputs	18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	$DQPa\sim Pd$	Data Inputs/Outputs	51,80,1,30
$\overline{BWx}$(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (2.5V)	4,11,20,27,54,61,70,77
$\overline{ZZ}$	Power Sleep Mode	64			
LBO	Burst Mode Control	31	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{20}	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50, 80,81,82,83,84,99,100	V_{DD}	Power Supply(2.5V)	14,15,16,41,65,66,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,25,28,29,30, 38,39,42,51,52,53, 56,57,75,78,79,95,96
$\overline{WE}$	Read/Write Control Input	88			
$\overline{CLK}$	Clock	89			
$\overline{CKE}$	Clock Enable	87			
$\overline{CS_1}$	Chip Select	98	$DQa_{0\sim a8}$	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CS_2	Chip Select	97	$DQb_{0\sim b8}$	Data Inputs/Outputs	8,9,12,13,18,19,22,23,24
$\overline{CS_2}$	Chip Select	92			
$\overline{BW}$x(x=a,b)	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (2.5V)	4,11,20,27,54,61,70,77
$\overline{ZZ}$	Power Sleep Mode	64			
$\overline{LBO}$	Burst Mode Control	31	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76

NOTE : A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

165-PIN FBGA PACKAGE CONFIGURATIONS(TOP VIEW)

K7N323645M(1Mx36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS}$1	$\overline{BW}$c	$\overline{BW}$b	$\overline{CS}$2	$\overline{CKE}$	ADV	A	A	NC
B	NC	A	CS2	$\overline{BW}$d	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	$\overline{LBO}$	A	A	A	TMS	A0*	TCK	A	A	A	A

Note : * A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
		VSS	Ground
A0,A1	Burst Address Inputs		
$\overline{ADV}$	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{CKE}$	Clock Enable	DQb	Data Inputs/Outputs
$\overline{CS}$1	Chip Select	DQc	Data Inputs/Outputs
CS2	Chip Select	DQd	Data Inputs/Outputs
$\overline{CS}$2	Chip Select	DQPa~Pd	Data Inputs/Outputs
$\overline{BW}$x	Byte Write Inputs		
(x=a,b,c,d)		VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

165-PIN FBGA PACKAGE CONFIGURATIONS(TOP VIEW)

K7N321845M(2Mx18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS}$1	$\overline{BW}$b	NC	$\overline{CS}$2	$\overline{CKE}$	ADV	A	A	A
B	NC	A	CS2	NC	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	$\overline{LBO}$	A	A	A	TMS	A0*	TCK	A	A	A	A

Note : * A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
		VSS	Ground
A0,A1	Burst Address Inputs		
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock		
$\overline{CKE}$	Clock Enable	DQa	Data Inputs/Outputs
$\overline{CS}$1	Chip Select	DQb	Data Inputs/Outputs
CS2	Chip Select	DQPa, Pb	Data Inputs/Outputs
$\overline{CS}$2	Chip Select		
$\overline{BW}$x (x=a,b)	Byte Write Inputs	VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
LBO	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7N323645M and K7N321845M are N*t*RAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

N*t*RAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS_1}$, CS_2, $\overline{CS_2}$) are active .
Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS_1}$, CS_2, $\overline{CS_2}$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[d:a] can be used for byte write operation. The pipe-lined N*t*RAM™ uses a late-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.
The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.
And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$=High)

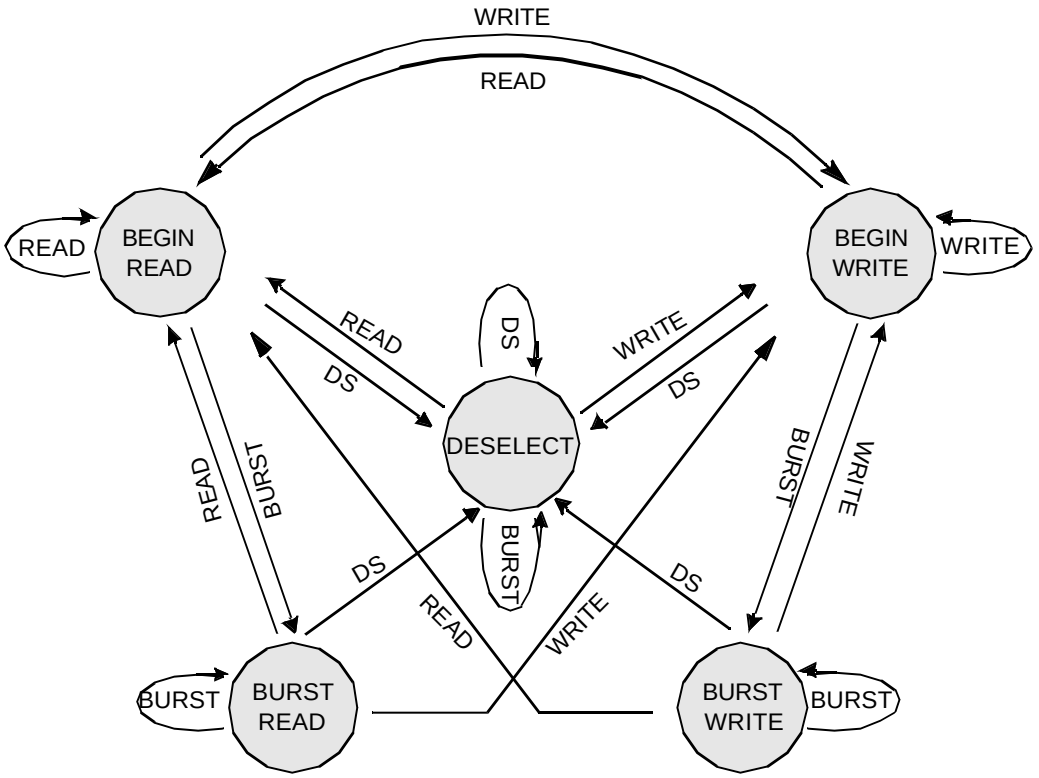
$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$=Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR N*t*RAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown is the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	ADV	$\overline{WE}$	$\overline{BW}x$	$\overline{OE}$	$\overline{CKE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).

3. A continue deselect cycle can only be enterd if a deselect cycle is executed first.

4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{WE}$	$\overline{BW}a$	$\overline{BW}b$	$\overline{BW}c$	$\overline{BW}d$	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{WE}$	$\overline{BW}a$	$\overline{BW}b$	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTEs
L	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 3.6	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	1.6	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Note** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	2.375	2.5	2.625	V
	V_{DDQ}	2.375	2.5	2.625	V
Ground	V_{SS}	0	0	0	V

***Note** : V_{DD} and V_{DDQ} must be supplied with identical vlotage levels.

CAPACITANCE*(T_A=25°C, f=1MHz)

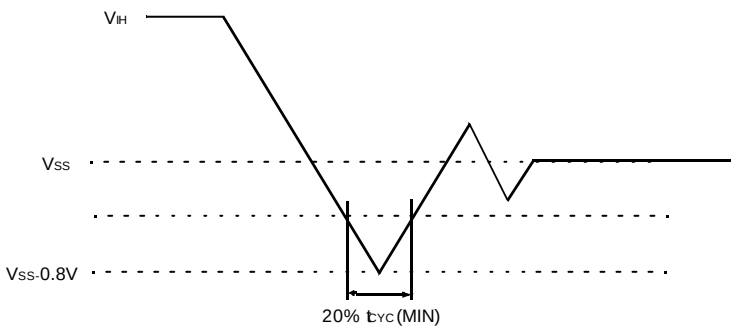
PARAMETER	SYMBOL	TEST CONDITION	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***Note** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS (V_{DD}=2.5V ±5%, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	µA	
Operating Current	I_{CC}	V_{DD}=Max I_{OUT}=0mA Cycle Time ≥ t_{CYC} Min	-25	-	460	mA	1,2
			-20	-	410		
			-16	-	360		
			-13	-	310		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-25	-	170	mA	
			-20	-	150		
			-16	-	140		
			-13	-	140		
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	110	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	100	mA	
Output Low Voltage	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage	V_{IL}			-0.3*	0.7	V	
Input High Voltage	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ} +0.3V

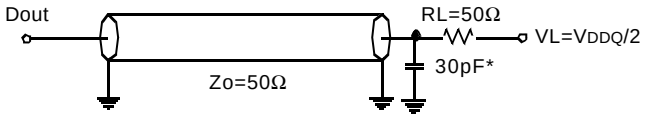


TEST CONDITIONS

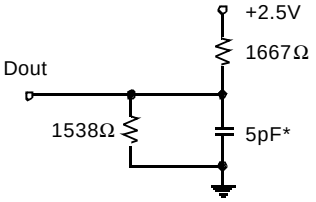
(T_A=0 to 70°C, V_{DD}=2.5V ±5%, unless otherwise specified)

PARAMETER	VALUE
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



Output Load(B),
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=2.5V ±5%, T_A=0 to 70°C)

PARAMETER	SYMBOL	-25		-20		-16		-13		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	4.0	-	5.0	-	6.0	-	7.5	-	ns
Clock Access Time	tCD	-	2.6	-	3.2	-	3.5	-	4.2	ns
Output Enable to Data Valid	tOE	-	2.6	-	3.2	-	3.5	-	4.2	ns
Clock High to Output Low-Z	tLZC	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	2.6	-	3.0	-	3.0	-	3.5	ns
Clock High to Output High-Z	tHZC	-	2.6	-	3.0	-	3.0	-	3.5	ns
Clock High Pulse Width	tCH	1.7	-	2.0	-	2.2	-	3.0	-	ns
Clock Low Pulse Width	tCL	1.7	-	2.0	-	2.2	-	3.0	-	ns
Address Setup to Clock High	tAS	1.2	-	1.4	-	1.5	-	1.5	-	ns
$\overline{CKE}$ Setup to Clock High	tCES	1.2	-	1.4	-	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.2	-	1.4	-	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BW}$x)	tWS	1.2	-	1.4	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.2	-	1.4	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.2	-	1.4	-	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.3	-	0.4	-	0.5	-	0.5	-	ns
$\overline{CKE}$ Hold from Clock High	tCEH	0.3	-	0.4	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.3	-	0.4	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BW}$x)	tWH	0.3	-	0.4	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.3	-	0.4	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.3	-	0.4	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature tLZC is more than tHZC.
The specs as shown do not imply bus contention because tLZC is a Min. parameter that is worst case at totally different test conditions (0°C,2.625V) than tHZC, which is a Max. parameter(worst case at 70°C,2.375V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

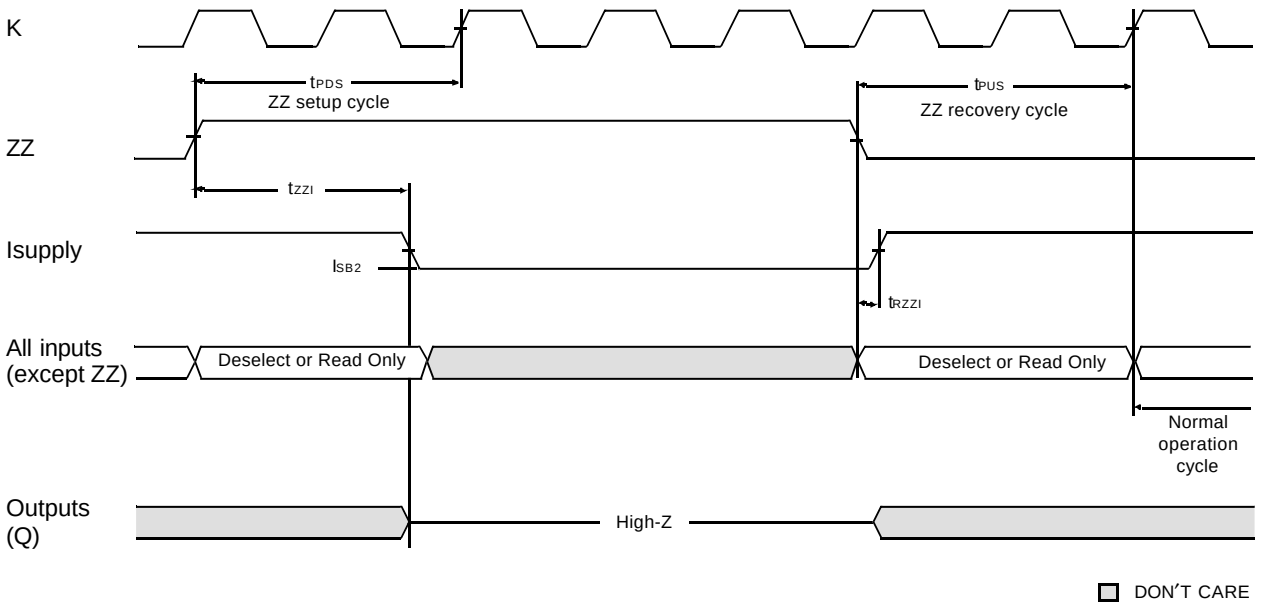
SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.
After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.
When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. similarly, when exiting SLEEP MODE during t_{PUS}, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	ZZ ≥ V_{IH}	I_{SB2}		60	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

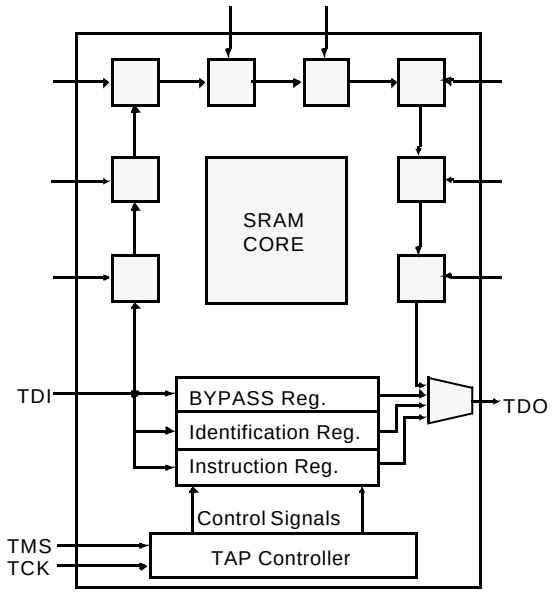
SLEEP MODE WAVEFORM



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



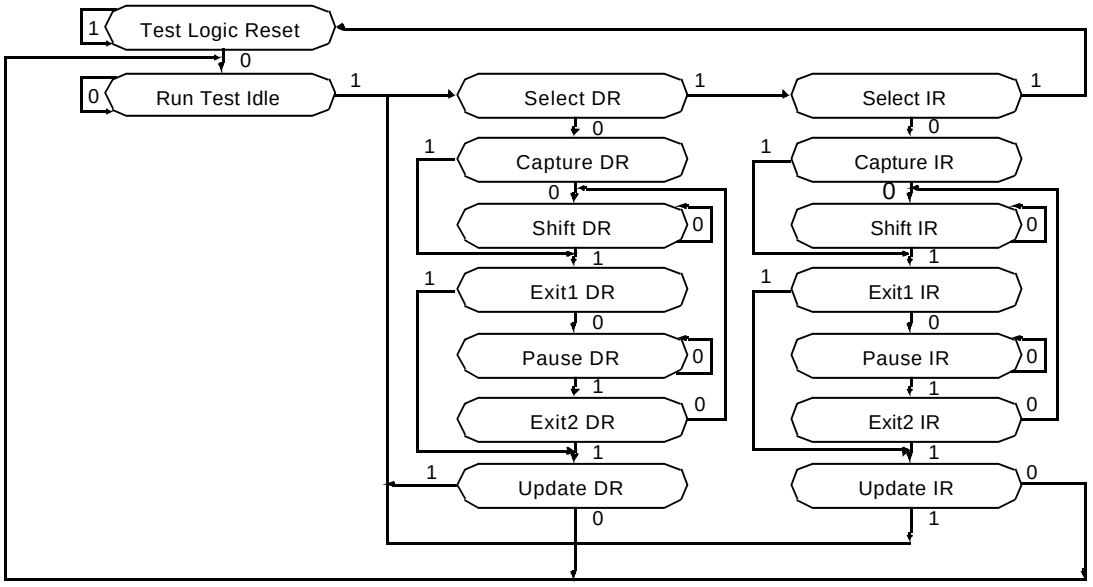
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



SCAN INFORMATION (165 FBGA)

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1Mx36	3 bits	1 bits	32 bits	76 bits
2Mx18	3 bits	1 bits	32 bits	76 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
1Mx36	0000	01000 00100	XXXXXX	00001001110	1
2Mx18	0000	01001 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER

BIT	PIN ID(x18)	PIN ID(x36)
1	6N	6N
2	8P	8P
3	8R	8R
4	9R	9R
5	9P	9P
6	10P	10P
7	10R	10R
8	11R	11R
9	11P	11P
10	11H	11H
11	11N	11N
12	11M	11M
13	11L	11L
14	11K	11K
15	11J	11J
16	10M	10M
17	10L	10L
18	10K	10K
19	10J	10J
20	11G	11G
21	11F	11F
22	11E	11E
23	11D	11D
24	11C	10G
25	10F	10F
26	10E	10E
27	10D	10D
28	10G	11C
29	11A	11A
30	11B	11B
31	10A	10A
32	10B	10B
33	9A	9A
34	9B	9B
35	8A	8A
36	8B	8B
37	7A	7A
38	7B	7B
39	6B	6B

BIT	PIN ID(x18)	PIN ID(x36)
40	6A	6A
41	5B	5B
42	5A	5A
43	4A	4A
44	4B	4B
45	3B	3B
46	3A	3A
47	2A	2A
48	2B	2B
49	1B	1B
50	1A	1A
51	1C	1C
52	1D	1D
53	1E	1E
54	1F	1F
55	1G	1G
56	2D	2D
57	2E	2E
58	2F	2F
59	2G	2G
60	1J	1J
61	1K	1K
62	1L	1L
63	1M	1M
64	1N	2J
65	2K	2K
66	2L	2L
67	2M	2M
68	2J	1N
69	2R	2R
70	1R	1R
71	3P	3P
72	3R	3R
73	4R	4R
74	4P	4P
75	6P	6P
76	6R	6R

Note: 1. NC and Vss pins included in the scan exit order are read as "X" (i.e. don't care).

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.135	3.3	3.465	V	
Input High Level	V_{IH}	1.7	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.7	V	
Output High Voltage	V_{OH}	2.0	-	-	V	
Output Low Voltage	V_{OL}	-	-	0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

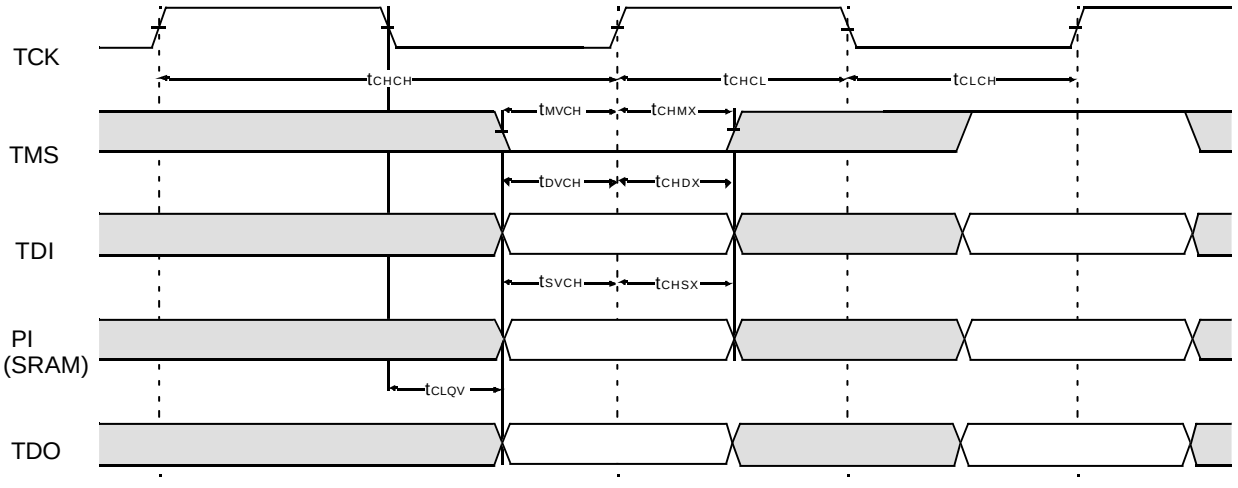
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	2.5/0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		$V_{DDQ}/2$	V	

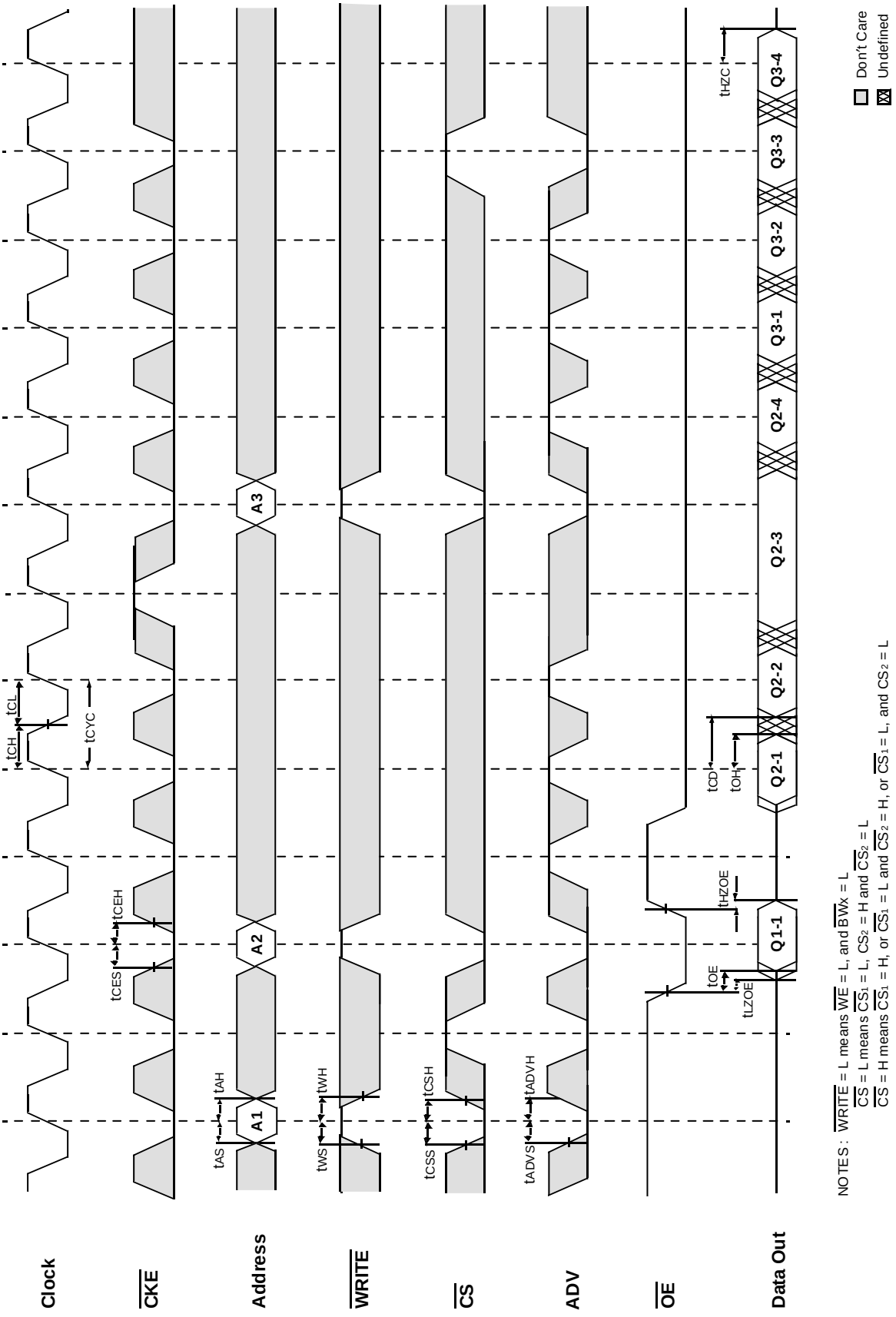
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM

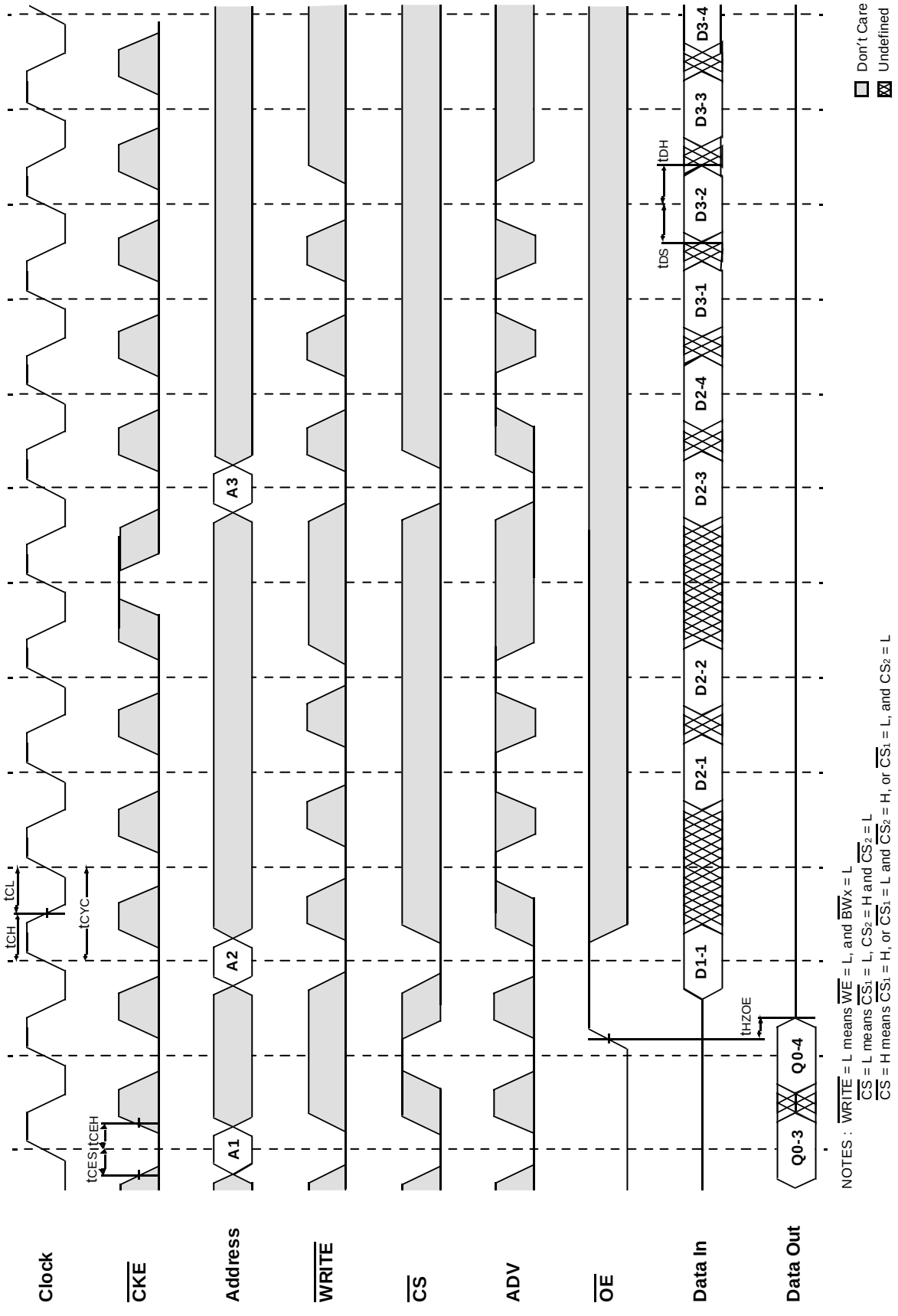


TIMING WAVEFORM OF READ CYCLE

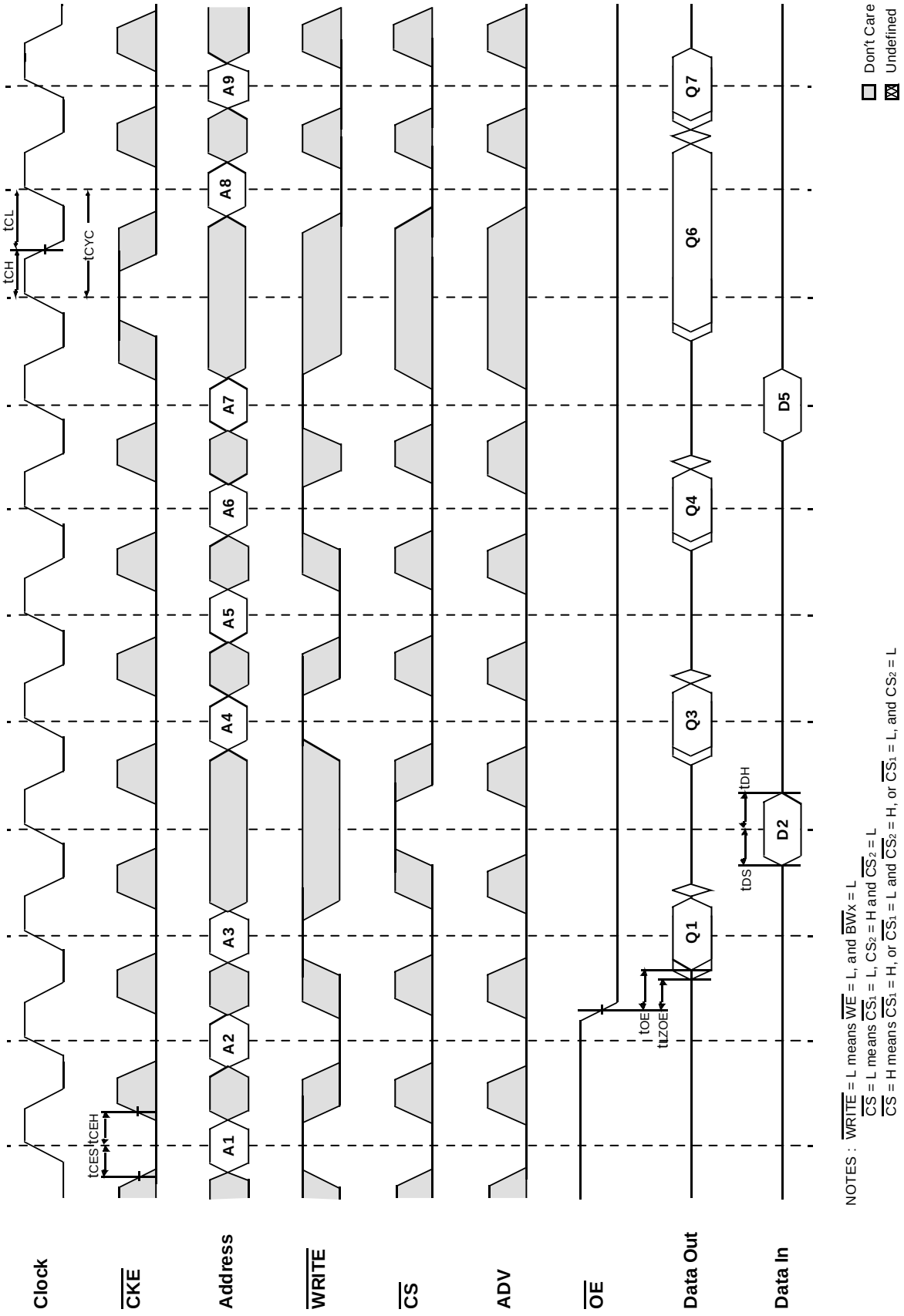


NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

TIMING WAVEFORM OF WRTE CYCLE

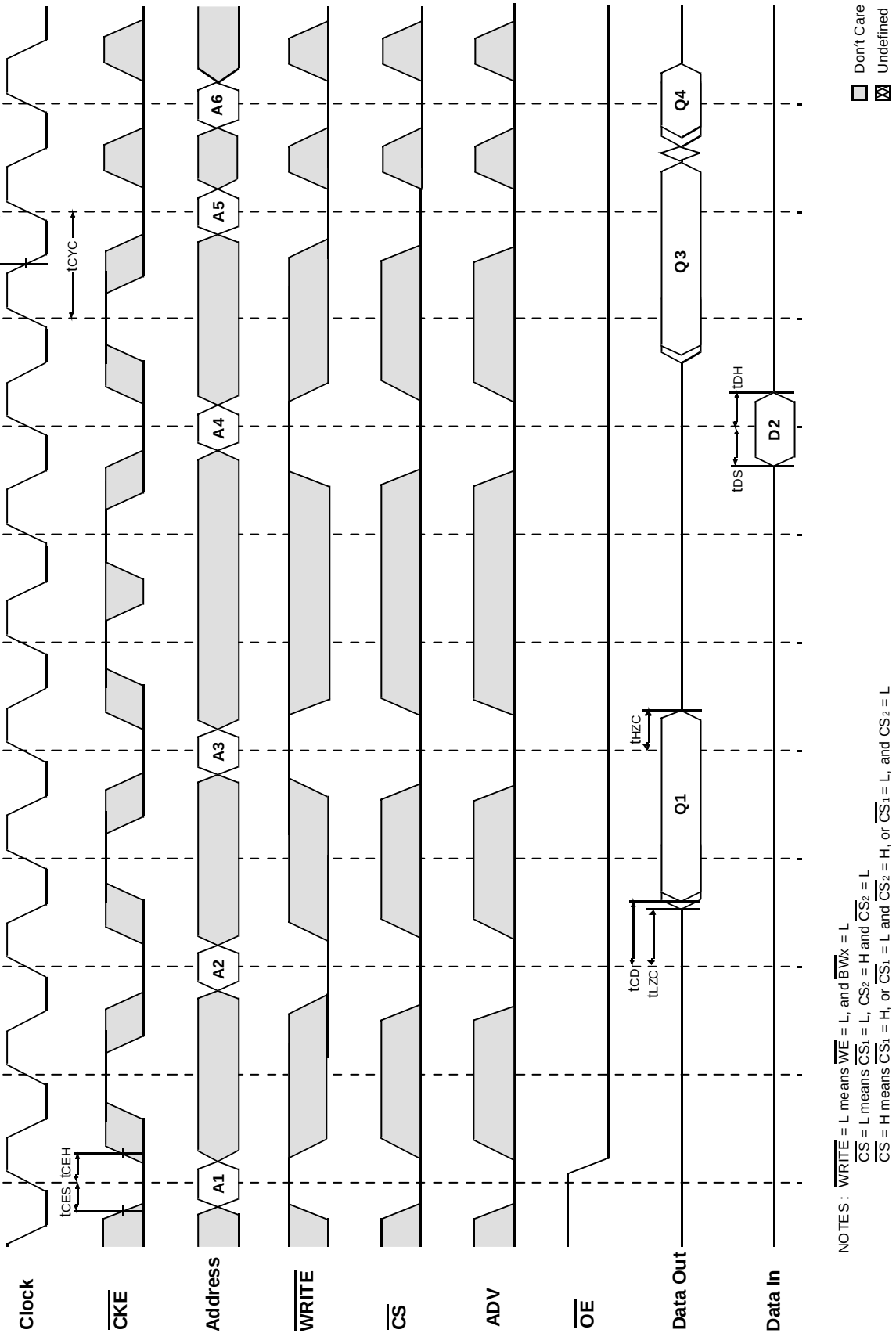


TIMING WAVEFORM OF SINGLE READ/WRITE



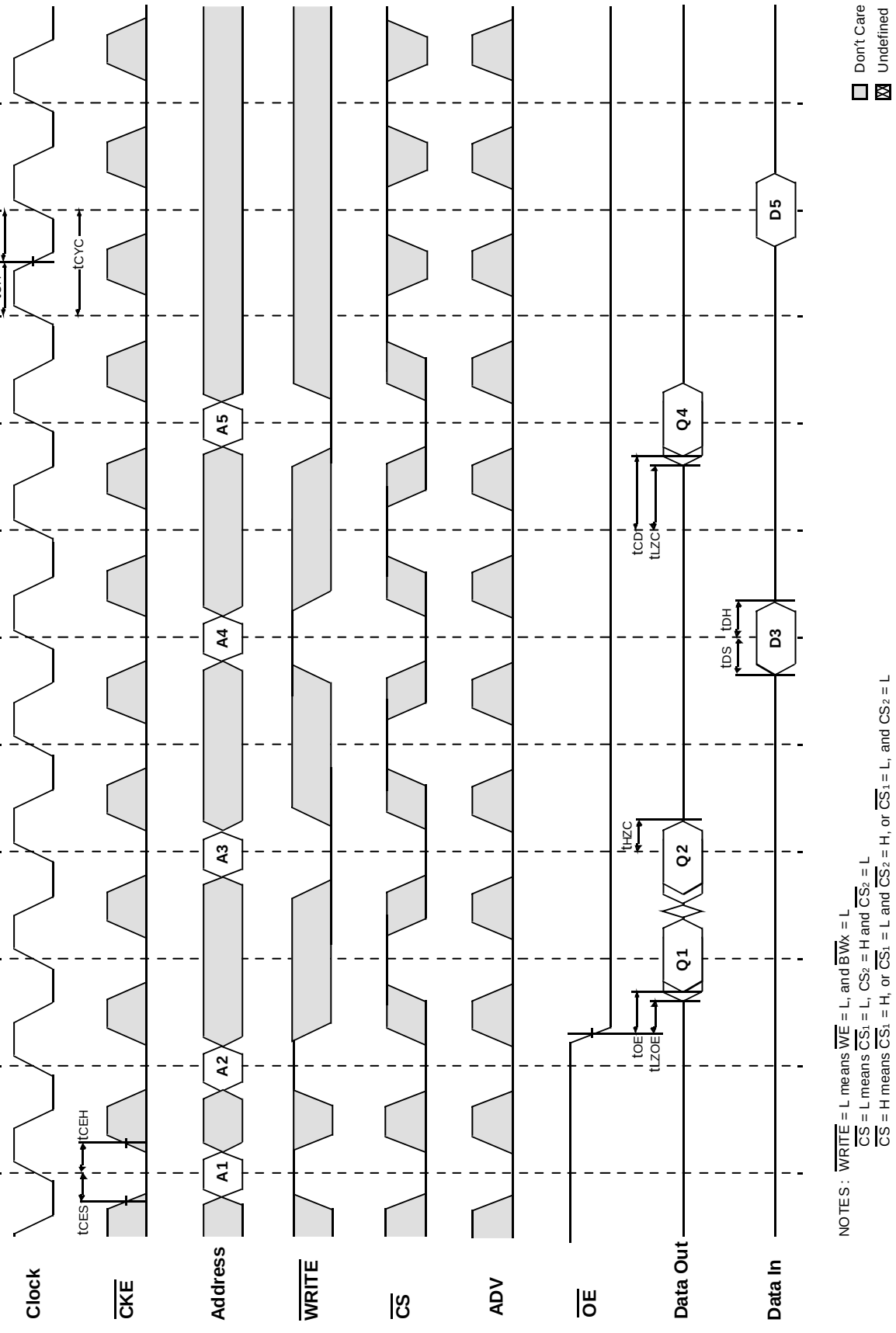
NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

TIMING WAVEFORM OF $\overline{CKE}$ OPERATION



NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $\overline{CS_2}$ = L

TIMING WAVEFORM OF $\overline{CS}$ OPERATION

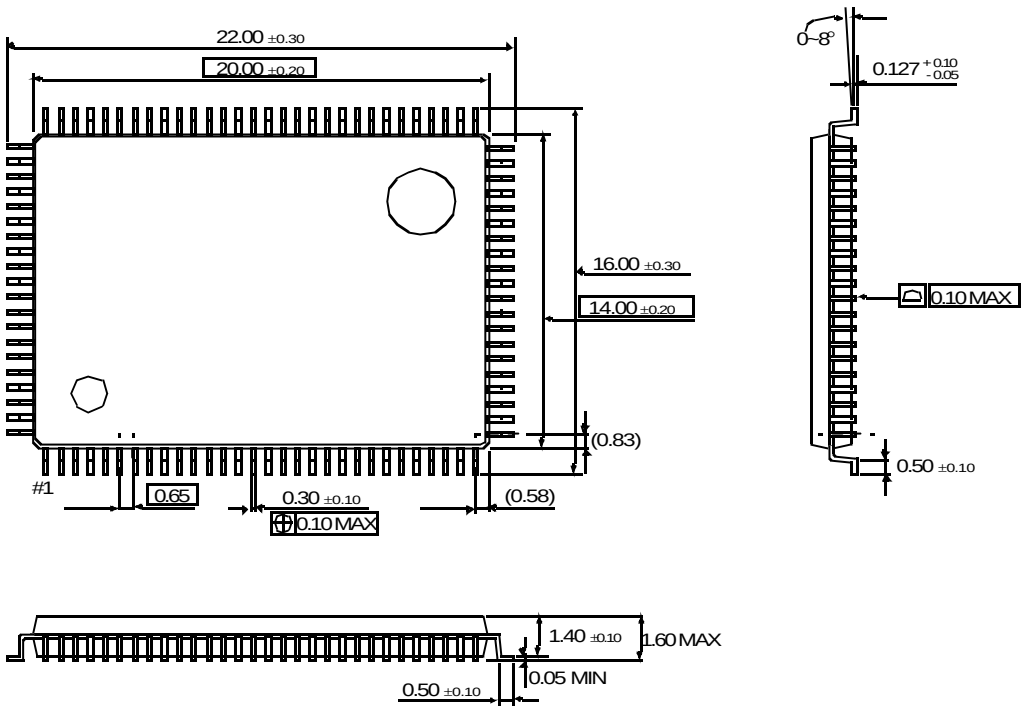


NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $\overline{CS_2}$ = L

PACKAGE DIMENSIONS

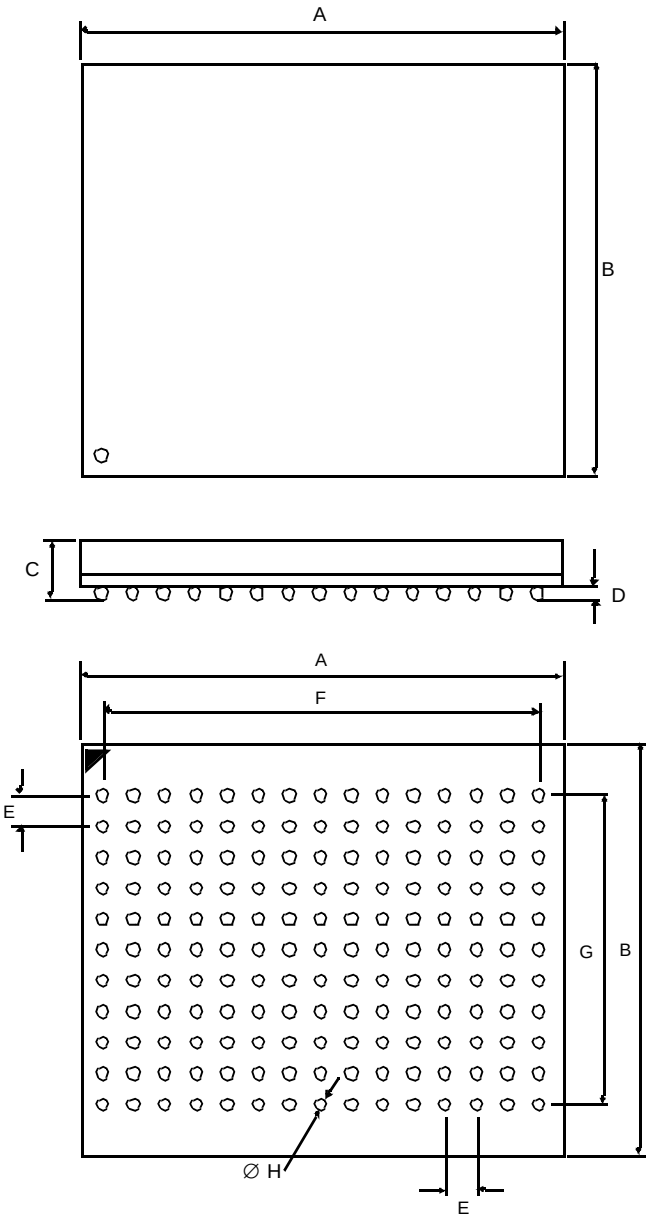
100-TQFP-1420A

Units ; millimeters/Inches



165 FBGA PACKAGE DIMENSIONS

15mm x 17mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Top View

Side View

Bottom View

Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	17 ± 0.1	mm		**E**	1.0	mm	
B	15 ± 0.1	mm		**F**	14.0	mm	
C	1.3 ± 0.1	mm		**G**	10.0	mm	
D	0.35 ± 0.05	mm		**H**	0.5 ± 0.05	mm	