Document Title

128Kx36 & 128Kx32-Bit Synchronous Pipelined Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial draft	May. 15. 2001	Preliminary
0.1	1. Changed DC parameters Icc ; from 350mA to 290mA at -16, from 330mA to 270mA at -15, from 300mA to 250mA at -14, I_{SB1} ; from 100mA to 80mA	June. 12. 2001	Preliminary
0.2	1 Delete Pass-Through	June. 25. 2001	Preliminary
0.3	1. Add x32 org and industrial temperature	Agu. 11. 2001	Preliminary

4Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
256Kx18	K7B401825B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns	Q (100TQFP)	C (Commercial Temperature Range) I: (Industrial Temperature Range)
	K7A401800B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A401809B-QC(I)30/27/25/22/20	SPB(2E1D)	3.3	300/275/250/225/200 MHz		
128Kx32	K7B403225B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns		
	K7A403200B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A403209B-QC(I)30/27/25/22/20	SPB(2E1D)	3.3	300/275/250/225/200 MHz		
	K7A403201B-QC(I)16/14	SPB(2E2D)	3.3	167/138/ MHz		
128Kx36	K7B403625B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns		
	K7A403600B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A403609B-QC(I)30/27/25/22/20	SPB(2E1D)	3.3	300/275/250/225/200 MHz		
	K7A403601B-QC(I)16/14	SPB(2E2D)	3.3	167/138 MHz		

128Kx36 & 128Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V+0.3V/-0.165V Power Supply.
- V_{DDQ} Supply Voltage 3.3V+0.3V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 2cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A
- Operating in commeical and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-16	-14	Unit
Cycle Time	t_{CYC}	6.0	7.2	ns
Clock Access Time	t_{CD}	3.5	4.0	ns
Output Enable Access Time	t_{OE}	3.5	4.0	ns

GENERAL DESCRIPTION

The K7A403601B and K7A403201B are a 4,718,592-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 128K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with CS1 high, ADSP is blocked to control signals.

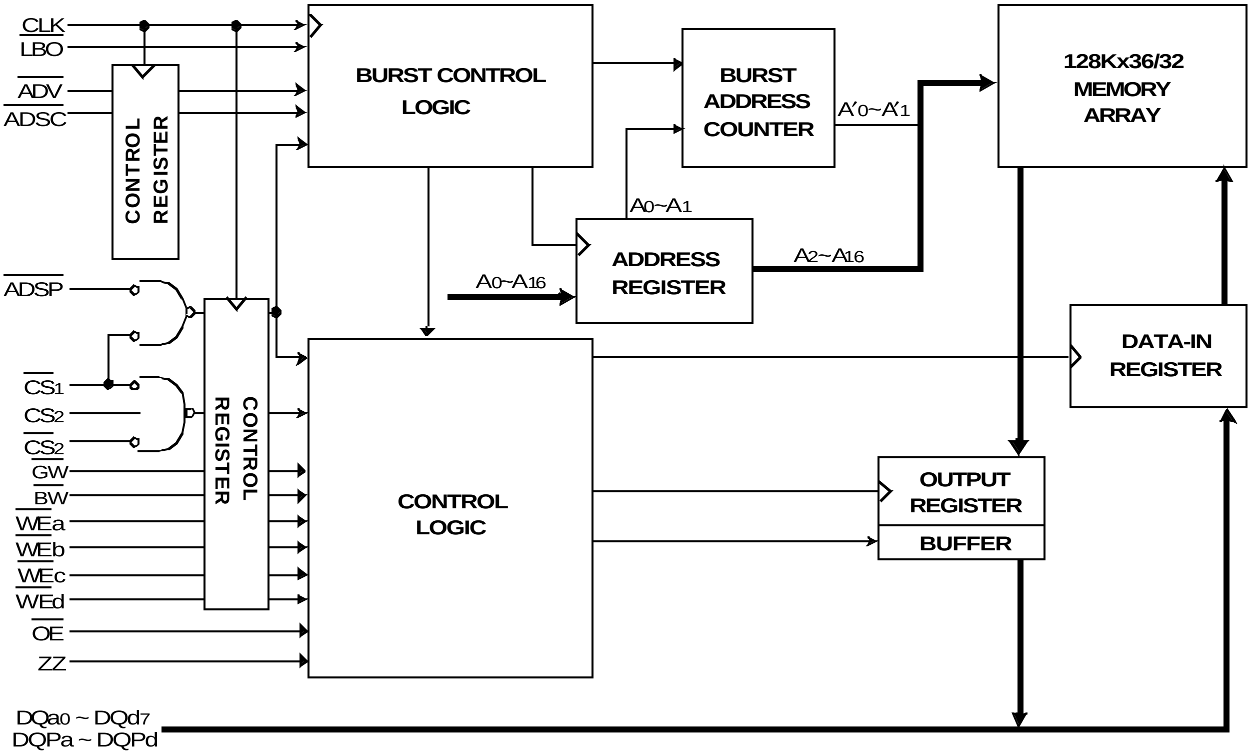
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system′s burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

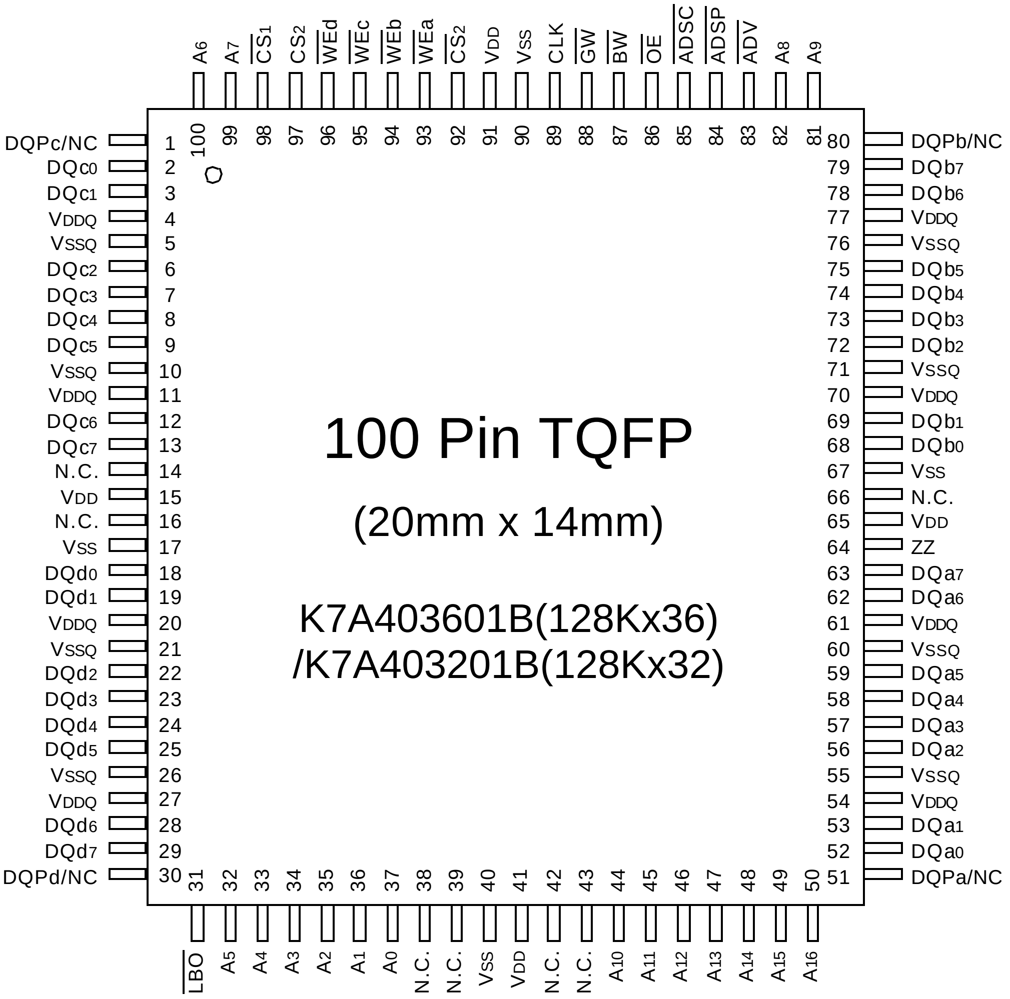
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A403601B and K7A403201B are fabricated using SAMSUNG′s high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{16}	Address Inputs	32,33,34,35,36,37,	V_{DD}	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,49,	V_{SS}	Ground	17,40,67,90
		50,81,82,99,100	N.C.	No Connect	14,16,38,39,42,43,66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0~b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
$\overline{CS_1}$	Chip Select	98	DQd0~d7		18,19,22,23,24,25,28,29
CS_2	Chip Select	97	DQPa~Pd		51,80,1,30
$\overline{CS_2}$	Chip Select	92	/NC		
$\overline{WE}x$	Byte Write Inputs	93,94,95,96	V_{DDQ}	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86		(2.5V or 3.3V)	
$\overline{GW}$	Global Write Enable	88	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The K7A4036/3201B are synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP(regardless of WEx and ADSC)using the new external address clocked into the on-chip address register whenever ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when WEx are sampled High and ADV is sampled low. And ADSP is blocked to control signals by disabling CS1.

All byte write is done by GW(regaedless of BW and WEx.), and each byte write is performed by the combination of BW and WEx when GW is high.
Write cycles are performed by disabling the output buffers with OE and asserting WEx. WEx are ignored on the clock edge that samples ADSP low, but are sampled on the subsequent clock edges. The output buffers are disabled when WEx are sampled Low(regaedless of OE). Data is clocked into the data input register when WEx sampled Low. The address increases internally to the next address of burst, if both WEx and ADV are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(WEa, WEb, WEc or WEd) sampled low. The WEa control DQa0 ~ DQa7 and DQPa, WEb controls DQb0 ~ DQb7 and DQPb, WEc controls DQc0 ~ DQc7 and DQPc, and WEd control DQd0 ~ DQd7 and DQPd. Read or write cycle may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSC and ADSP as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.
WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{\text{CS}}_1$	CS_2	$\overline{\text{CS}}_2$	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don′t Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{\text{WRITE}}$ = L means Write operation in WRITE TRUTH TABLE.
$\overline{\text{WRITE}}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{\text{OE}}$).

WRITE TRUTH TABLE

$\overline{\text{GW}}$	$\overline{\text{BW}}$	$\overline{\text{WE}}\text{a}$	$\overline{\text{WE}}\text{b}$	$\overline{\text{WE}}\text{c}$	$\overline{\text{WE}}\text{d}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don′t Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	ZZ	$\overline{\text{OE}}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don′t Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{\text{OE}}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}		V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation		P_D	2.2	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

***Note :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C≤ T_A≤70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	3.135	3.3	3.6	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE**: Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(TA=0 to 70°C, VDD=3.3V+0.3V/-0.165V)

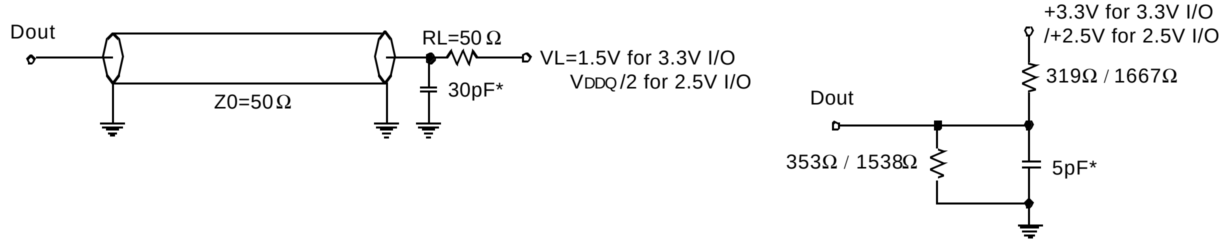
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Input Leakage Current(except ZZ)	IIL	VDD = Max ; VIN=VSS to VDD		-2	+2	µA
Output Leakage Current	IOL	Output Disabled, VOUT=VSS to VDDQ		-2	+2	µA
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ≤VIL, All Inputs=VIL or VIH	-16	-	290	mA
			-14	-	250	
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-16	-	140	mA
			-14	-	120	
	ISB1	Device deselected, IOUT=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (VDD-0.2V or 0.2V)		-	80	mA
	ISB2	Device deselected, IOUT=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH		-	50	mA
Output Low Voltage(3.3V I/O)	VOL	IOL = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	VOH	IOH = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	VOL	IOL = 1.0mA		-	0.4	V
Output High Voltage(2.5V I/O)	VOH	IOH = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	VIL			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	VIH			2.0	VDD+0.3**	V
Input Low Voltage(2.5V I/O)	VIL			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	VIH			1.7	VDD+0.3**	V

* VIL(Min)=-2.0(Pulse Width ≤ tCYC/2)
** VIH(Max)=4.6(Pulse Width ≤ tCYC/2)
** In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

TEST CONDITIONS

(VDD=3.3V+0.3V/-0.165V,VDDQ=3.3V+0.3/-0.165V or VDD=3.3V+0.3V/-0.165V,VDDQ=2.5V+0.4V/-0.125V, TA=0 to 70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	1ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	1ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1


Output Load(A)

Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})

* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

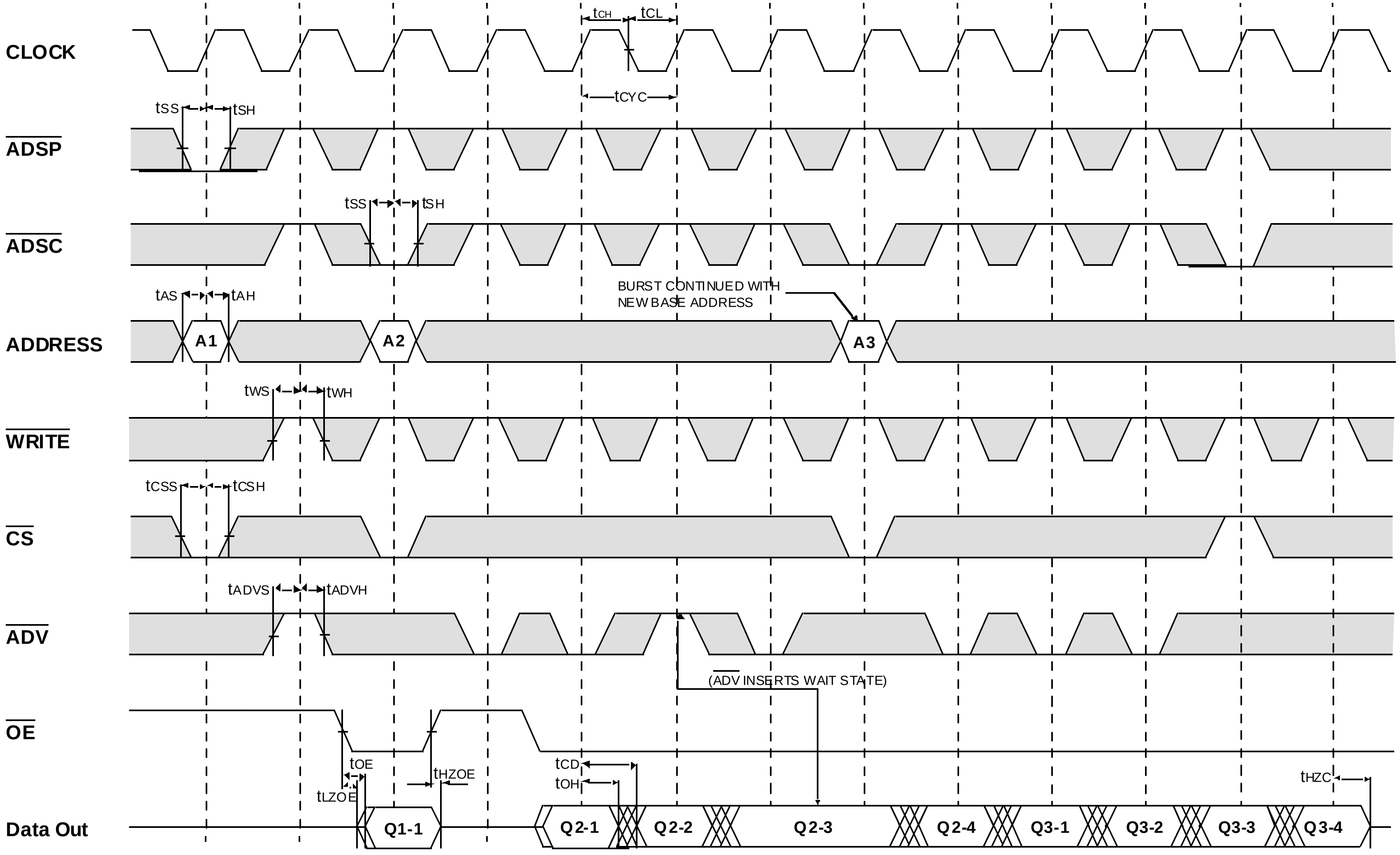
Fig. 1

AC TIMING CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.3V/-0.165V)

Parameter	Symbol	-16		-14		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	6.0	-	7.2	-	ns
Clock Access Time	t_{CD}	-	3.5	-	4.0	ns
Output Enable to Data Valid	t_{OE}	-	3.5	-	4.0	ns
Clock High to Output Low-Z	t_{LZC}	0	-	0	-	ns
Output Hold from Clock High	t_{OH}	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	-	4.0	ns
Clock High to Output High-Z	t_{HZC}	1.5	3.5	1.5	4.0	ns
Clock High Pulse Width	t_{CH}	2.4	-	2.8	-	ns
Clock Low Pulse Width	t_{CL}	2.4	-	2.8	-	ns
Address Setup to Clock High	t_{AS}	1.5	-	1.5	-	ns
Address Status Setup to Clock High	t_{SS}	1.5	-	1.5	-	ns
Data Setup to Clock High	t_{DS}	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}_x$)	t_{WS}	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t_{ADVS}	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	1.5	-	1.5	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}_x$)	t_{WH}	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.
4. At any given voltage and temperature, t_{HZC} is less than t_{LZC}

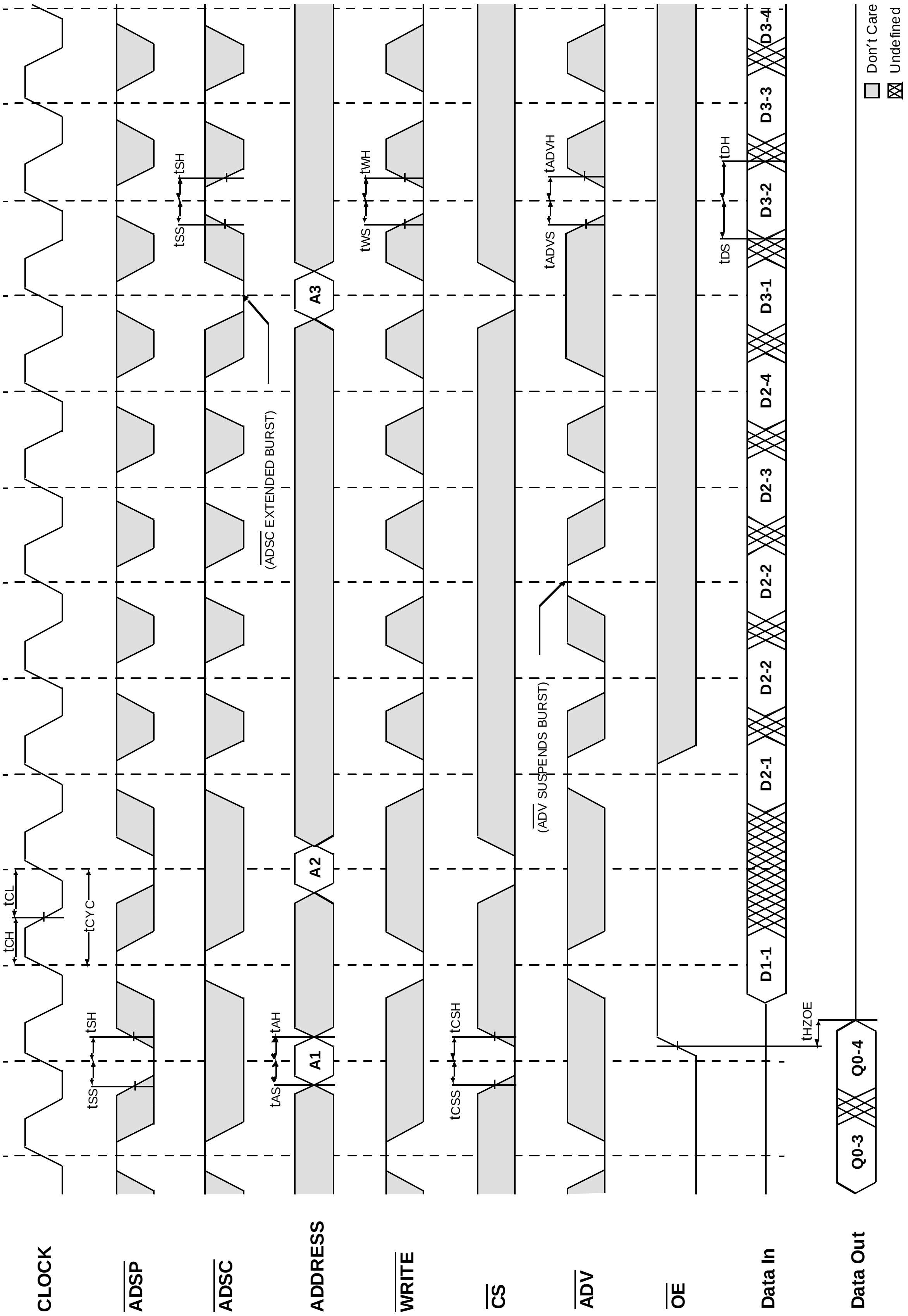
TIMING WAVEFORM OF READ CYCLE



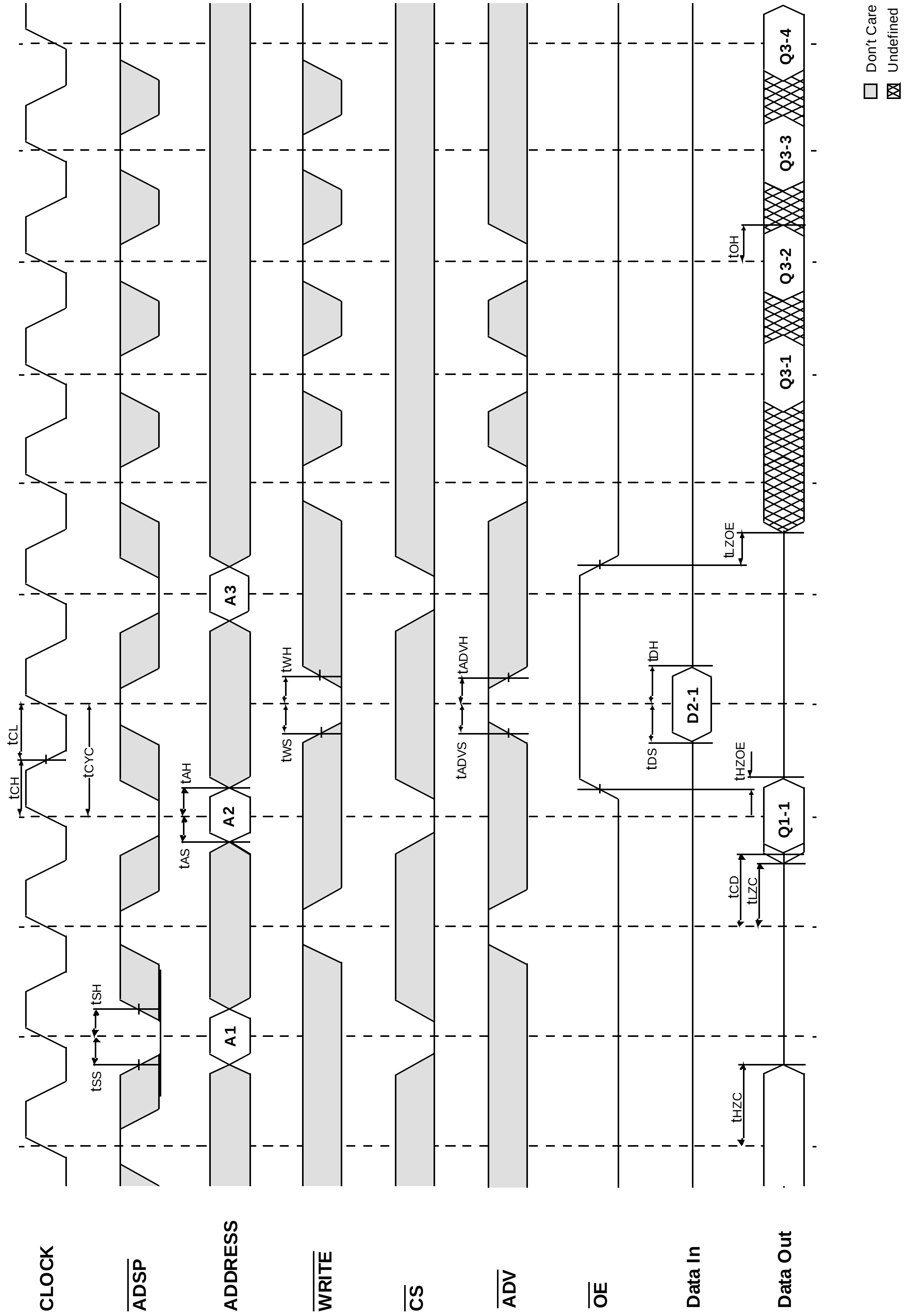
NOTES : $\overline{\text{WRITE}}$ = L means $\overline{\text{GW}}$ = L, or $\overline{\text{GW}}$ = H, $\overline{\text{BW}}$ = L, $\overline{\text{WE}}_x$ = L
$\overline{\text{CS}}$ = L means $\overline{\text{CS}}_1$ = L, CS_2 = H and $\overline{\text{CS2}}$ = L
$\overline{\text{CS}}$ = H means $\overline{\text{CS}}_1$ = H, or $\overline{\text{CS}}_1$ = L and $\overline{\text{CS}}_2$ = H, or $\overline{\text{CS}}_1$ = L, and CS_2 = L

☐ Don't Care
☒ Undefined

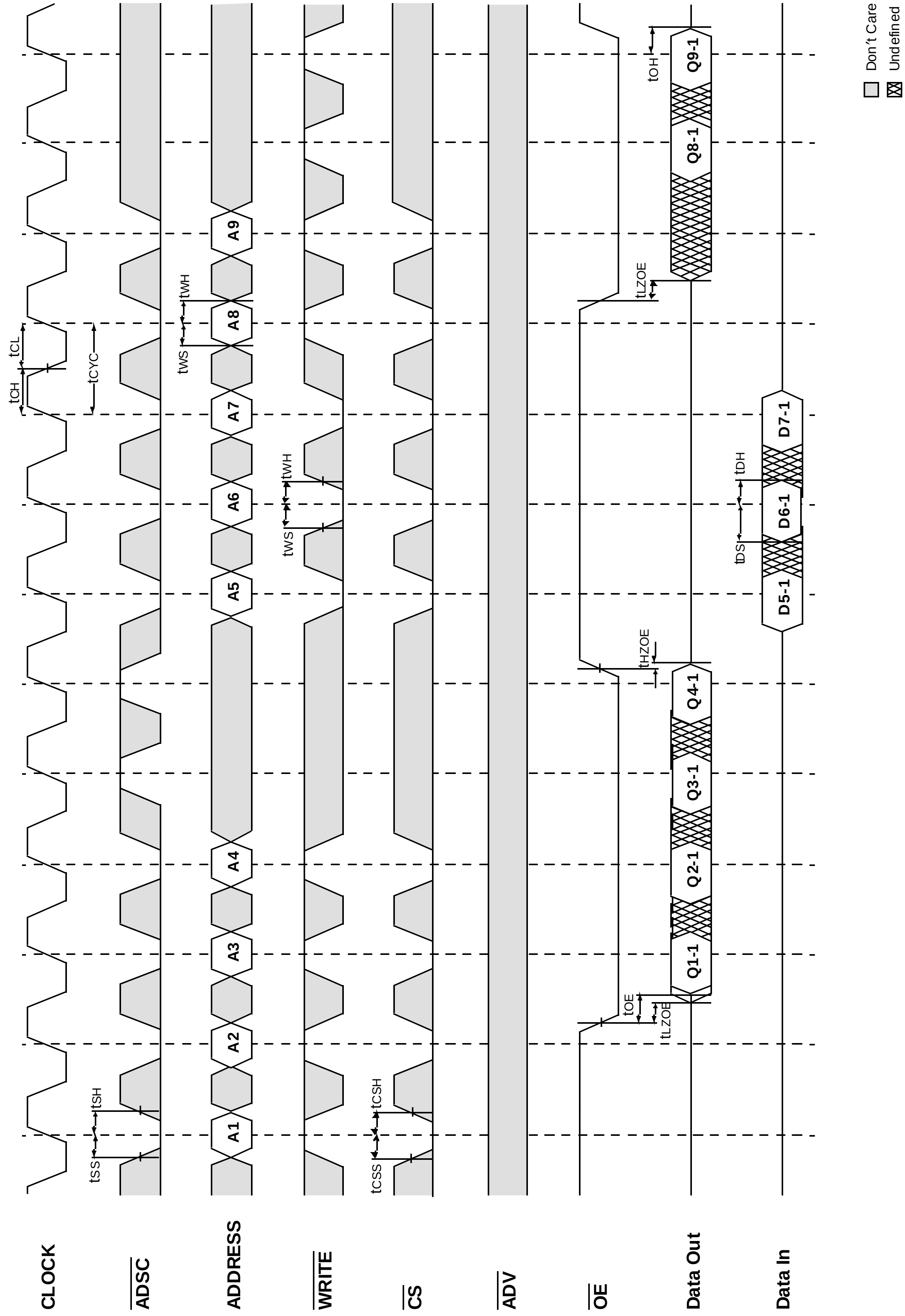
TIMING WAVEFORM OF WRTE CYCLE



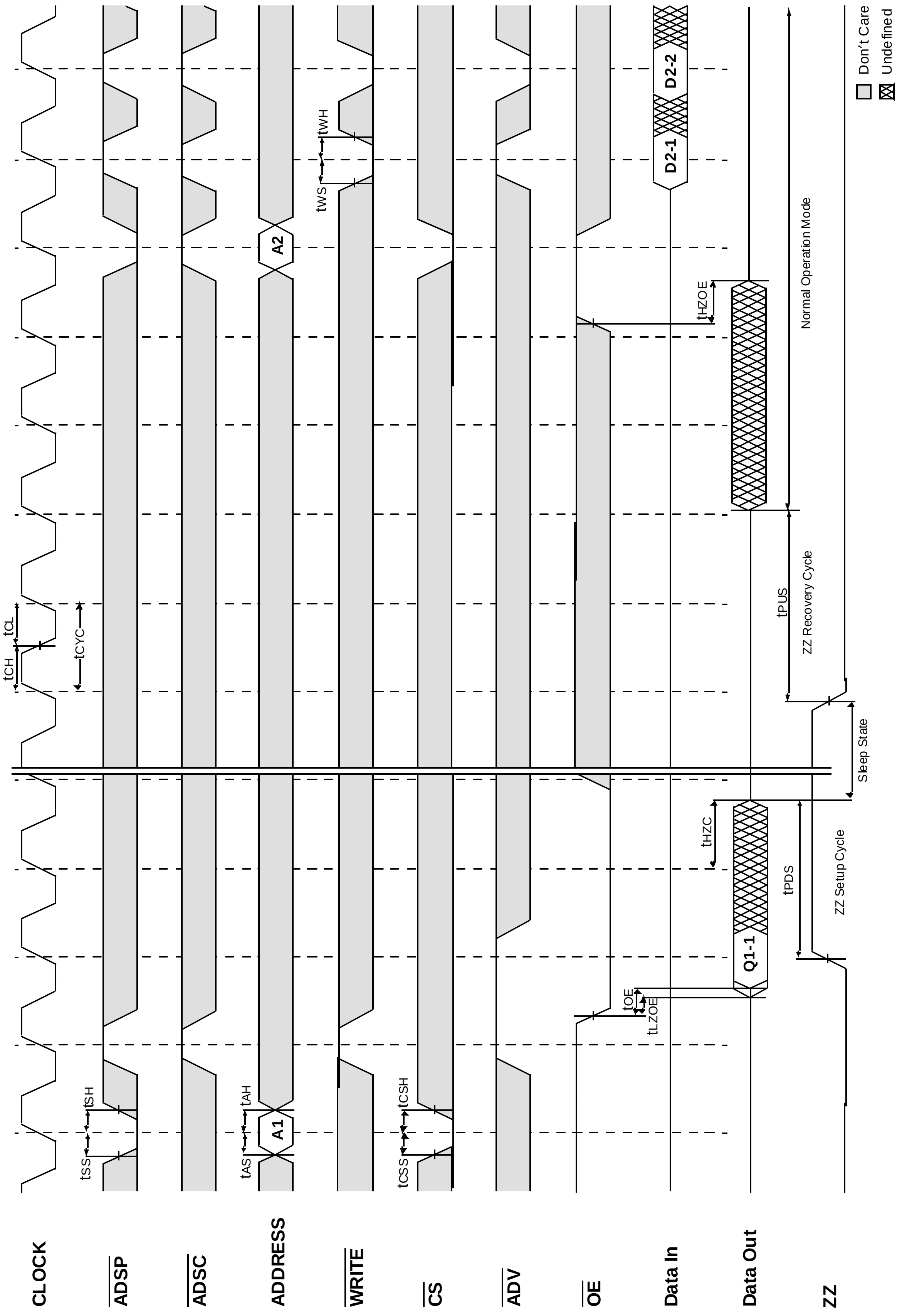
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED , ADSC=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED , ADSP=HIGH)



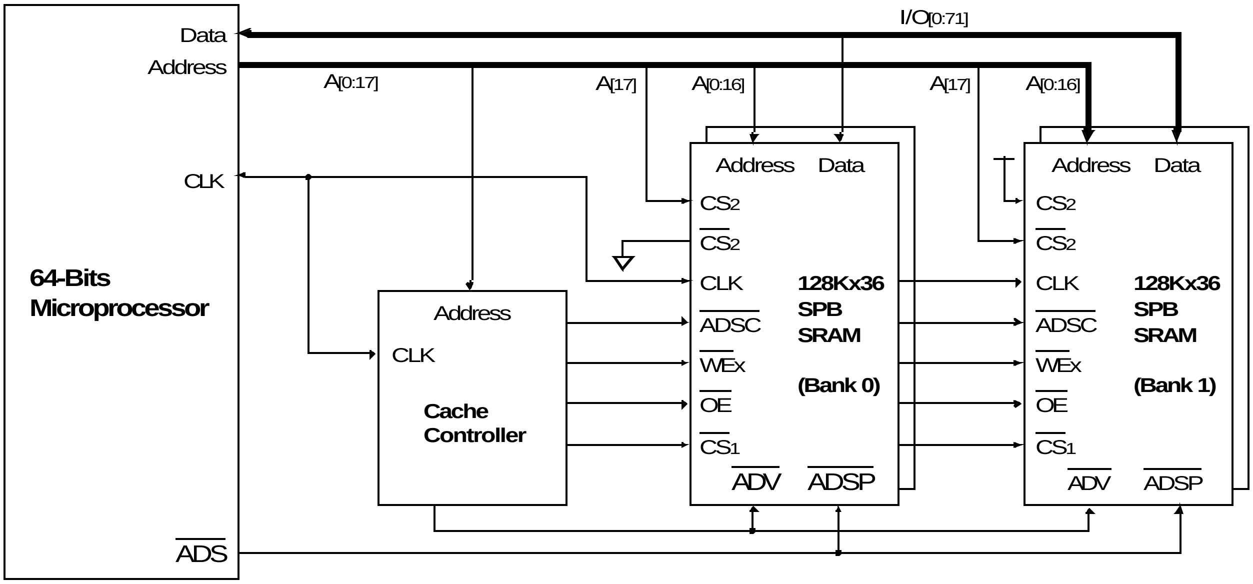
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

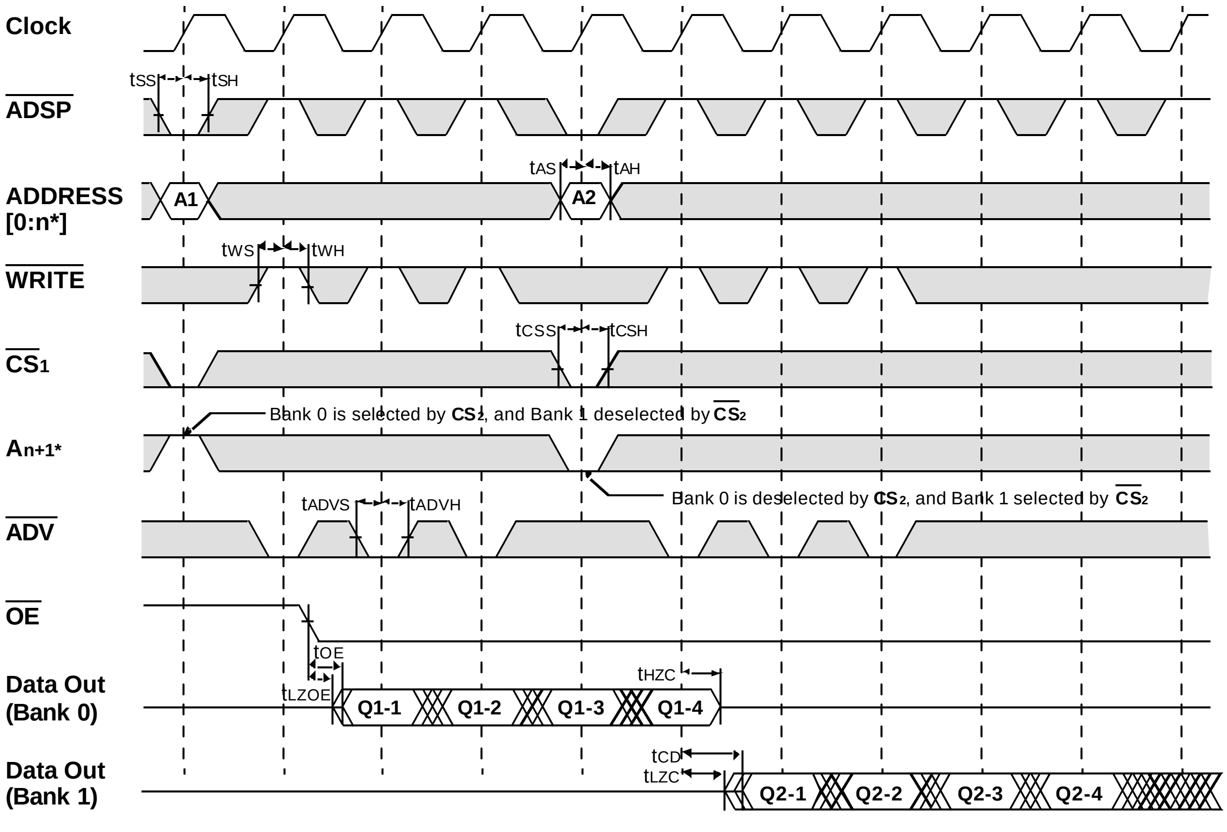
DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{\text{ADSP}}$ CONTROLLED , $\overline{\text{ADSC}}$=HIGH)



***Notes :** n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

☐ Don't Care ▨ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units:millimeters/inches