Document Title

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial draft	Feb. 23. 2001	Preliminary
0.1	1. Add JTAG Scan Order	May. 10. 2001	Preliminary
0.2	1. Add x32 org and industrial temperature . 2. Add 165FBGA package	Aug. 30. 2001	Preliminary
1.0	1. Final spec release	May. 10. 2002	Final
1.1	1. Delete 119BGA package. 2. Correct the Ball Size of 165 FBGA.	April 04. 2003	Final
2.0	1. Delete x32 Org. 2. Delete 165FBGA package. 3. Delelte the 6.5 ns speed bin.	Nov. 17, 2003	Final

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16Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7B161825A-QC(I)75/85	SB	3.3	7.5/8.5ns		C ; Commercial Temp.Range
	K7A161800A-QC(I)25/16/14	SPB(2E1D)	3.3	250/167/138MHz		
	K7A161801A-QC(I)20/16	SPB(2E2D)	3.3	200/167MHz	Q : 100TQFP	
512Kx36	K7B163625A-QC(I)75/85	SB	3.3	7.5/8.5ns		I ; Industrial Temp.Range
	K7A163600A-QC(I)25/16/14	SPB(2E1D)	3.3	250/167/138MHz		
	K7A163601A-QC(I)20/16	SPB(2E2D)	3.3	200/167MHz		

K7B163625A
K7B161825A
512Kx36 & 1Mx18 Synchronous SRAM

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O
  or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A
- Operating in commeical and industrial temperature range.

GENERAL DESCRIPTION

The K7B163625A and K7B161825A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(32/18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS_1}$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).
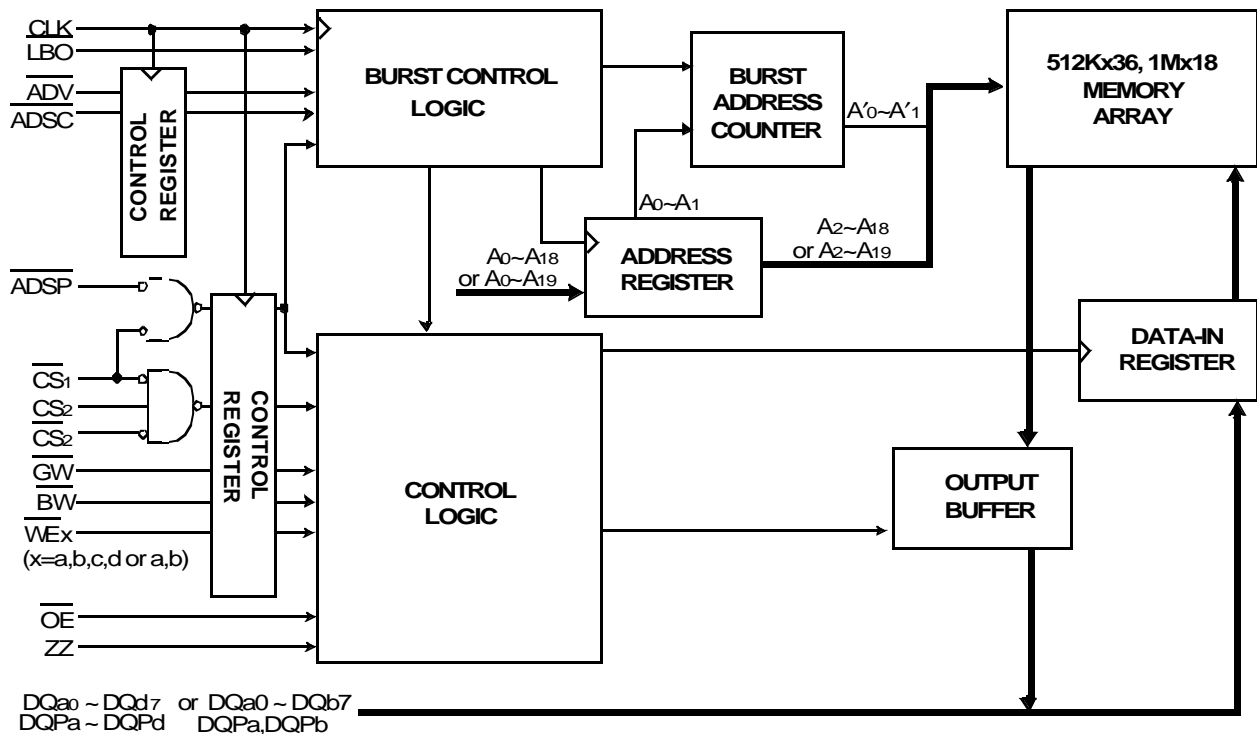
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B163625A and K7B161825A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

FAST ACCESS TIMES

PARAMETER	Symbol	-75	-85	Unit
Cycle Time	t_{CYC}	8.5	10	ns
Clock Access Time	t_{CD}	7.5	8.5	ns
Output Enable Access Time	t_{OE}	3.5	4.0	ns

LOGIC BLOCK DIAGRAM

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K7B163625A
K7B161825A

512Kx36 & 1Mx18 Synchronous SRAM

PIN CONFIGURATION (TOP VIEW)

Top pins (left to right): A6, A7, CS1, CS2, WEd, WEc, WEb, WEa, CS2, VDD, VSS, CLK, GW, BW, OE, ADSC, ADSP, ADV, A8, A9

Pins 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 88, 87, 86, 85, 84, 83, 82, 81

Left side:
- 1 NC/DQPc
- 2 DQc0
- 3 DQc1
- 4 VDDQ
- 5 VSSQ
- 6 DQc2
- 7 DQc3
- 8 DQc4
- 9 DQc5
- 10 VSSQ
- 11 VDDQ
- 12 DQc6
- 13 DQc7
- 14 N.C.
- 15 VDD
- 16 N.C.
- 17 VSS
- 18 DQd0
- 19 DQd1
- 20 VDDQ
- 21 VSSQ
- 22 DQd2
- 23 DQd3
- 24 DQd4
- 25 DQd5
- 26 VSSQ
- 27 VDDQ
- 28 DQd6
- 29 DQd7
- 30 NC/DQPd

Right side:
- 80 DQPb/NC
- 79 DQb7
- 78 DQb6
- 77 VDDQ
- 76 VSSQ
- 75 DQb5
- 74 DQb4
- 73 DQb3
- 72 DQb2
- 71 VSSQ
- 70 VDDQ
- 69 DQb1
- 68 DQb0
- 67 VSS
- 66 N.C.
- 65 VDD
- 64 ZZ
- 63 DQa7
- 62 DQa6
- 61 VDDQ
- 60 VSSQ
- 59 DQa5
- 58 DQa4
- 57 DQa3
- 56 DQa2
- 55 VSSQ
- 54 VDDQ
- 53 DQa1
- 52 DQa0
- 51 DQPa/NC

Center: 100 Pin TQFP (20mm x 14mm) K7B163625A(512Kx36)

Bottom pins (left to right): LBO, A5, A4, A3, A2, A1, A0, N.C., N.C., VSS, VDD, A18, A17, A10, A11, A12, A13, A14, A15, A16

Pins 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	VDD VSS	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd		51,80,1,30
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	or NC		
OE	Output Enable	86			
GW	Global Write Enable	88	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
BW	Byte Write Enable	87			
ZZ	Power Down Input	64	VSSQ	Output Ground	5,10,21,26,55,60,71,76
LBO	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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K7B163625A
K7B161825A

512Kx36 & 1Mx18 Synchronous SRAM

PIN CONFIGURATION(TOP VIEW)

100 Pin TQFP
(20mm x 14mm)

K7B161825A(1Mx18)

Top pins (left to right): A6, A7, $\overline{CS_1}$, CS2, N.C., N.C., $\overline{WEb}$, $\overline{WEa}$, $\overline{CS_2}$, VDD, VSS, CLK, GW, BW, OE, ADSC, ADSP, ADV, A8, A9

Left pins (top to bottom, 1-30): N.C.(1), N.C.(2), N.C.(3), VDDQ(4), VSSQ(5), N.C.(6), N.C.(7), DQb0(8), DQb1(9), VSSQ(10), VDDQ(11), DQb2(12), DQb3(13), N.C.(14), VDD(15), N.C.(16), VSS(17), DQb4(18), DQb5(19), VDDQ(20), VSSQ(21), DQb6(22), DQb7(23), DQPb(24), N.C.(25), VSSQ(26), VDDQ(27), N.C.(28), N.C.(29), N.C.(30)

Right pins (top to bottom, 80-51): A10(80), N.C.(79), N.C.(78), VDDQ(77), VSSQ(76), N.C.(75), DQPa(74), DQa7(73), DQa6(72), VSSQ(71), VDDQ(70), DQa5(69), DQa4(68), VSS(67), N.C.(66), VDD(65), ZZ(64), DQa3(63), DQa2(62), VDDQ(61), VSSQ(60), DQa1(59), DQa0(58), N.C.(57), N.C.(56), VSSQ(55), VDDQ(54), N.C.(53), N.C.(52), N.C.(51)

Bottom pins (left to right, 31-50): LBO(31), A5(32), A4(33), A3(34), A2(35), A1(36), A0(37), N.C.(38), N.C.(39), VSS(40), VDD(41), A19(42), A18(43), A11(44), A12(45), A13(46), A14(47), A15(48), A16(49), A17(50)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	VDD VSS N.C.	Power Supply(+3.3V) Ground No Connect	15,41,65,91 17,40,67,90 1,2,3,6,7,14,16,25,28,29, 30,38,39,51,52,53,56,57, 66,75,78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_1}$	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
$\overline{CS_2}$	Chip Select	92			
$\overline{WEx}$(x=a,b)	Byte Write Inputs	93,94	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86		(2.5V or 3.3V)	
$\overline{GW}$	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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K7B163625A
K7B161825A

512Kx36 & 1Mx18 Synchronous SRAM

FUNCTION DESCRIPTION

The K7B163625A and K7B161825A are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$, and $\overline{WEd}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WEx}$.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B163625M, a 512Kx36 organization, $\overline{WEa}$ controls DQa0 ~ DQa7 and DQPa, $\overline{WEb}$ controls DQb0 ~ DQb7 and DQPb, $\overline{WEc}$ controls DQc0 ~ DQc7 and DQPc and $\overline{WEd}$ controls DQd0 ~ DQd7 and DQPd.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS2	$\overline{CS_2}$	ADSP	ADSC	ADV	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don′t Care".

2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.

$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don′t Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don′t Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes
1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}		V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation		P_D	1.6	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

*Note : Sampled not 100% tested.

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DC ELECTRICAL CHARACTERISTICS $(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C$ to $+70°C)$

Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; $V_{IN}=V_{SS}$ to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled, $V_{out}=V_{SS}$ to V_{DDQ}		-2	+2	µA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, $ZZ\leq V_{IL}$, Cycle Time $\geq t_{CYC}$ Min	-75	-	250	mA	1,2
			-85	-	230		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, $ZZ\leq V_{IL}$, f=Max, All Inputs$\leq$0.2V or $\geq V_{DD}$-0.2V	-75	-	90	mA	
			-85	-	80		
	I_{SB1}	Device deselected, I_{OUT}=0mA, $ZZ\leq$0.2V, f=0, All Inputs=fixed (VDD-0.2V or		-	70	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, $ZZ\geq V_{DD}$-0.2V, f=Max, All Inputs$\leq V_{IL}$or $\geq V_{IH}$		-	60	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
    2. Reference AC Operating Conditions and Characteristics for input and timing.
    3. Data states are all zero.
    4. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3V$

V_{IH}
V_{SS}
V_{SS}-1.0V
20% t_{CYC}(MIN)
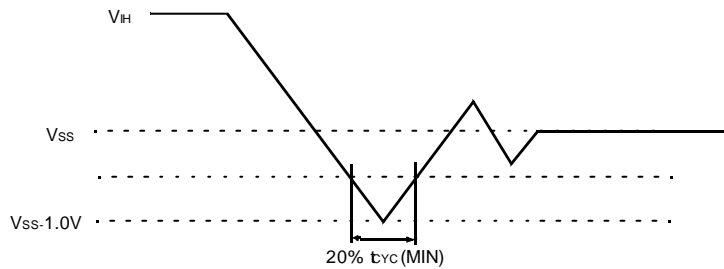
TEST CONDITIONS
$(V_{DD}=3.3V+0.165V/-0.165V, V_{DDQ}=3.3V+0.165/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V, V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0to70°C)$

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

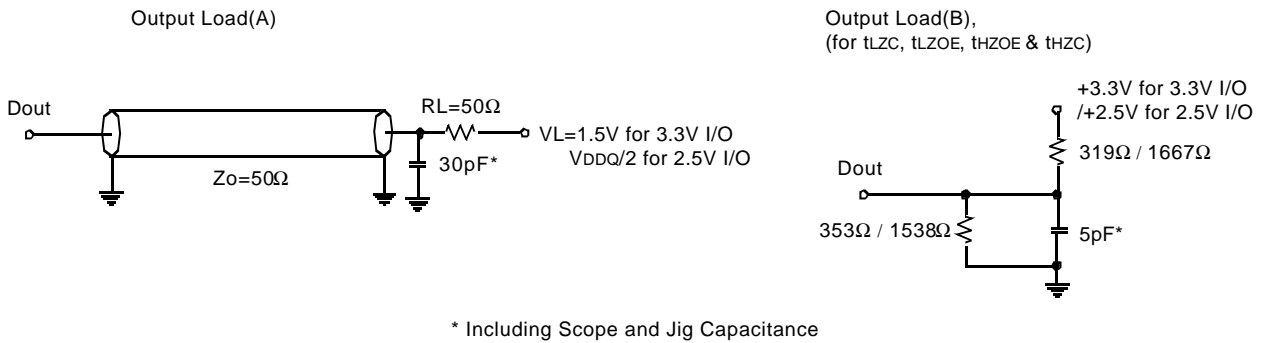* The above parameters are also guaranteed at industrial temperature range.

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Output Load(A)

Output Load(B),
(for tLZC, tLZOE, tHZOE & tHZC)

* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(V$_{DD}$=3.3V+0.165V/-0.165V, T$_A$=0°C to +70°C)

PARAMETER	SYMBOL	-75		-85		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	tCYC	8.5	-	10	-	ns
Clock Access Time	tCD	-	7.5	-	8.5	ns
Output Enable to Data Valid	tOE	-	3.5	-	4.0	ns
Clock High to Output Low-Z	tLZC	2.5	-	2.5	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	4.0	ns
Clock High to Output High-Z	tHZC	-	4.0	-	5.0	ns
Clock High Pulse Width	tCH	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
    2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
    3. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
    4. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.
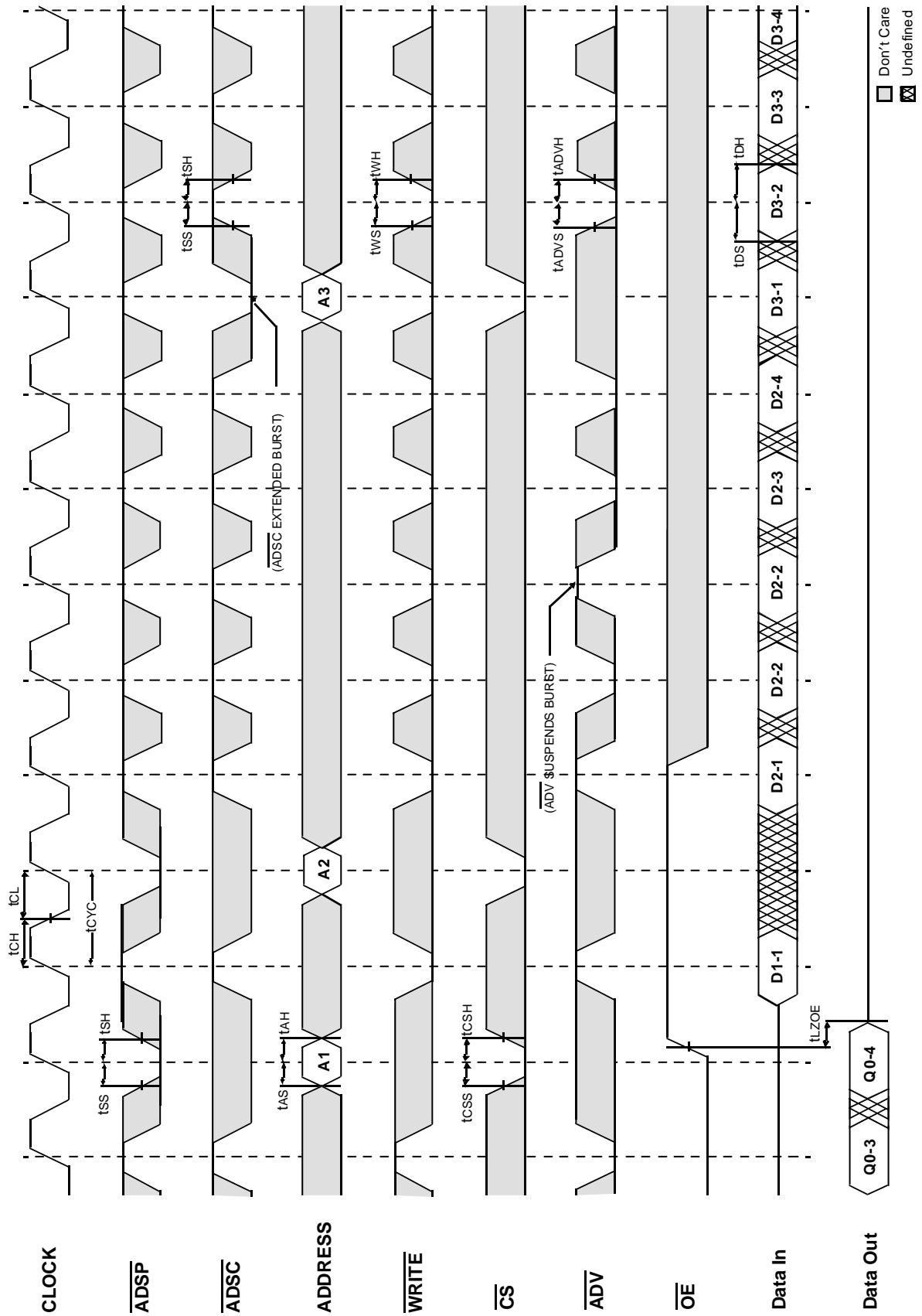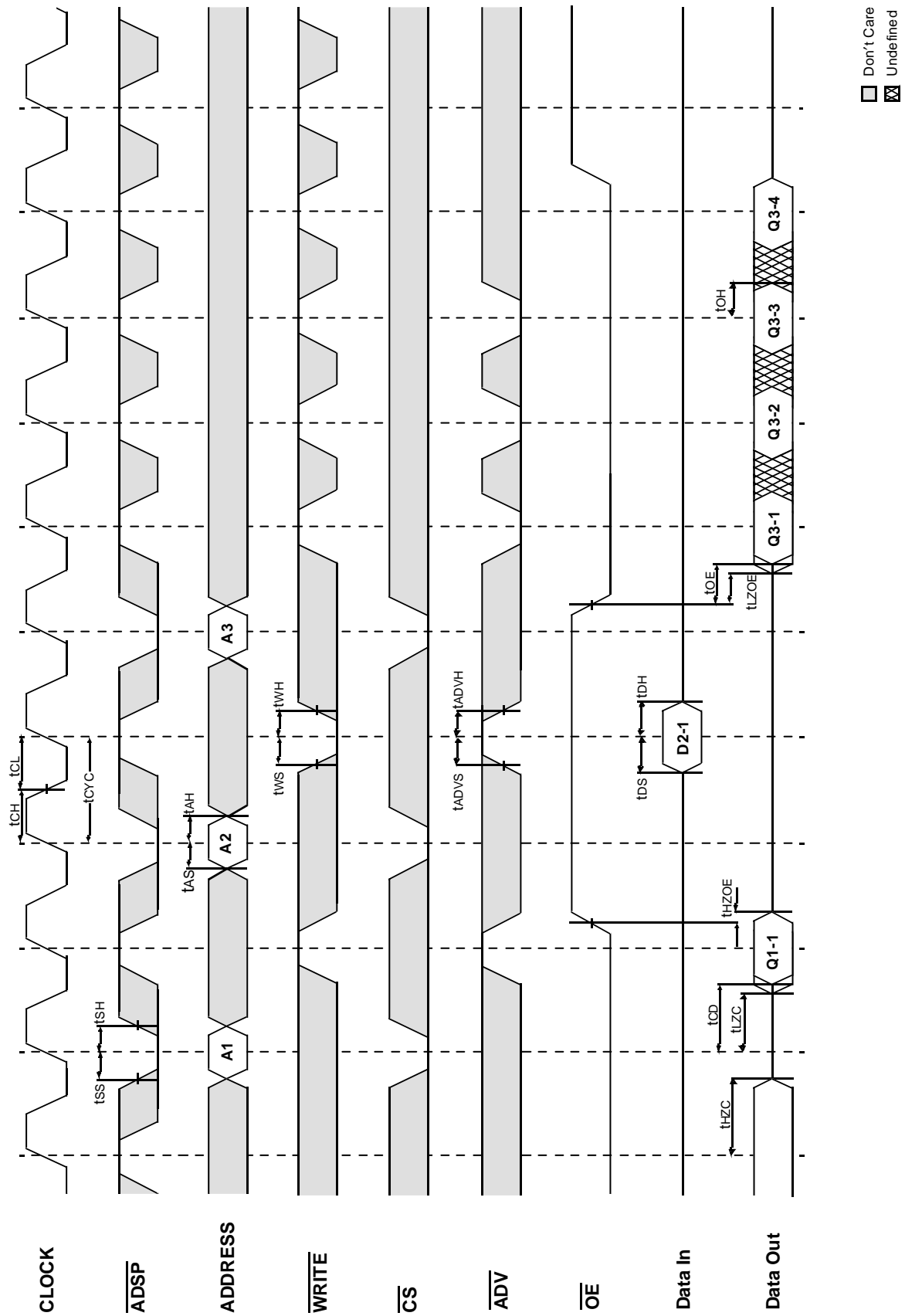
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TIMING WAVEFORM OF READ CYCLE
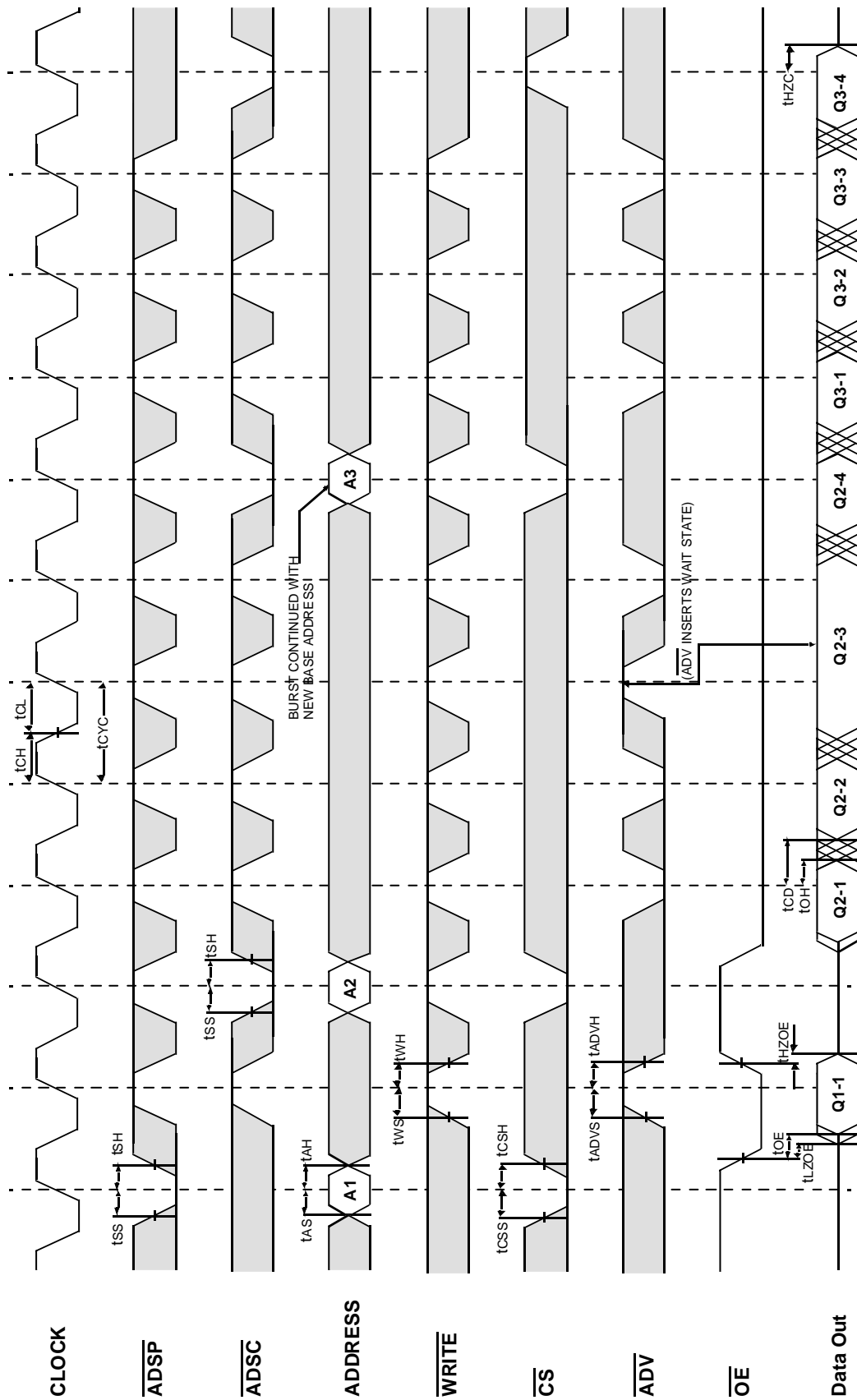
Don't Care

Undefined

NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WEx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and CS_2 = H, or $\overline{CS_1}$ = L, and $\overline{CS_2}$ = L
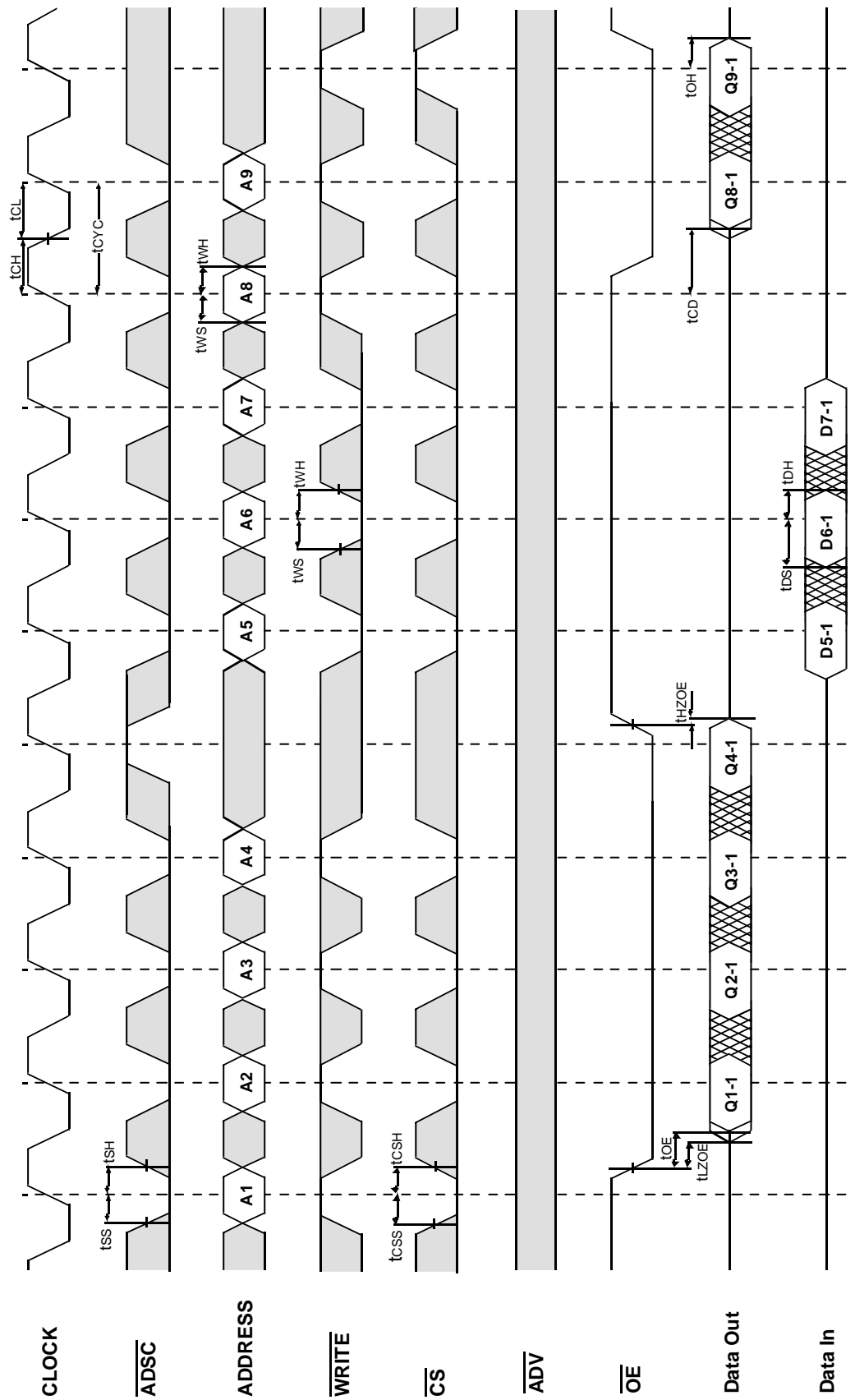
CLOCK

$\overline{ADSP}$

$\overline{ADSC}$

ADDRESS

$\overline{WRITE}$

$\overline{CS}$

$\overline{ADV}$

$\overline{OE}$

Data Out

TIMING WAVEFORM OF WRITE CYCLE

Signals (bottom to top reading order of rows): CLOCK, ADSP, ADSC, ADDRESS, WRITE, CS, ADV, OE, Data In, Data Out

Timing parameters shown: tCH, tCL, tCYC, tSS, tSH, tAS, tAH, tCSS, tCSH, tWS, tWH, tADVS, tADVH, tDS, tDH, tLZOE

Address values: A1, A2, A3

(ADSC EXTENDED BURST)
(ADV SUSPENDS BURST)

Data In values: D1-1, D2-1, D2-2, D2-2, D2-3, D2-4, D3-1, D3-2, D3-3, D3-4

Data Out values: Q0-3, Q0-4

Legend: Don't Care, Undefined

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TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

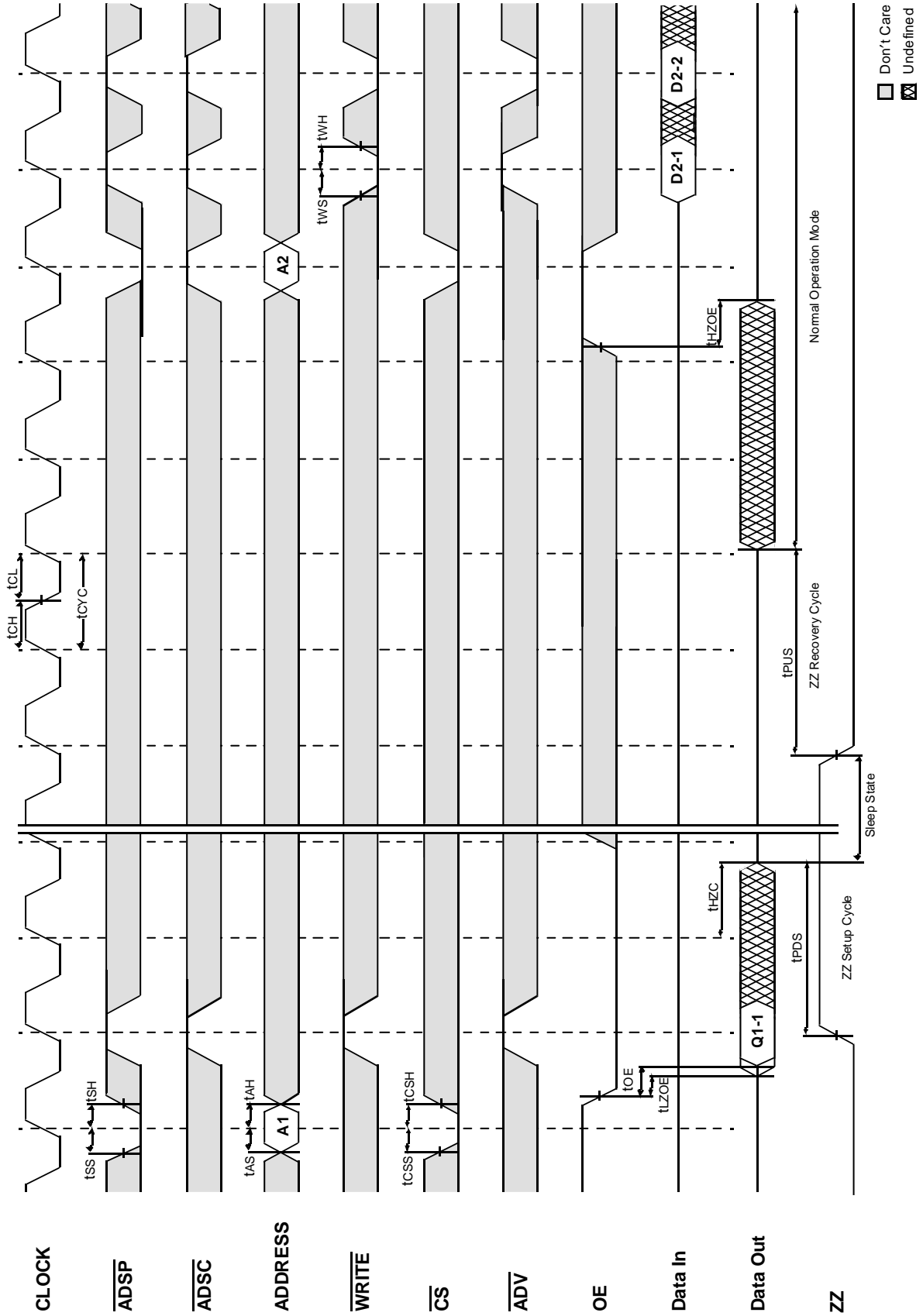**TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)**

Don't Care
Undefined

CLOCK
ADSC
ADDRESS
WRITE
CS
ADV
OE
Data Out
Data In

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

Don't Care
Undefined
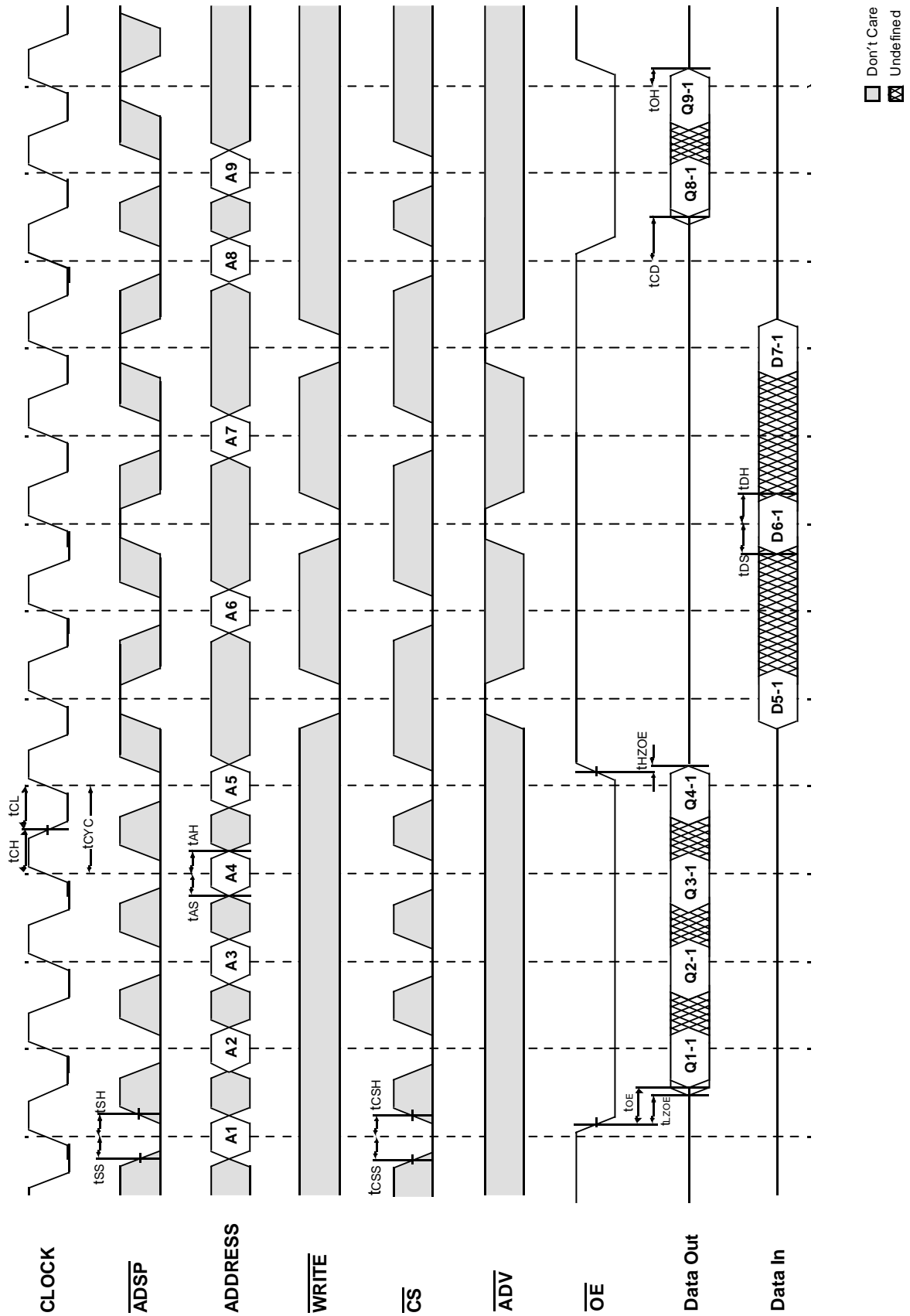
TIMING WAVEFORM OF POWER DOWN CYCLE

Signals: CLOCK, ADSP, ADSC, ADDRESS, WRITE, CS, ADV, OE, Data In, Data Out, ZZ

Timing parameters: tSS, tSH, tAS, tAH, tCSS, tCSH, tOE, tLZOE, tHZC, tPDS, tHZOE, tPUS, tCH, tCL, tCYC, tWS, tWH

Labels: A1, A2, Q1-1, D2-1, D2-2, ZZ Setup Cycle, Sleep State, ZZ Recovery Cycle, Normal Operation Mode

Legend: ☐ Don't Care   ⊠ Undefined

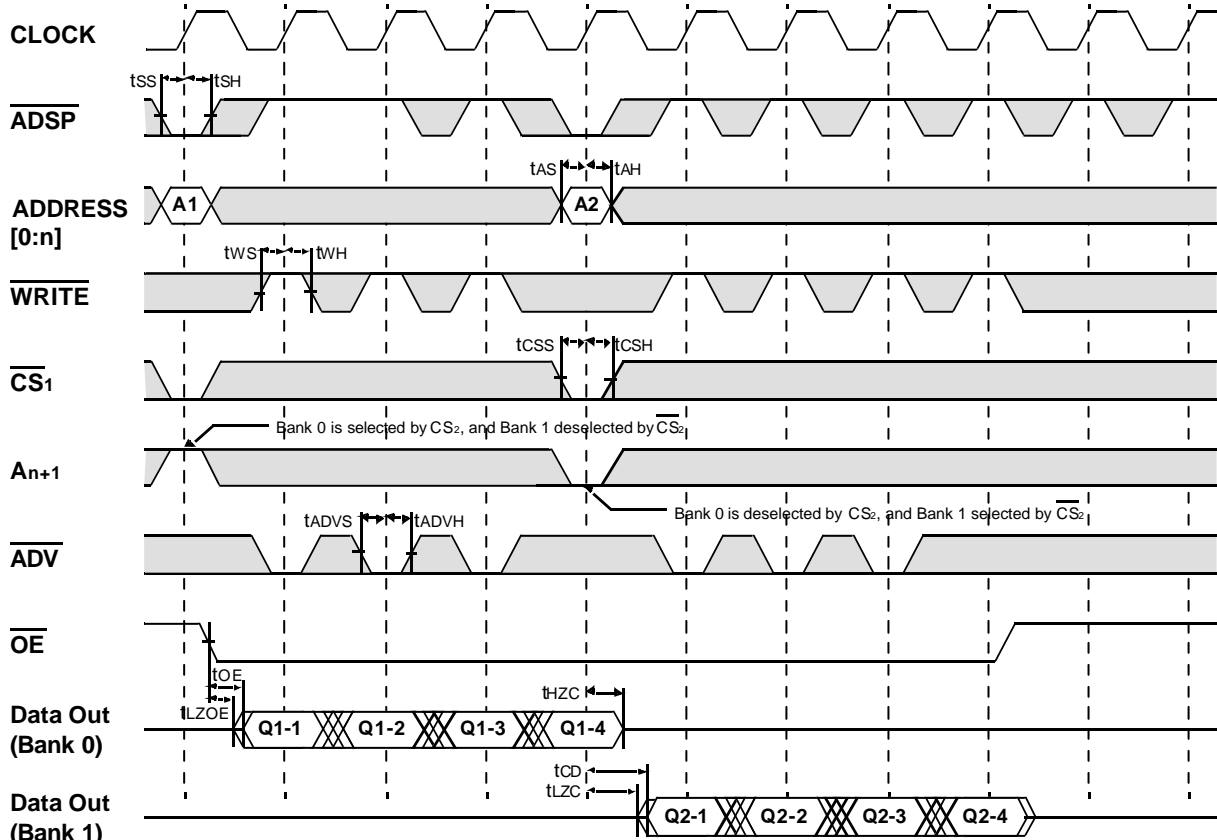## APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.
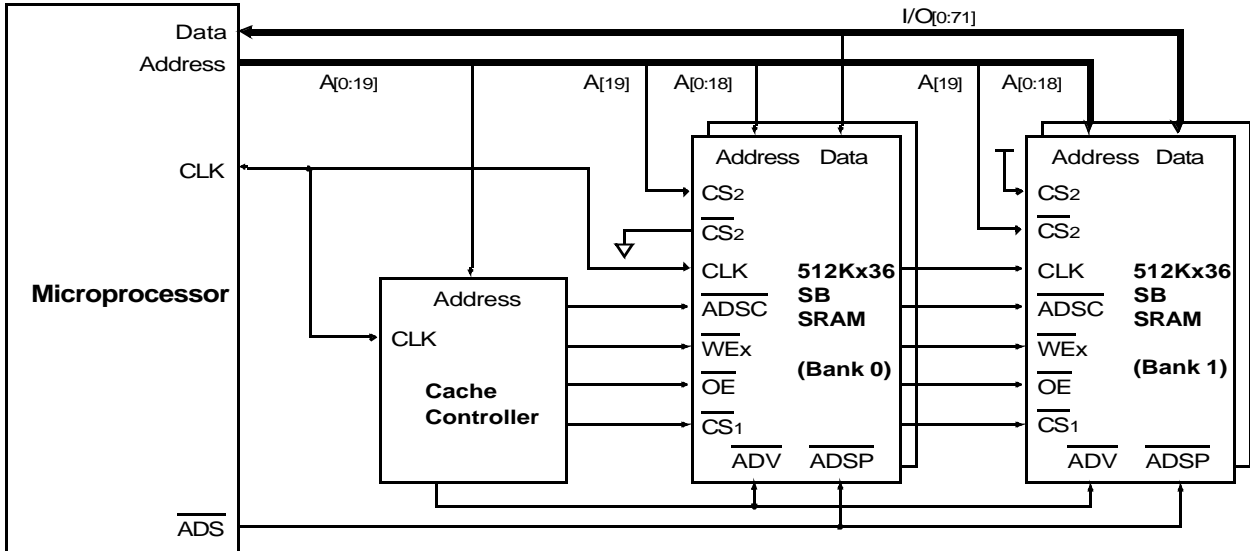
INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{\text{ADSP}}$ CONTROLLED , $\overline{\text{ADSC}}$=HIGH)
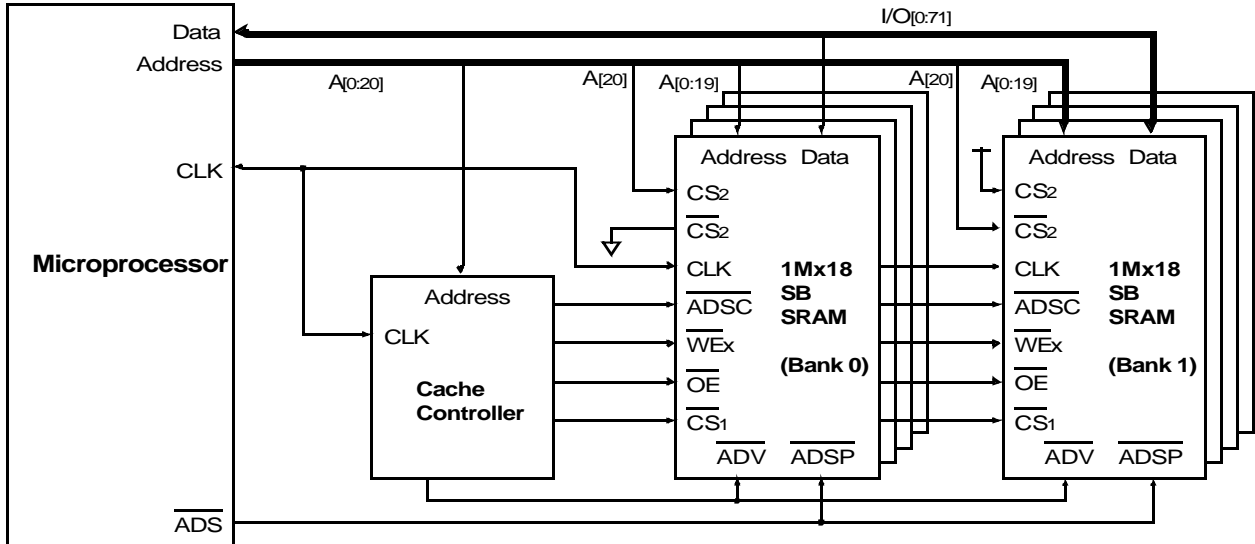

*Notes : n = 14 32K depth ,   15 64K depth
                16 128K depth ,   17 256K depth
                18 512K depth ,   19 1M depth

☐ Don't Care   ☒ Undefined

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APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)
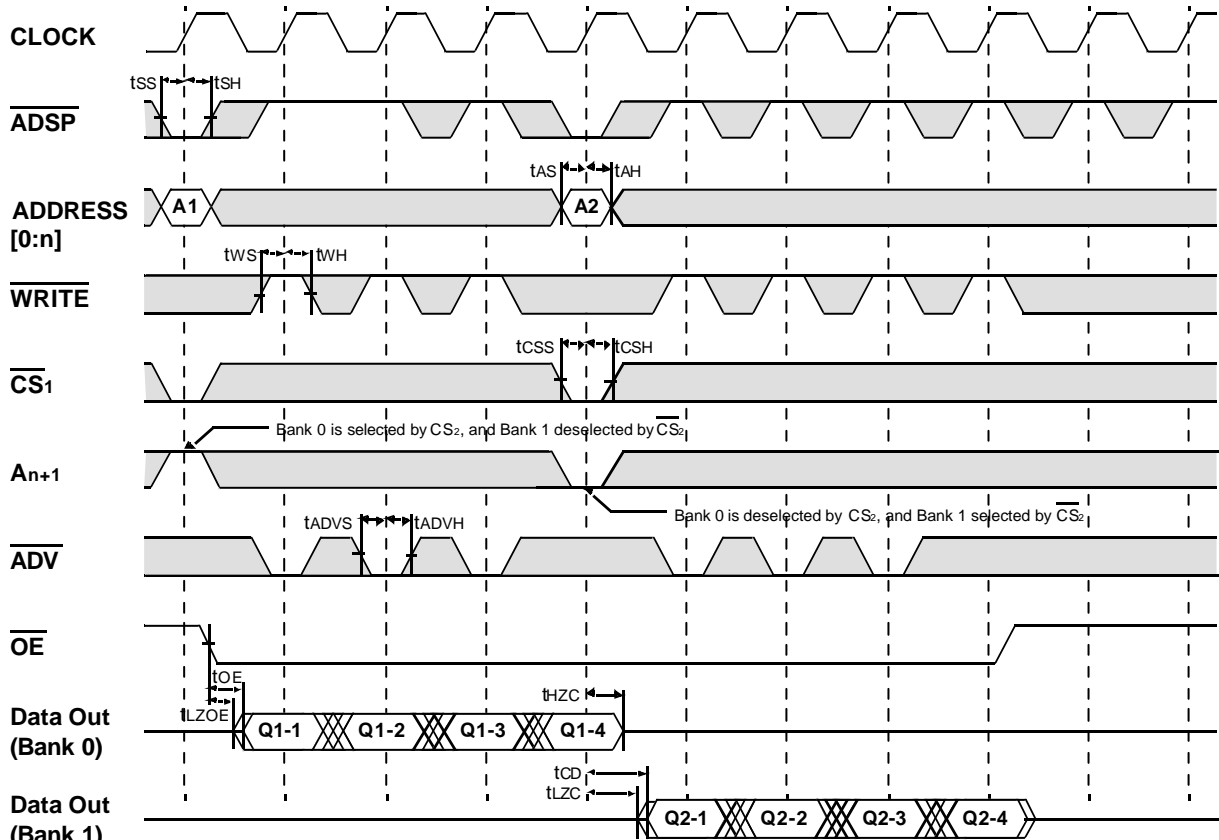
*Notes : n = 14   32K depth ,   15   64K depth
                  16   128K depth ,   17   256K depth
                  18   512K depth ,   19   1M depth
                  20   2M depth

☐ Don't Care   ☒ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units ; millimeters/Inches

22.00 ±0.30

20.00 ±0.20

16.00 ±0.30

14.00 ±0.20

(0.83)

#1

0.65

0.30 ±0.10

⊕ 0.10 MAX

(0.58)

0~8°

0.127 $^{+0.10}_{-0.05}$

□ 0.10 MAX

0.50 ±0.10

1.40 ±0.10 1.60 MAX

0.05 MIN

0.50 ±0.10

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