Document Title

Multi-Chip Package MEMORY

256M Bit (16Mx16) Nand Flash / 64M Bit (4Mx16) Burst UtRAM / 256M Bit (4Mx16x4Banks) Mobile SDRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft - 256Mb NAND C-Die_Ver 2.6 - 64Mb UtRAM B-Die(Burst)_Ver 0.4 - 256Mb Mobile SDRAM E-Die_Ver 0.7	September 24, 2003	Preliminary

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

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256M Bit (16Mx16) Nand Flash / 64M Bit (4Mx16) Burst UtRAM / 256M Bit (4Mx16x4Banks) Mobile SDRAM

FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 137-ball FBGA Type - 10.5x13mm, 0.8mm pitch

<NAND>
- Power Supply Voltage : 1.7~1.95V
- Organization
  - Memory Cell Array : (16M + 512K)bit x 16bit
  - Data Register : (256 + 8)bit x16bit
- Automatic Program and Erase
  - Page Program : (2)Word
  - Block Erase : (8K + 256)Word
- Page Read Operation
  - Page Size : (256 + 8)Word
  - Random Access : 10μs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back
- Unique ID for Copyright Protection

<U*t*RAM>
- Process Technology: CMOS
- Organization: 4M x16 bit
- Power Supply Voltage: V_{CC} 2.7~3.1V / V_{CCQ} 1.7~2.0V
- Three State Outputs
- Compatible with Low Power SRAM
- Supports MRS (Mode Register Set)
- Supports Asynchronous Read/Write Operation in Asynchronous-mode
- Supports Synchronous Burst Read and Asynchronous Write Operation in Synchronous mode
- Synchronous Burst Read Operation
  - Supports 4 word / 8 word / 16 word Burst Read mode
  - Supports Linear Burst type & Interleave Burst type
  - Latency support : 3, 4, 5, 6 (depends on clock frequency)
- Max. Burst Clock Frequency : 54MHz

<SDRAM>
- Power Supply Voltage : 1.65~1.95V
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - -. CAS latency (1, 2 & 3).
  - -. Burst length (1, 2, 4, 8 & Full page).
  - -. Burst type (Sequential & Interleave).
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- Special Function Support.
  - -. PASR (Partial Array Self Refresh).
  - -. Internal TCSR (Temperature Compensated Self Refresh)
  - -. DS (Driver Strength)
- DQM for masking.
- Auto refresh.
- 64ms refresh period (4K cycle).

GENERAL DESCRIPTION

The KAA00BB07M is a Multi Chip Package Memory which combines 256Mbit Nand Flash Memory, 64Mbit Unit Transistor CMOS RAM and 256Mbit synchronous high data rate Dynamic RAM.

256Mbit NAND Flash memory is organized as 16M x16 bits and 64Mbit U*t*RAM is organized as 4M x16 bits and 256Mbit SDRAM is organized as 4M x16 bits x4 banks.

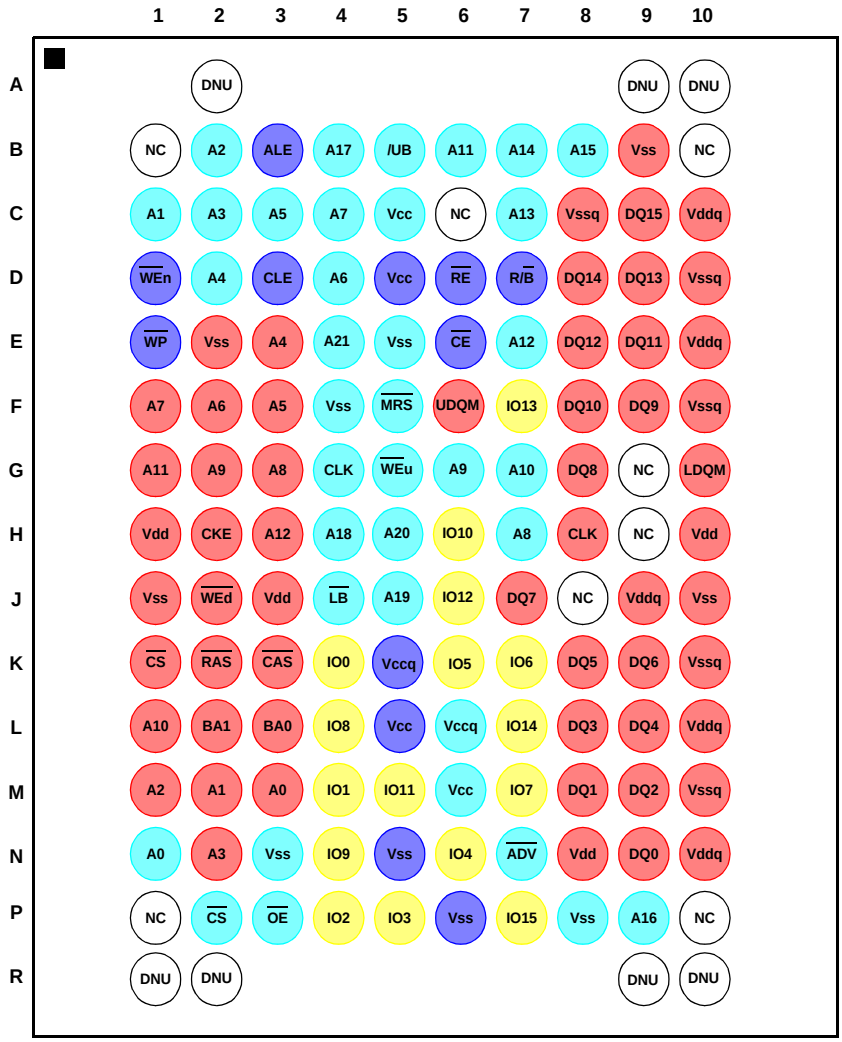
In 256Mbit NAND Flash, a 264-word page program can be typically achieved within 200us and an 8K-word block erase can be typically achieved within 2ms. In serial read operation, a word can be read by 50ns. DQ pins serve as the ports for address and data input/output as well as command inputs. Even the write-intensive systems can take advantage of FLASH′s extended reliability of 100K program/erase cycles with real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications.

In 64Mb burst UtRAM,the device supports DPD(Deep Power Down) mode and partial refresh mode for power saving. the device has 3 types of PAR(Partial Array Refresh) mode - 3/4 block refresh, 1/2 block refresh and 1/4 block refresh. In case of PAR mode, only the data in the refreshed block are valid. DPD and PAR mode is controlled by $\overline{MRS}$ pin. The device supports MRS(Mode Register Set) and synchronous burst read mode.

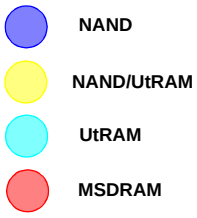
In 256Mbit SDRAM, Synchronous design make a device controlled precisely with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

The KAA00BB07M is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 137-ball FBGA Type.

PIN CONFIGURATION



FBGA: Top View (Ball Down)



PIN DESCRIPTION

Pin Name	Pin Function (NAND Flash)
/CE	Chip Enable
/RE	Read Enable
/WP	Write Protection
/WEn	Write Enable
ALE	Address Latch Enable
CLE	Command Latch Enable
R/$\overline{B}$	Ready/Busy Output
Vcc	Power Supply
Vccq	Dataout Power(It should be biased to Vcc)
Vss	Ground

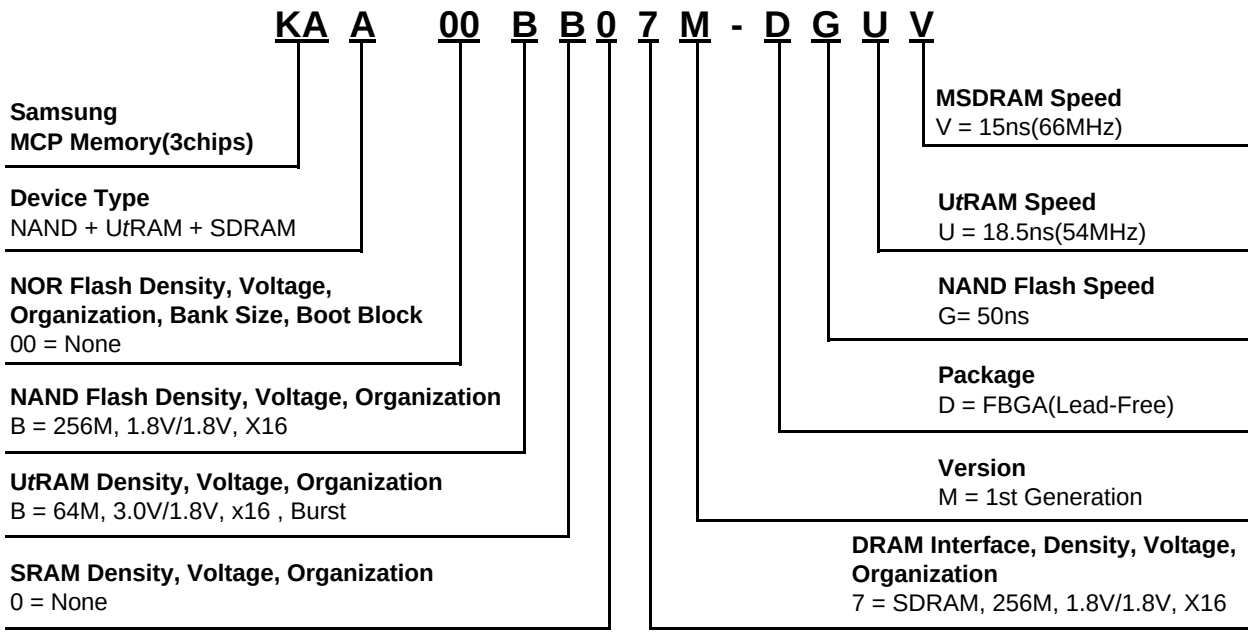
Pin Name	Pin Function (UtRAM)
CLK	Clock Input
/ADV	Address Valid Input
/MRS	Mode Resister Set
/CS	Chip Select
/OE	Output Enable Input
/WEu	Write Enable Input
/UB	Upper Byte(IO8 ~ IO15)
/LB	Lower Byte(IO0 ~ IO7)
A0 ~ A21	Address Inputs
Vcc	Power Supply
Vccq	Dataout Power
Vss	Ground

Pin Name	Pin Function (NAND Flash & UtRAM)
IO0 ~ IO15	Data Input/Output

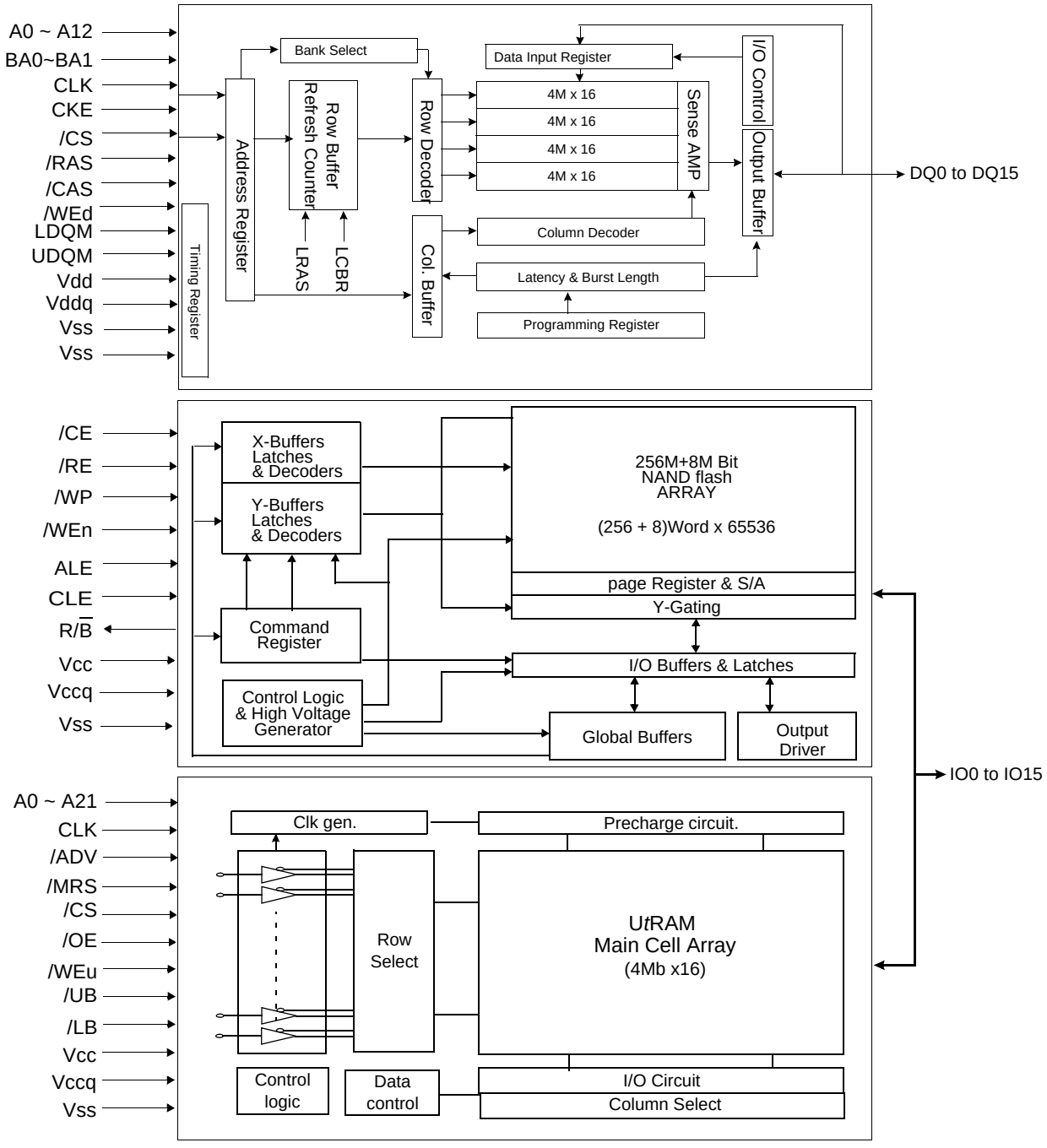
Pin Name	Pin Function (Mobile SDRAM)
CLK	System Clock
CKE	Clock Enable
/CS	Chip Select
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WEd	Chip Enable
A0~A12	Address Input
BA0~BA1	Bank Select Address
LDQM	Lower Data Input/Output Mask
UDQM	Upper Data Input/Output Mask
DQ0~DQ15	Data Input/Output
Vdd	Power Supply
Vddq	Dataout Power
Vss	Ground
Vssq	DQ Ground

Pin Name	Pin Function
DNU	Do Not Use
NC	No Connection

ORDERING INFORMATION

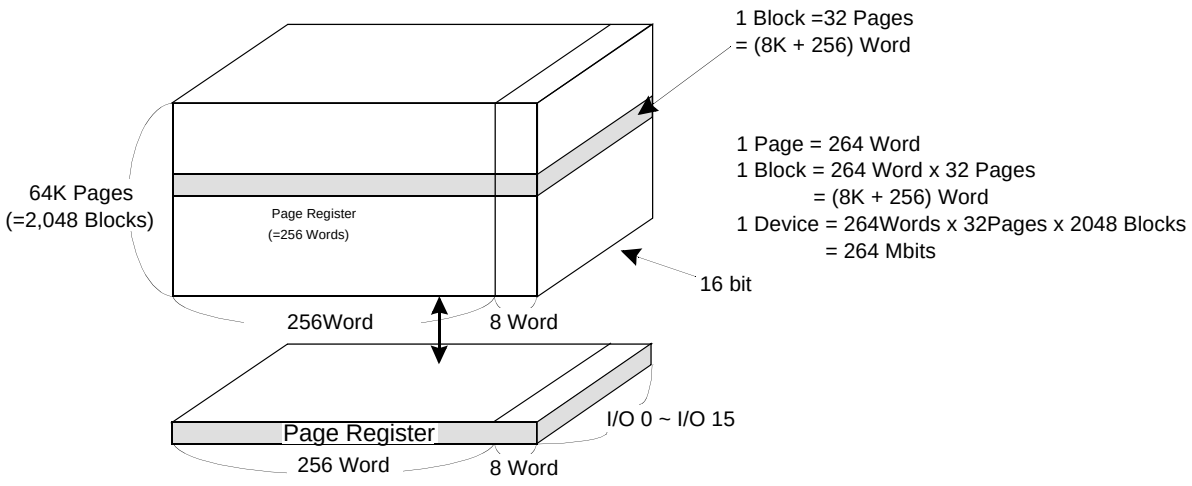


FUNCTIONAL BLOCK DIAGRAM



256Mb(16M x 16)
NAND Flash C-Die

Figure 1.NAND Flash ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O8 to 15	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	L*	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	L*	**Row Address (Page Address)**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	L*	

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

PRODUCT INTRODUCTION

The NAND Flash is a 264Mbit(276,824,064 bit) memory organized as 131,072 rows(pages) by 264 columns. Spare eight columns are located from column address of 256~263. A 264-word data register is connected to memory cell arrays accommodating data transfer between the IO buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 16 cells. Total 135168 NAND cells reside in a block. The array organization is shown in Figure 1. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4096 separately erasable 8K-Word blocks. It indicates that the bit by bit erase operation is prohibited on the NAND Flash.

The NAND Flash has addresses multiplexed into lower 8 IO's. The NAND Flash allows sixteen bit wide data transport into and out of page registers. This scheme dramatically reduces pin counts while providing high performance and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through IO′s by bringing $\overline{WE}$ to low while $\overline{CE}$n is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the IO pins. Some commands require one bus cycle. For example, Reset command, Read command, Status Read command, etc require just one cycle bus. Some other commands like Page Program and Copy-back Program and Block Erase, require two cycles: one cycle for setup and the other cycle for execution. The 32M-word physical space requires 25 addresses, thereby requiring four cycles for word-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the NAND Flash.

Table 1. COMMAND SET

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	00h	8Ah	
Block Erase	60h	D0h	
Read Status	70h	-	O

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN/OUT}$	-0.6 to + 2.45	V
	V_{CC}	-0.2 to + 2.45	
	V_{CCQ}	-0.2 to + 2.45	
Temperature Under Bias	T_{BIAS}	-40 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Short Circuit Current	Ios	5	mA

NOTE : 1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A=-25 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{CCQ}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I_{CC1}	tRC=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	8	15	mA
	Program	I_{CC2}	-	-	8	15	
	Erase	I_{CC3}	-	-	8	15	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	
Input High Voltage		V_{IH}	I/O pins	V_{CCQ}-0.4	-	V_{CCQ} +0.3	V
			Except I/O pins	V_{CC}-0.4	-	V_{CC} +0.3	
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.4	
Output High Voltage Level		V_{OH}	I_{OH}=-100µA	VccQ-0.1	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=100uA	-	-	0.1	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.1V	3	4	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	2013	-	2048	Blocks

NOTE :
1. The NAND Flash may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.
3. Minimum 1004 valid blocks are guaranteed for each contiguous 128Mb memory space.

AC TEST CONDITION

(Vcc=1.7V~1.95V , T_A=-40 to 85°C unless otherwise noted)

Parameter	Value
Input Pulse Levels	0V to VccQ
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VccQ/2
Output Load (VccQ:1.8V +/-10%)	1 TTL GATE and CL=30pF

CAPACITANCE(TA=25°C, VCC=1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	PRE	$\overline{WP}$	Mode	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input(3clock)
H	L	L	↑	H	X	H	Write Mode	Command Input
L	H	L	↑	H	X	H		Address Input(3clock)
L	L	L	↑	H	X	H	Data Input	
L	L	L	H	↓	X	X	Data Output	
X	X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(2)	0V/Vcc(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Dummy Busy Time for the Lock or Lock-tight Block		t_{LBSY}	-	5	10	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	.-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25 (1)	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	25	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{CE}$ Access Time	t_{CEA}	-	45	ns
$\overline{RE}$ Access Time	t_{REA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR1}	60	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low in Block Lcok Mode	t_{WHR2}	100	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NOTE : 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st word in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFFFh data at the column address of 256 and 261. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original invalid block information is prohibited.

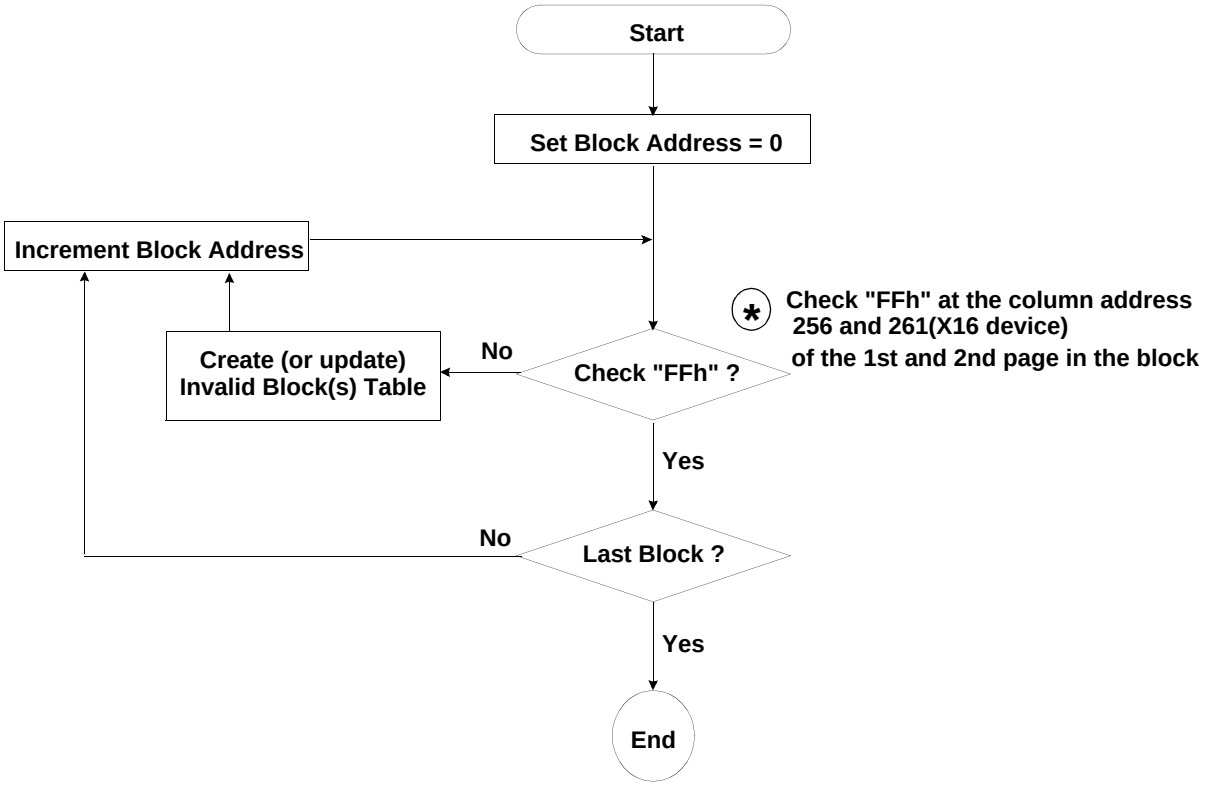


Figure 2. Flow chart to create invalid block table.

NAND Flash Technical Notes *(Continued)*

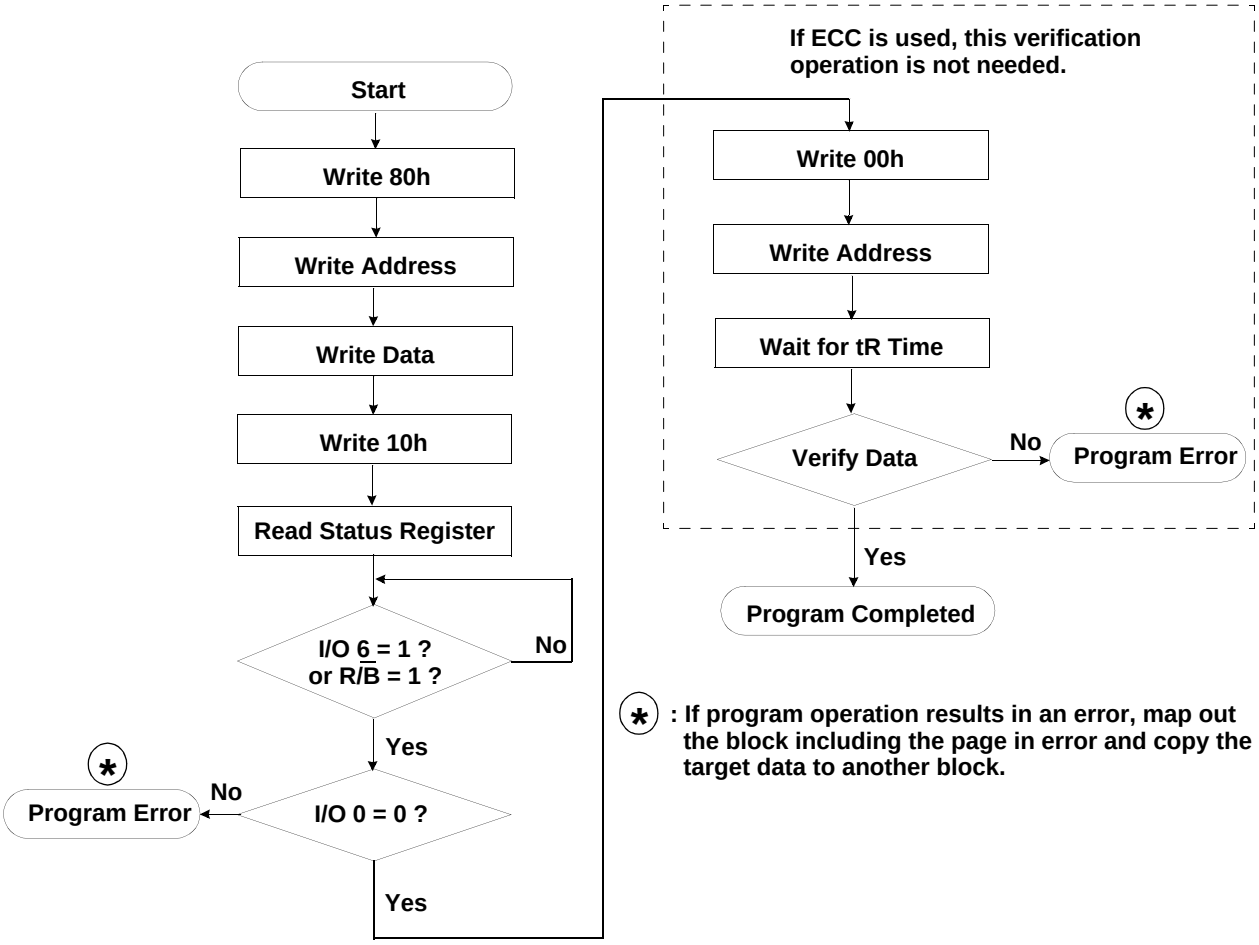
Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

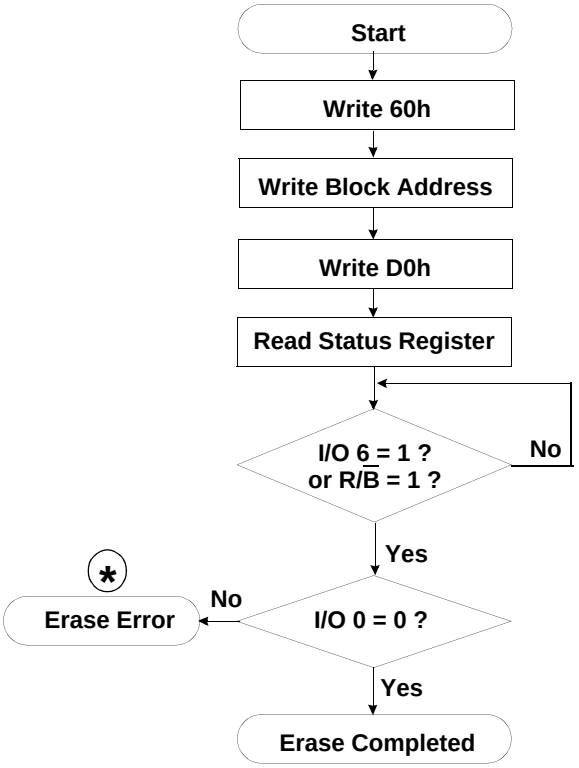
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

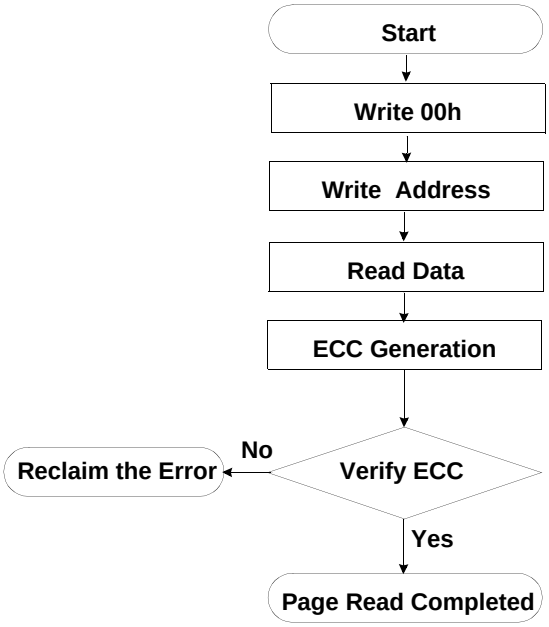


NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

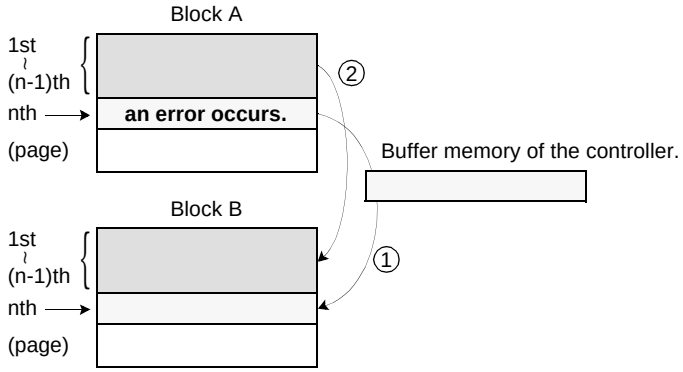


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Pointer Operation

Samsung NAND Flash has two address pointer commands as a substitute for the most significant column address. '00h' command sets the pointer to 'A' area(0~255word), and '50h' command sets the pointer to 'B' area(256~263word). With these commands, the starting column address can be set to any of a whole page(0~263word). '00h' or '50h' is sustained until another address pointer command is inputted. To program data starting from 'A' or 'B' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary.

Table 2. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 word	main array(A)
50h	256 ~ 263 word	spare array(B)

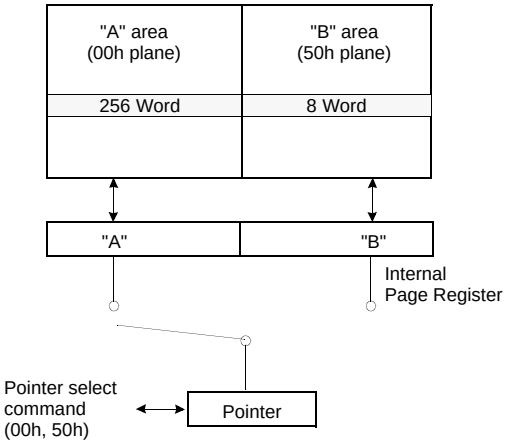
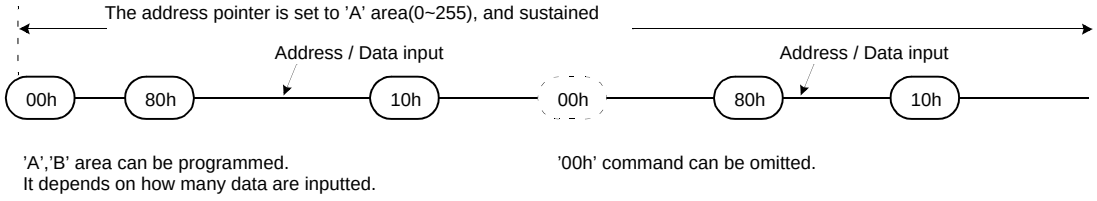
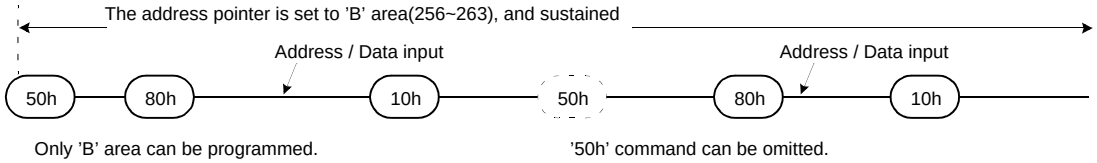


Figure 3. Block Diagram of Pointer Operation

(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 264word page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{CE}$ don't-care.

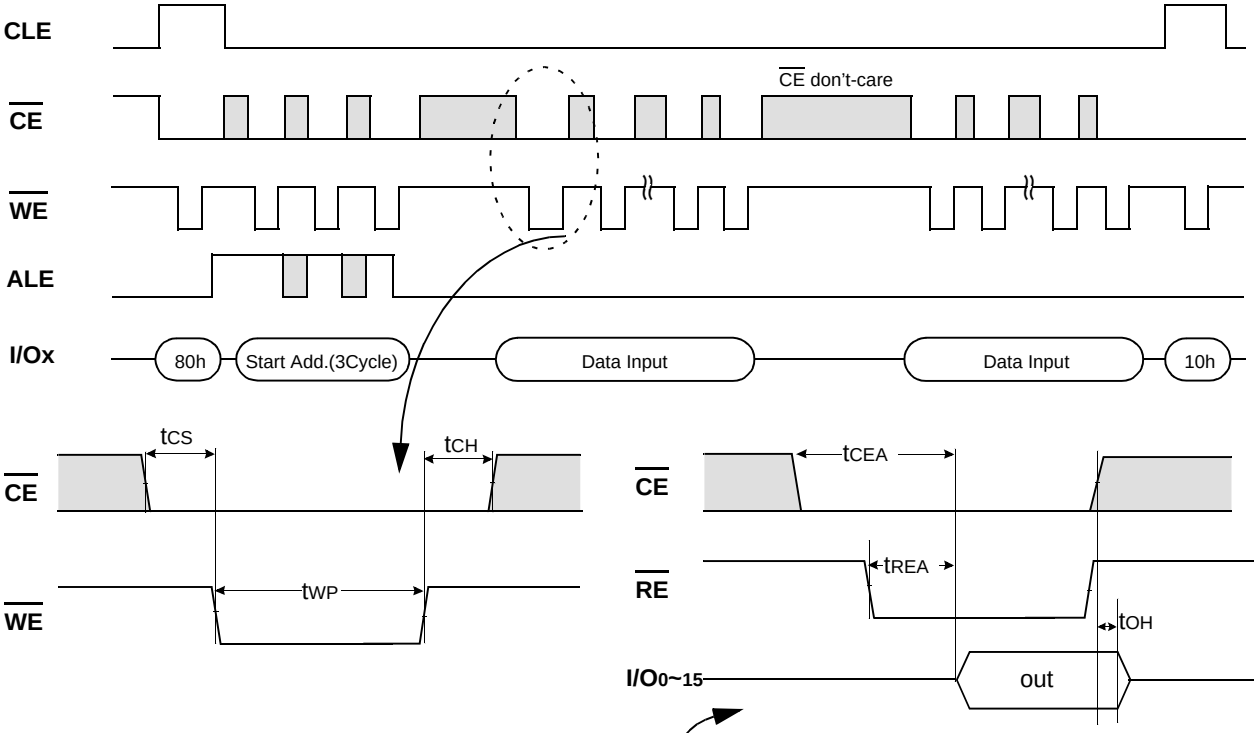
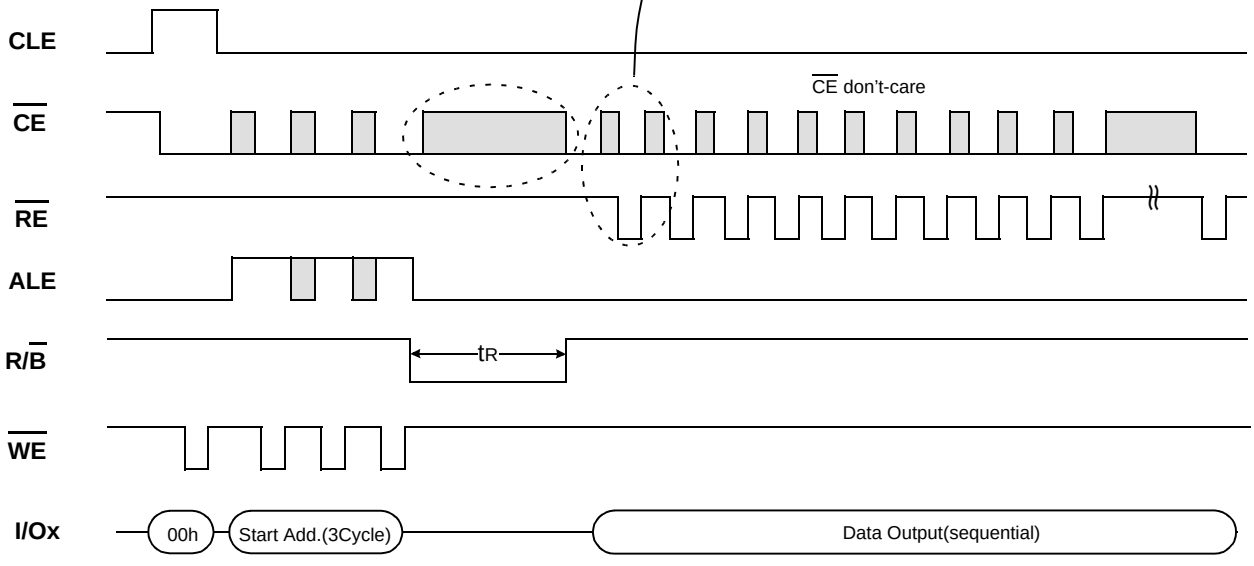
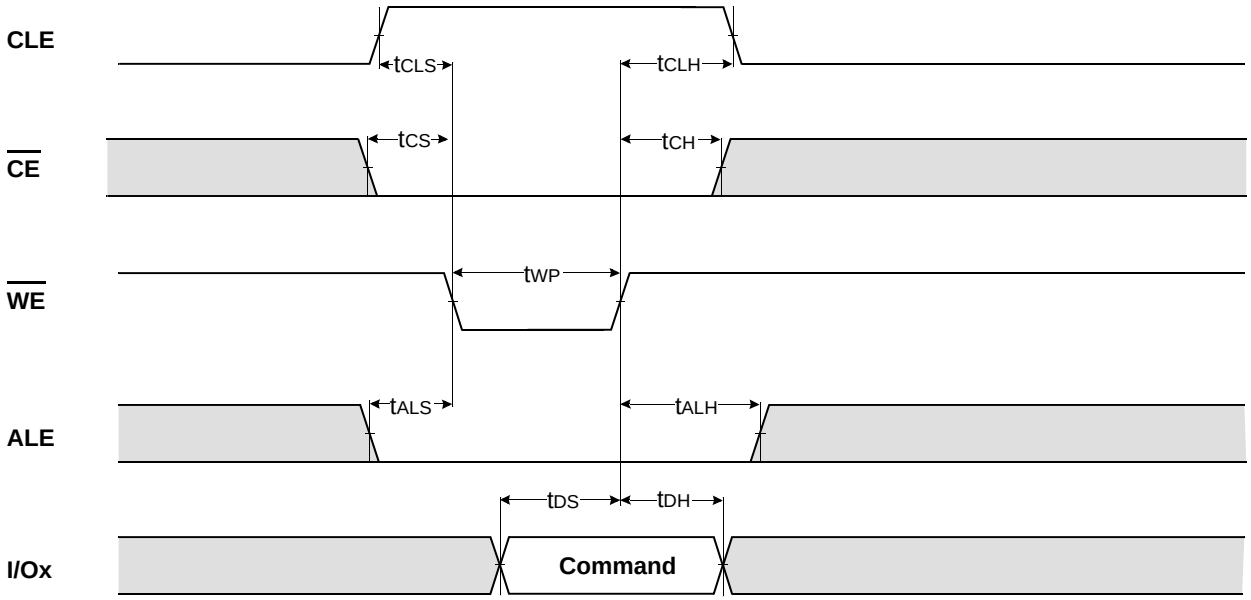


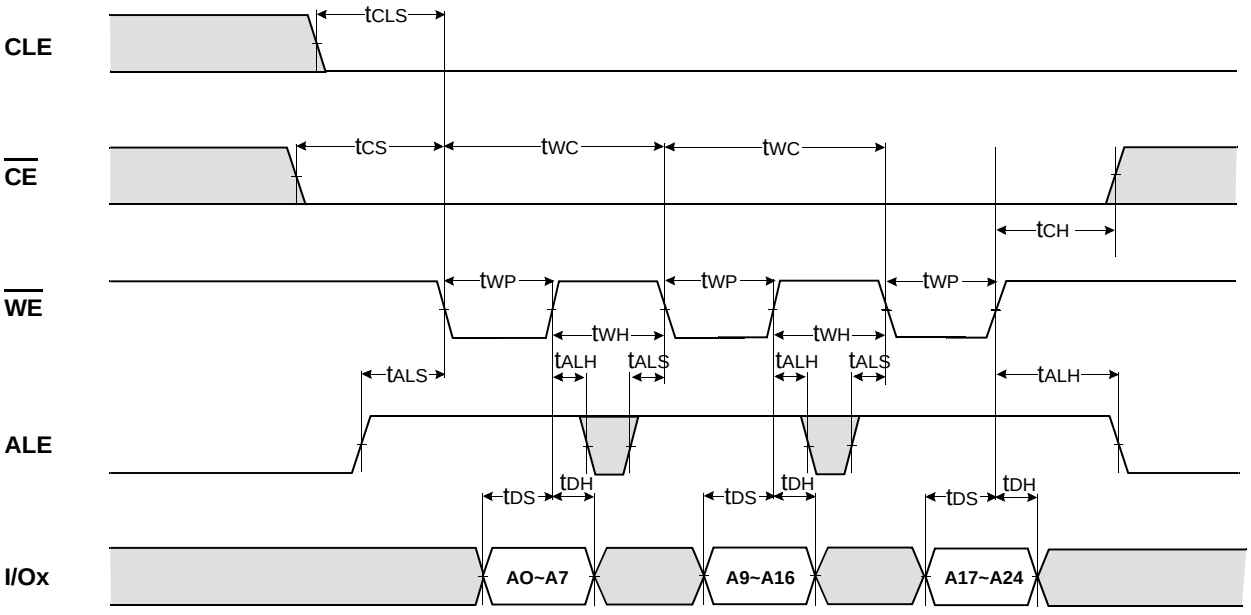
Figure 5. Read Operation with $\overline{CE}$ don't-care.



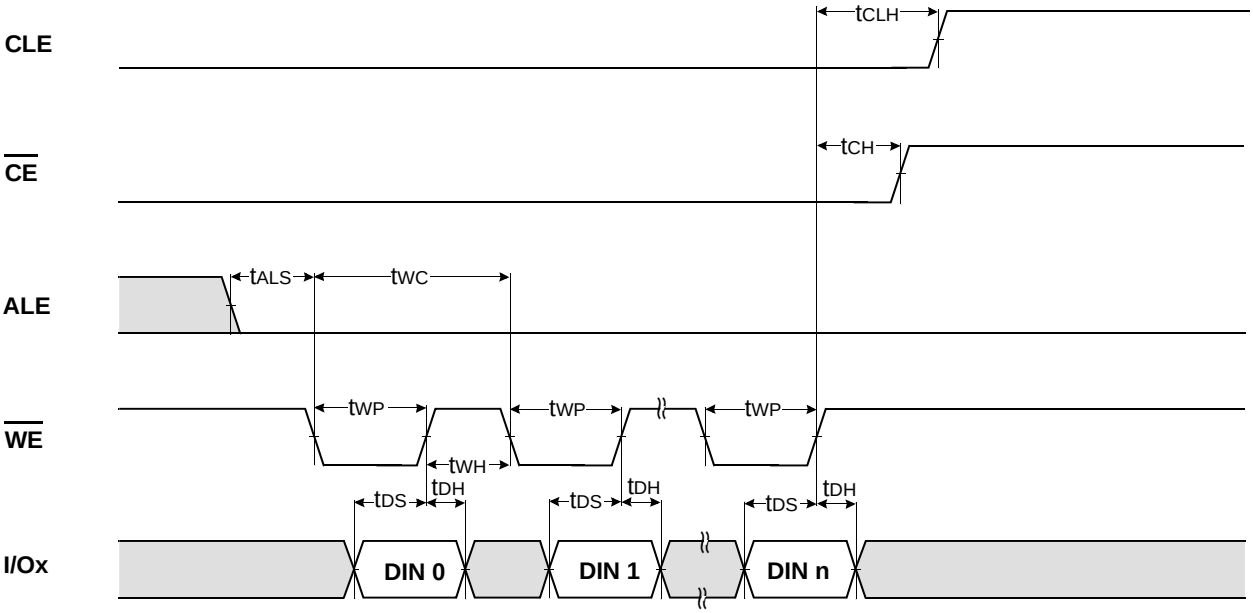
*** Command Latch Cycle**



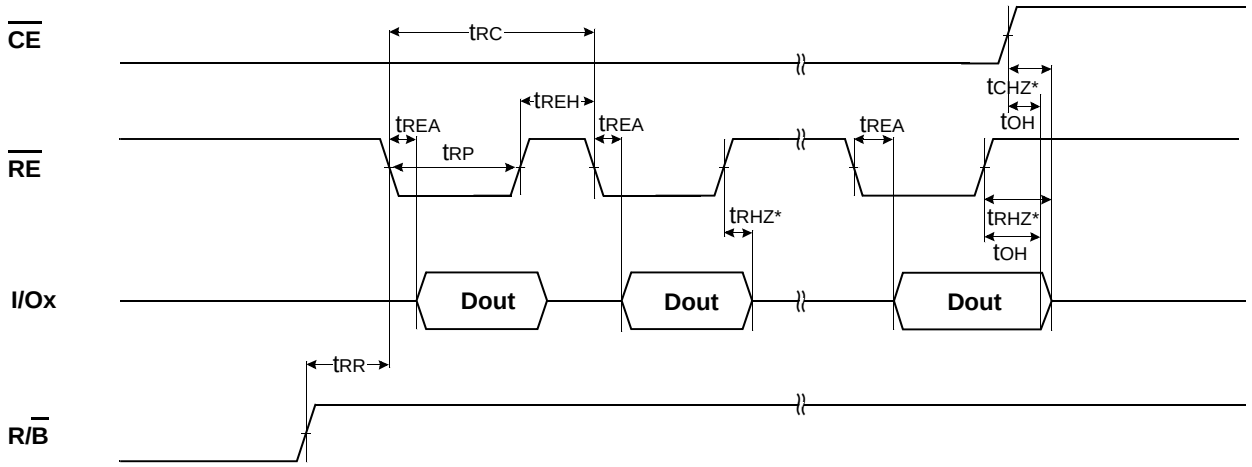
*** Address Latch Cycle**



Input Data Latch Cycle

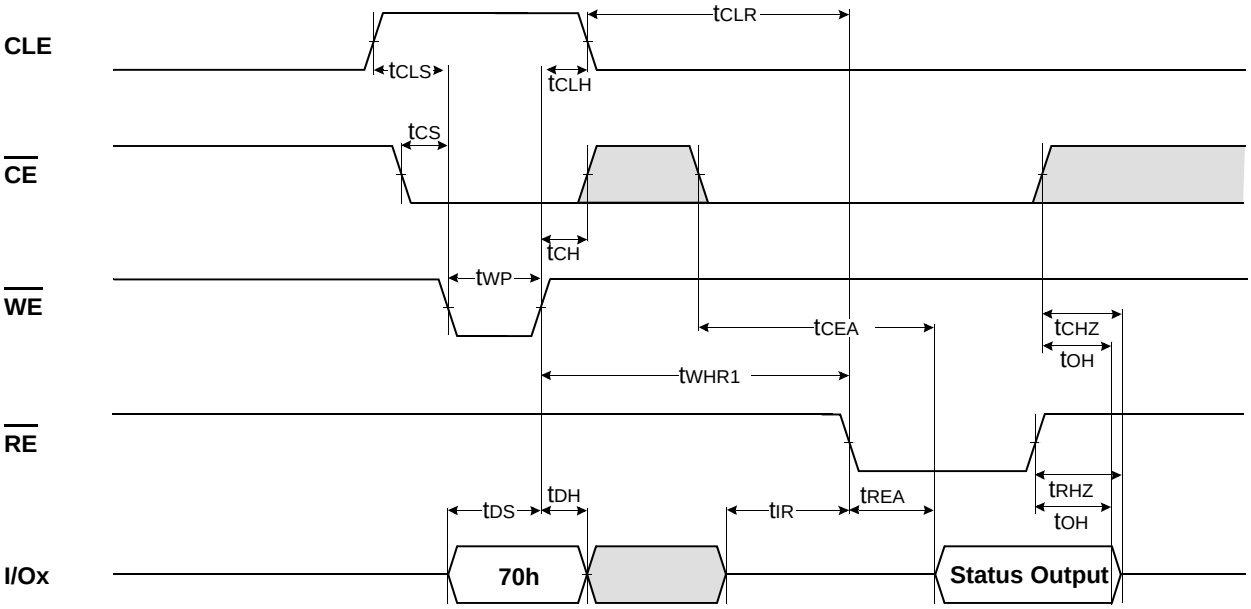


Sequential Out Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

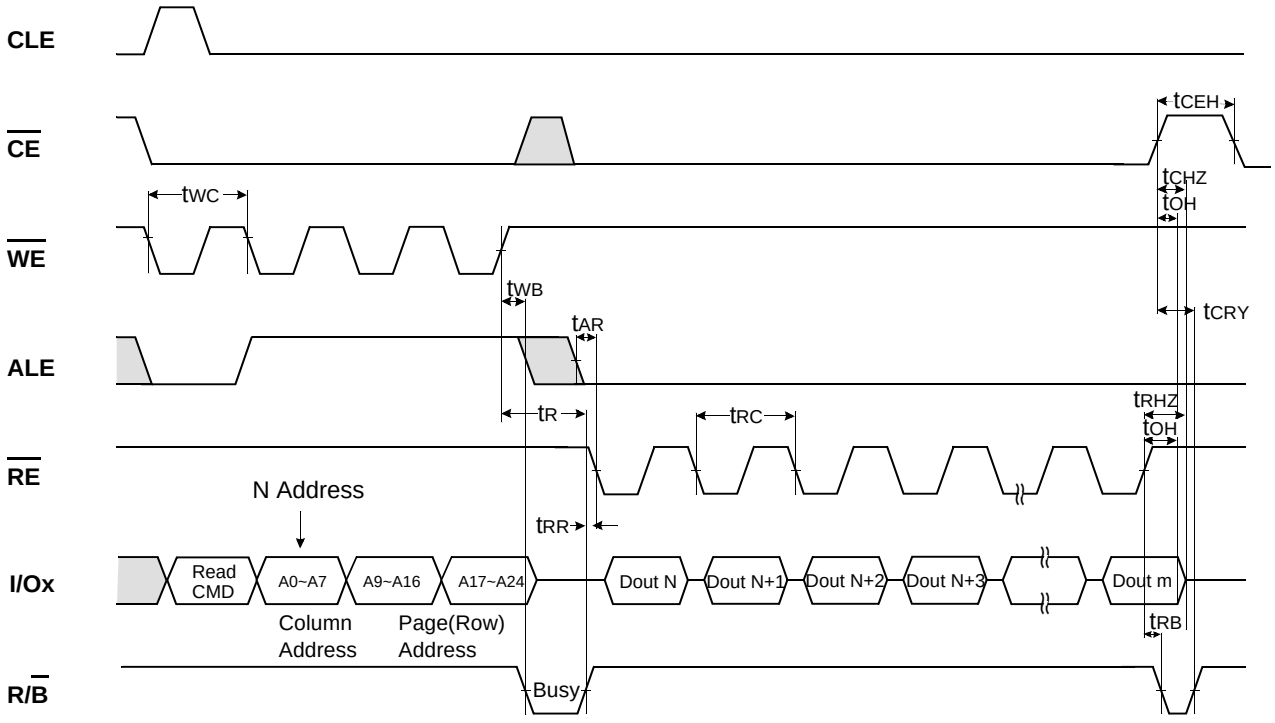


NOTE : 1.Transition is measured ±200mV from steady state voltage with load.
2.This parameter is sampled and not 100% tested.

*** Status Read Cycle**

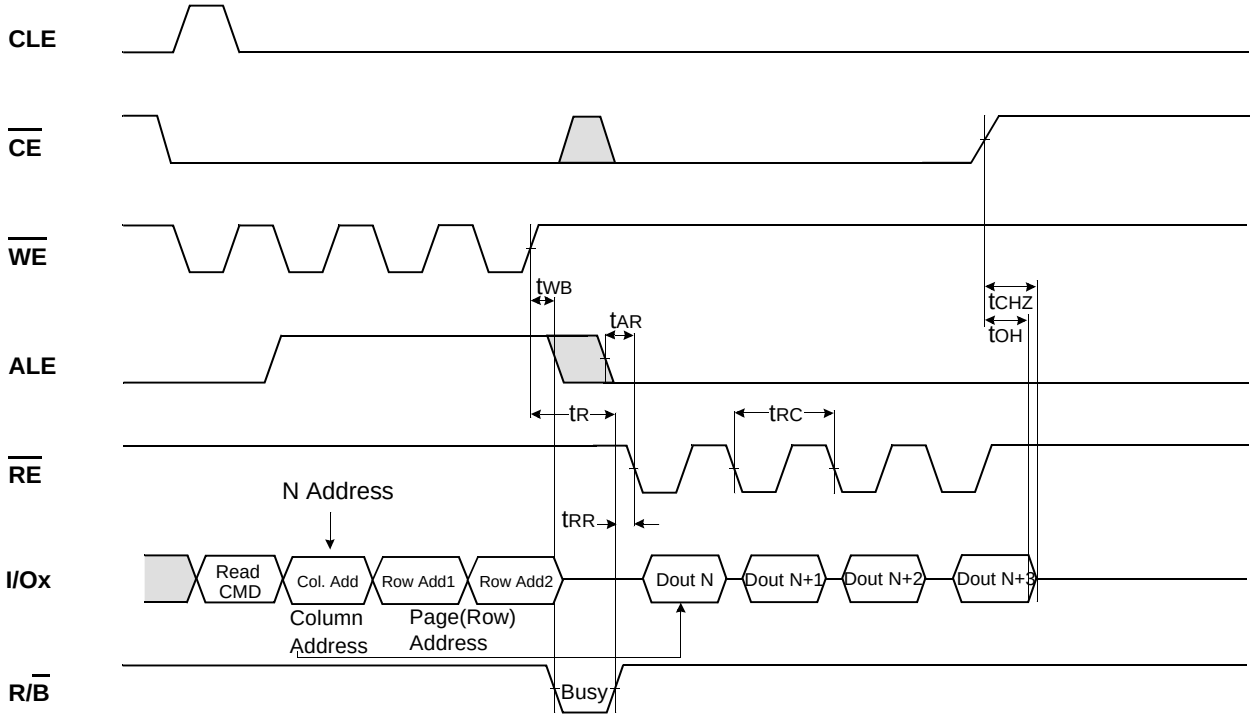


READ1 OPERATION(READ ONE PAGE)

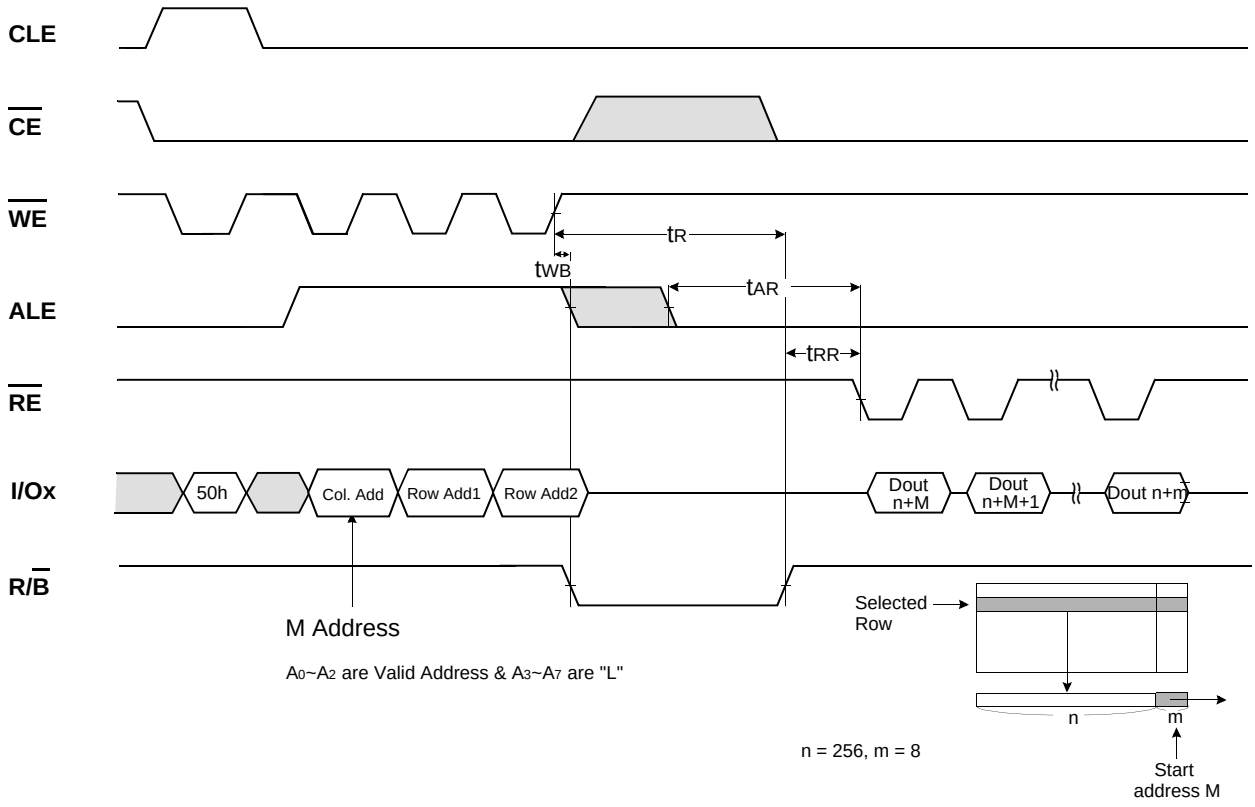


m = 264 , Read CMD = 00h

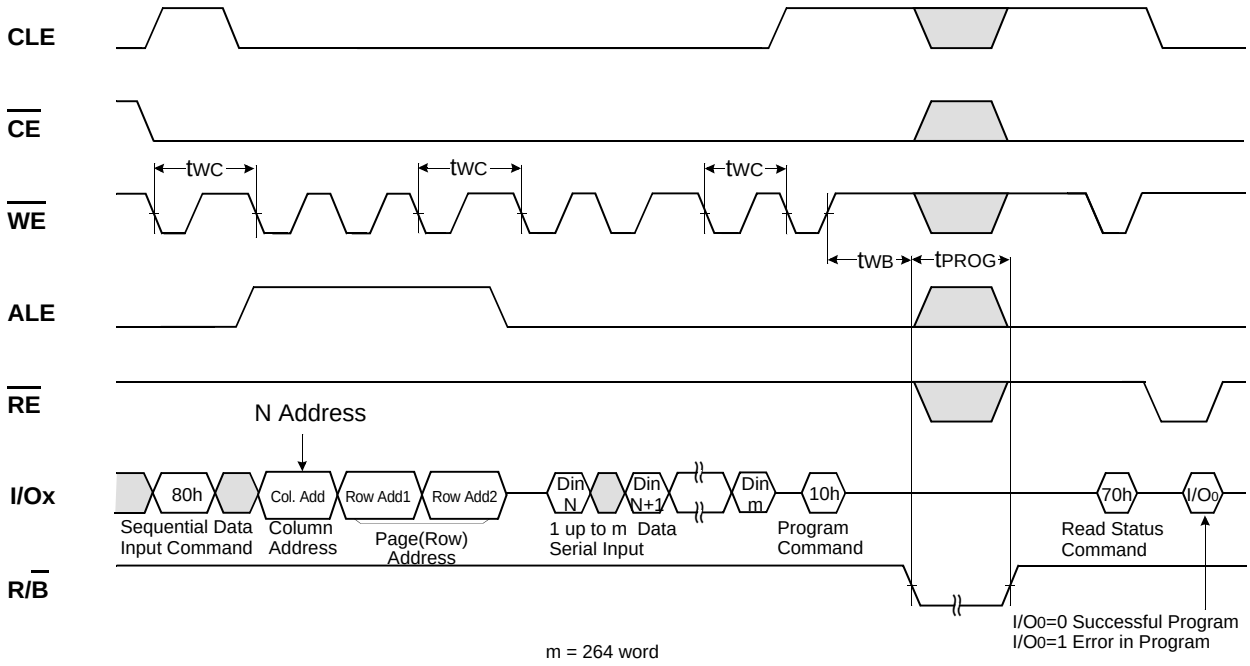
READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)



READ2 OPERATION (READ ONE PAGE)

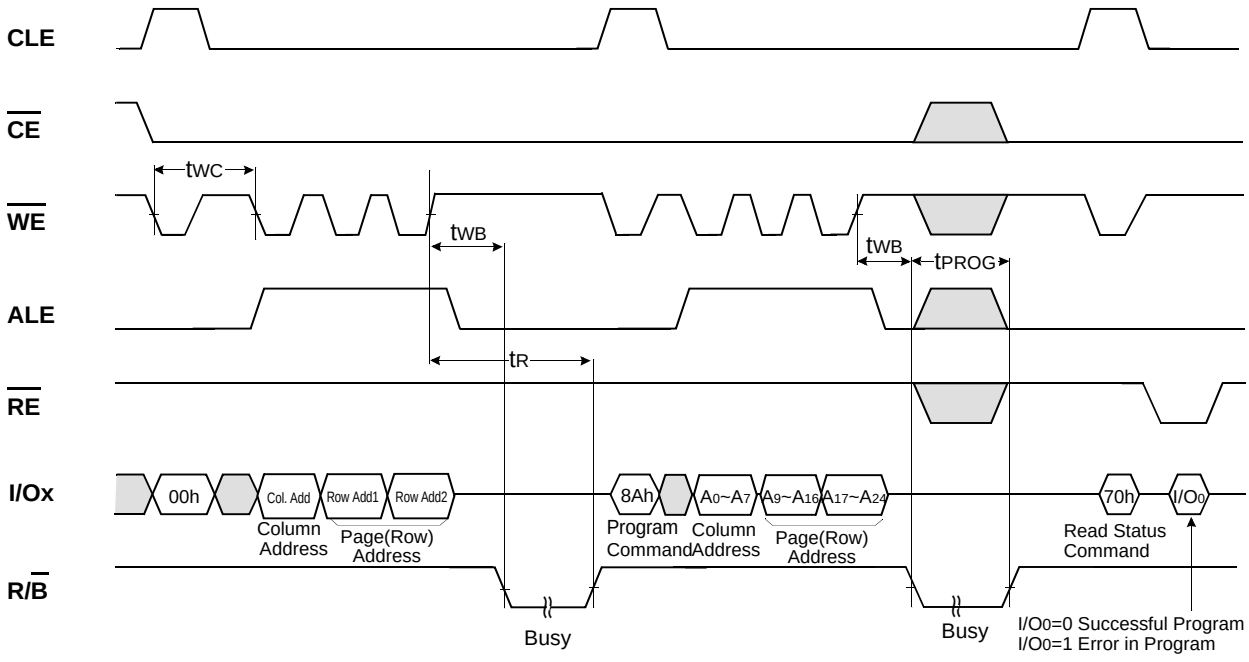


PAGE PROGRAM OPERATION

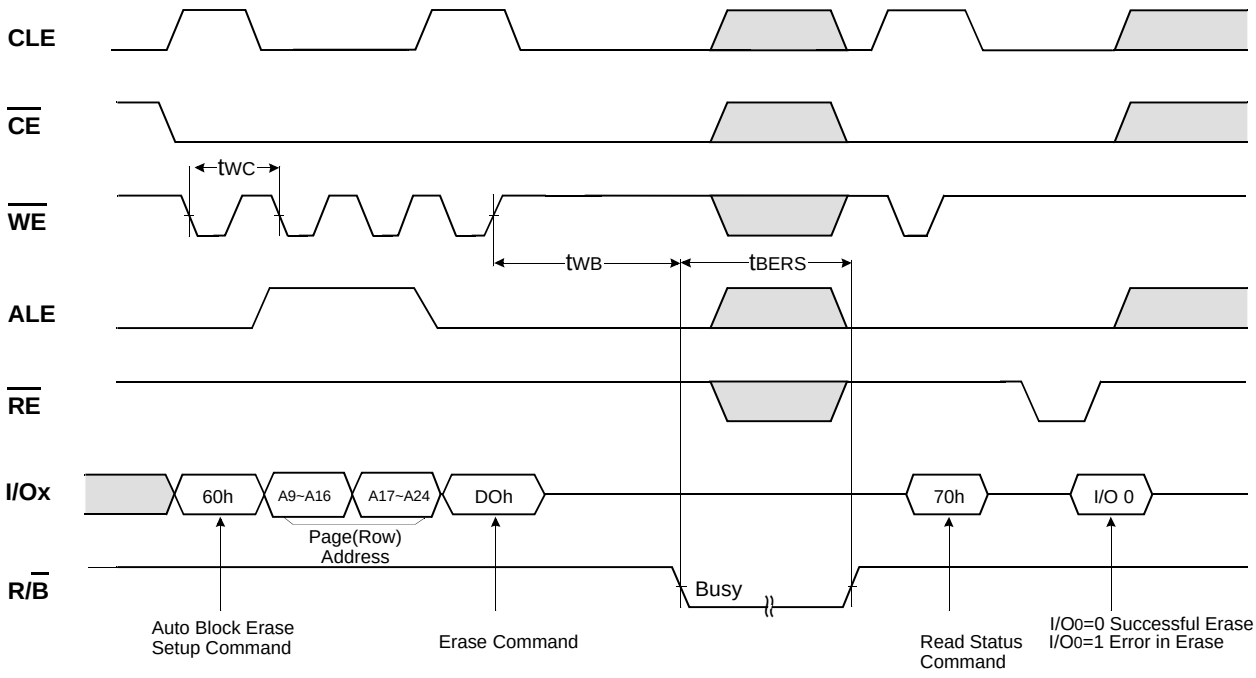


m = 264 word

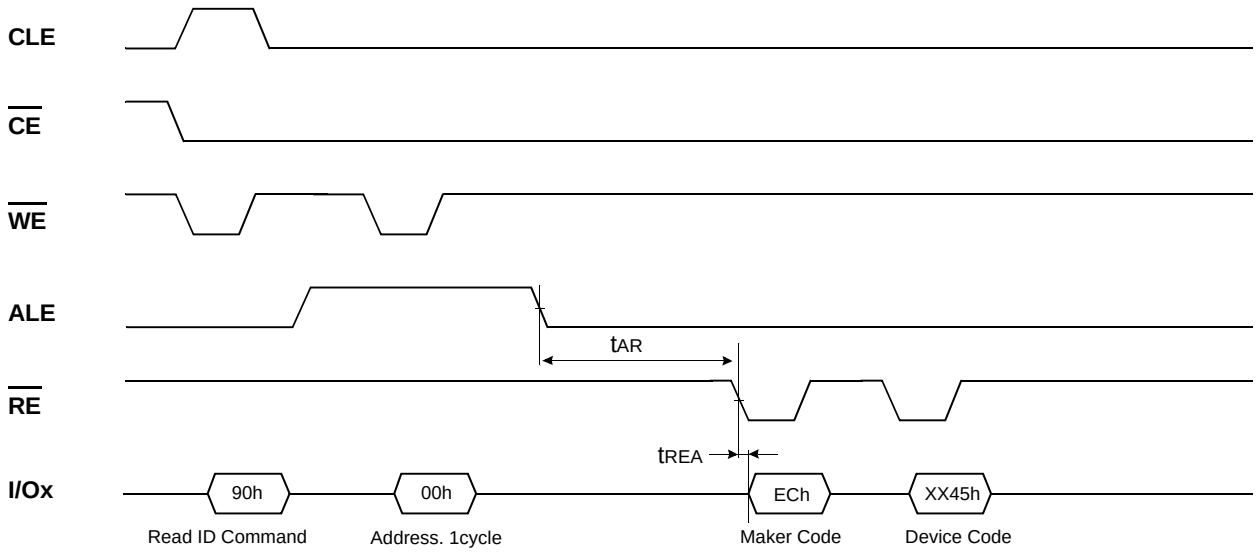
COPY-BACK PROGRAM OPERATION



BLOCK ERASE OPERATION (ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION



DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operations are available : random read, serial page read.

The random read mode is enabled when the page address is changed. The 264 words of data within the selected page are transferred to the data registers in less than 10μs(t_R). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address[column 255 /263 depending on the state of GND input pin].

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 256~263 words may be selectively accessed by writing the Read2 command with GND input pin low. Addresses A_0~A_2 set the starting address of the spare area while addresses A_3~A_7 must be "L". The Read1 command is needed to move the pointer back to the main area. Figures 6, 7 show typical sequence and timings for each read operation.

Figure 6. Read1 Operation

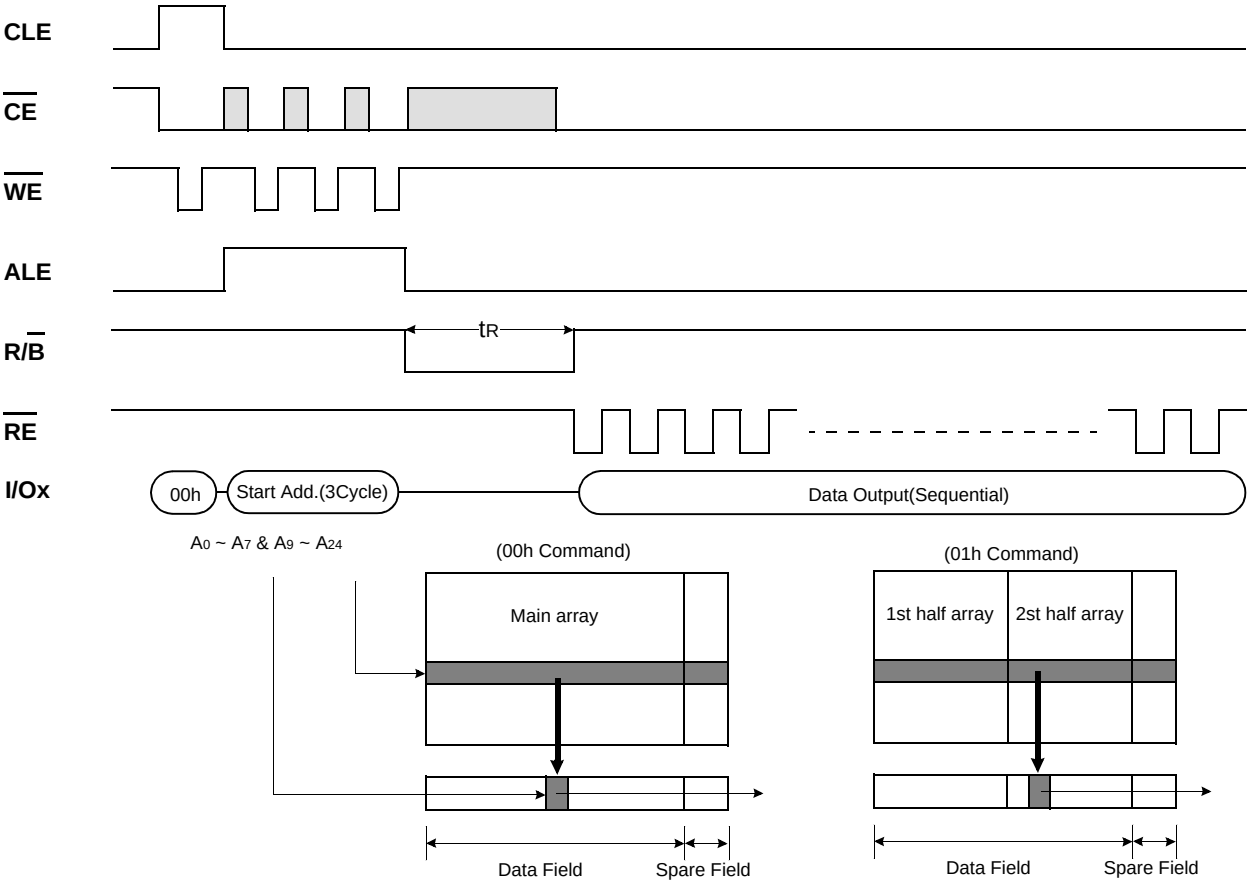
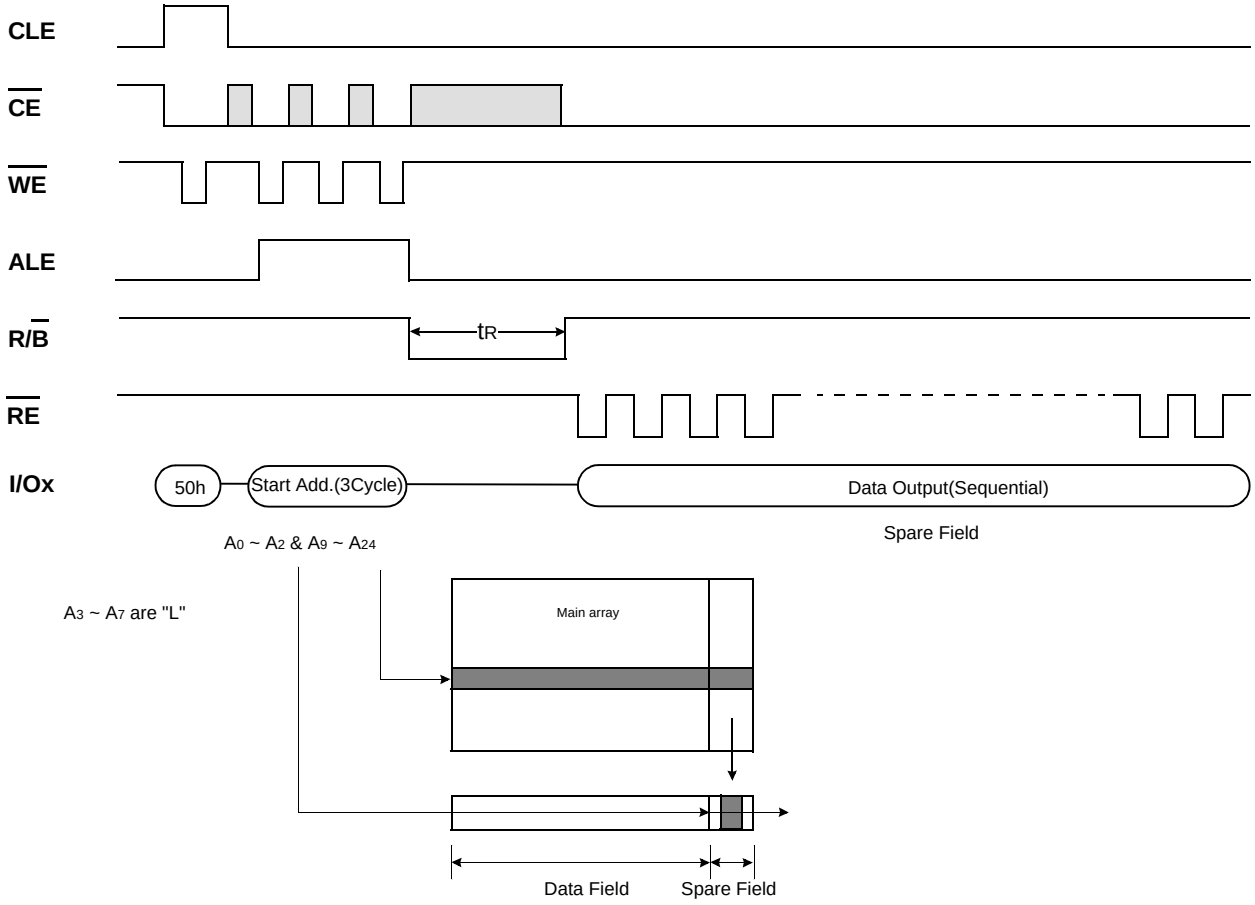


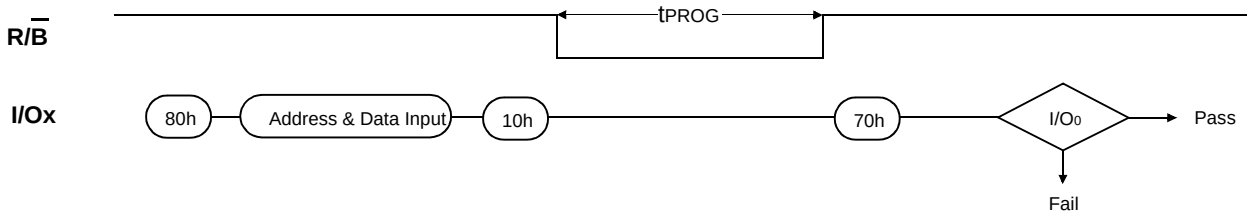
Figure 7. Read2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a word or consecutive words up to 264, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 264 words of data may-be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The words other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

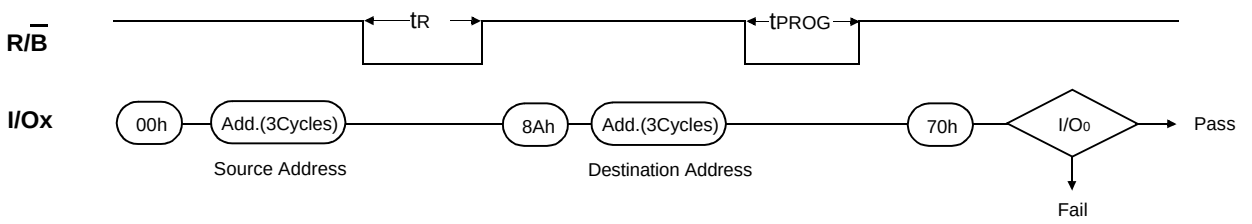
Figure 8. Program Operation



COPY-BACK PROGRAM

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the array to another page within the same array without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command with the address of the source page moves the whole 264words data into the internal buffer. As soon as the Flash returns to Ready state, copy-back programming command "8Ah" may be given with three address cycles of target page followed. The data stored in the internal buffer is then programmed directly into the memory cells of the destination page. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Since the memory array is internally partitioned into two different planes, copy-back program is allowed only within the same memory plane. Thus, A14, the plane address, of source and destination page address must be the same.

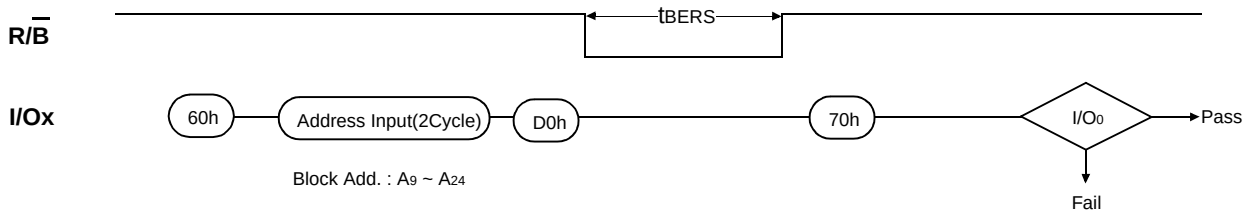
Figure 9. Copy-Back Program Operation



BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{14} to A_{24} is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 10 details the sequence.

Figure 10. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

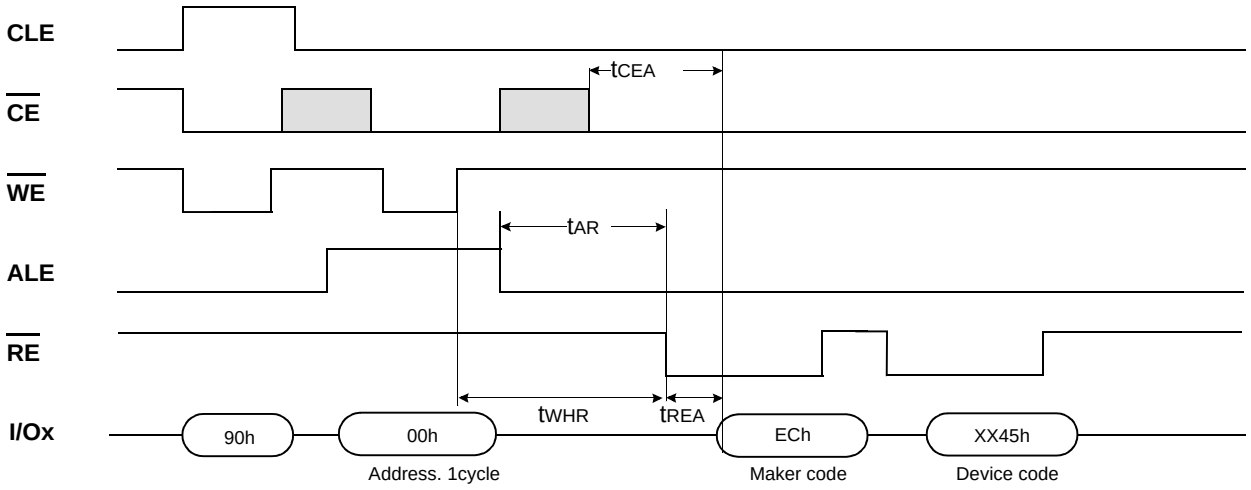
Table 3. Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected
I/O 8~15	Not use	Don't care

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 11 shows the operation sequence.

Figure 11. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 4 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 12 below.

Figure 12. RESET Operation

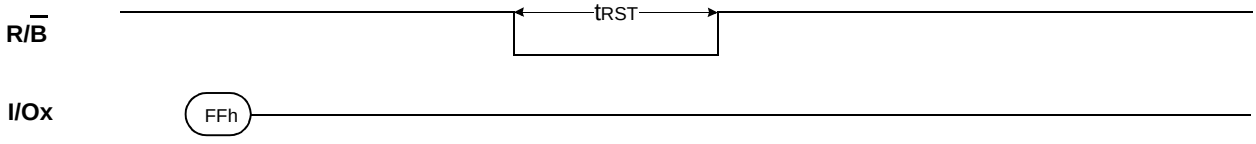
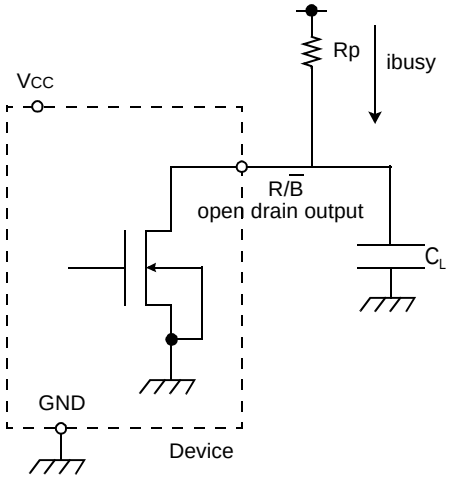


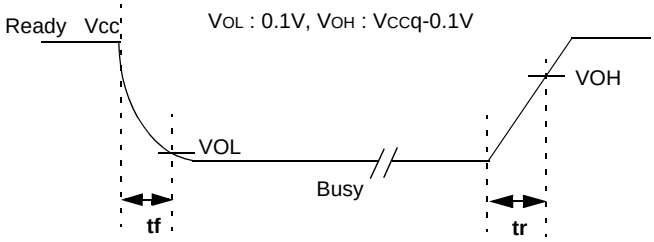
Table4. Device Status

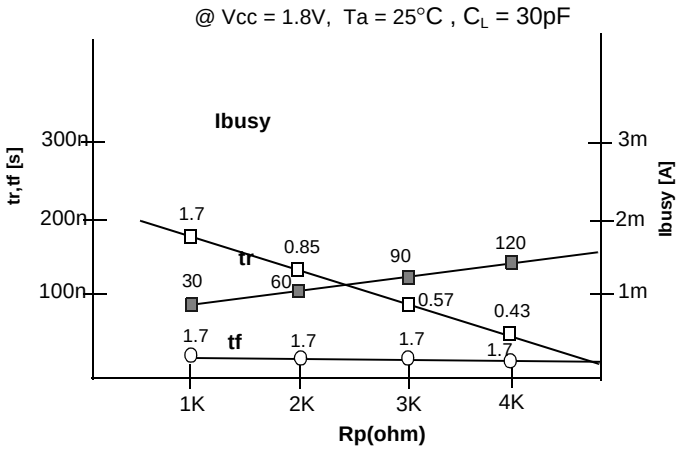
	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/BUSY

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.







Rp value guidance

$$Rp(min, 1.8V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

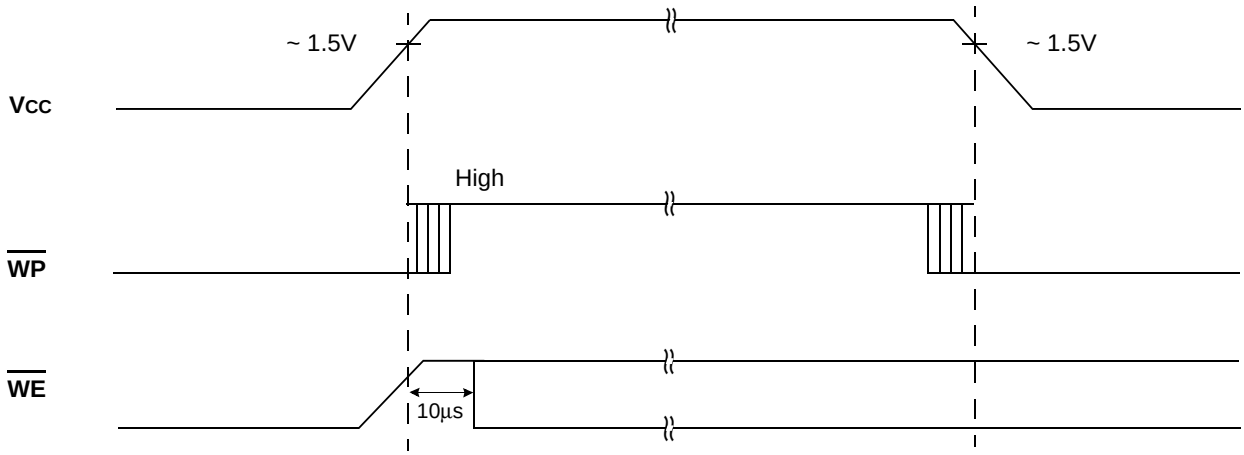
where I_L is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 10μs is required before internal circuit gets ready for any command sequences as shown in Figure 13. The two step command sequence for program/erase provides additional software protection.

Figure 13. AC Waveforms for Power Transition

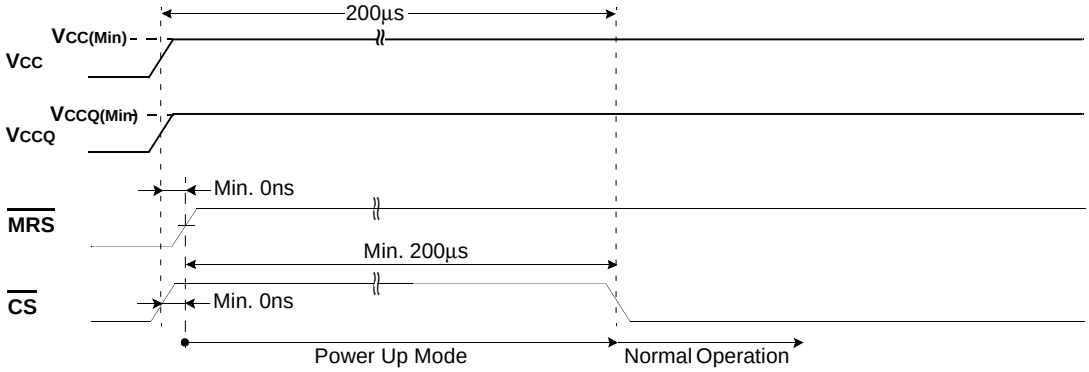


64Mb(4M x 16)
Burst UtRAM B-Die

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minimum 200µs with $\overline{CS}$ and $\overline{MRS}$ high.

TIMING WAVEFORM OF POWER UP



(POWER UP)

1. After V_{CC} reaches V_{CC}(Min.), wait 200µs with $\overline{CS}$ and $\overline{MRS}$ high. Then the device gets into the normal operation.

FUNCTIONAL DESCRIPTION for ASYNCHRONOUS MODE(A15=0)

$\overline{CS}$	$\overline{MRS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
H	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	DPD or PAR
L	H	H	H	X[1)]	X[1)]	High-Z	High-Z	Output Disabled	Active
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	H	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	Word Write	Active
L	L	H	L	X[1)]	X[1)]	High-Z	High-Z	Mode Register Set	Active

1. X must be low or high state.
2. In asynchronous mode, Clock and $\overline{ADV}$ are ignored.

FUNCTIONAL DESCRIPTION for SYNCHRONOUS MODE(A15=1)

$\overline{CS}$	$\overline{MRS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[2)]	X[2)]	Deselected	Standby
H	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[2)]	X[2)]	Deselected	DPD or PAR
L	H	H	H	X[1)]	X[1)]	High-Z	High-Z	X[2)]	H	Output Disabled	Active
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	X[2)]	H	Output Disabled	Active
L	H	X[1)]	H	X[1)]	X[1)]	High-Z	High-Z	⎍	⎍	Read Add. Input Load	Active
L	H	L	H	L	H	Dout	High-Z	⎍	H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	⎍	H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	⎍	H	Word Read	Active
L	H	H	L	L	H	Din	High-Z	X[2)]	L or ⎍	Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	X[2)]	L or ⎍	Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	X[2)]	L or ⎍	Word Write	Active
L	L	H	L	X[1)]	X[1)]	High-Z	High-Z	X[2)]	L	Mode Register Set	Active

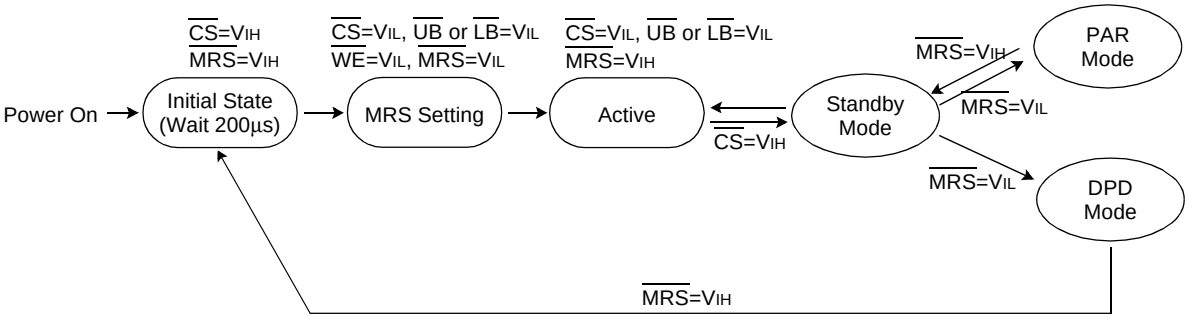
1. X must be low or high state.
2. X means "Don't care"(can be low, high or toggling).

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Power supply voltage relative to Vss	V_{CC}	-0.2 to 3.6V	V
Output power supply voltage relative to Vss	V_{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

STANDBY MODE STATE MACHINES



NOTE : Default mode after power up is Asynchronous mode and DPD enable. But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up or after getting out of DPD mode.
If Synchronous operation is needed, set A15=1. For more detail, please refer to the Mode Register Set(See Page 36).
Once the device gets out of DPD mode, all the register settings are initialized into the default mode.

For entry to PAR mode, drive $\overline{MRS}$ pin into V_{IL} for over 0.5us(suspend period) during standby mode after MRS setting has been completed(A4=1, A3=0). If $\overline{MRS}$ pin is driven into V_{IH} during PAR mode, the device gets back to the standby mode without wake up sequence.

For entry to DPD mode, drive $\overline{MRS}$ pin into V_{IL} for over 0.5us(suspend period) during standby mode after MRS setting has been completed(A4=0). To get out of the DPD mode, drive $\overline{MRS}$ pin into V_{IH} with wake up sequence(See Page 51).

DPD mode or PAR mode can be selected through Mode Register Set(See Page 36).

STANDBY MODE CHARACTERISTIC

Power Mode	Address (Bottom Array)[2)]	Address (Top Array)[2)]	Memory Cell Data	Standby Current (µA, Max)	Wait Time(µs)
Standby(Full Array)	000000h ~ 3FFFFFh	3FFFFFh ~ 000000h	Valid[1)]	150	0
Partial Refresh(3/4 Block)	000000h ~ 2FFFFFh	3FFFFFh ~ 0FFFFFh	Valid[1)]	TBD	0
Partial Refresh(1/2 Block)	000000h ~ 1FFFFFh	3FFFFFh ~ 1FFFFFh	Valid[1)]	TBD	0
Partial Refresh(1/4 Block)	000000h ~ 0FFFFFh	3FFFFFh ~ 2FFFFFh	Valid[1)]	TBD	0
Deep Power Down	000000h ~ 3FFFFFh	3FFFFFh ~ 000000h	Invaild	20	200

1. Only the data in the refreshed block are valid
2. PAR Array can be selected through Mode Register Set(See Page 36).

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	2.7	2.9	3.1	V
I/O power supply voltage	V_{CCQ}	1.7	1.85	2.0	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	1.5	-	V_{DDQ}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to V_{CCQ}		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to V_{CCQ}		-1	-	1	µA
Average operating current	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{MRS}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}		-	-	45	mA
Output low voltage	V_{OL}	I_{OL}=0.1mA		-	-	0.2	V
Output high voltage	V_{OH}	I_{OH}=-0.1mA		1.4	-	-	V
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥V_{CCQ}-0.2V, $\overline{MRS}$≥V_{CCQ}-0.2V, Other inputs=Vss to V_{CCQ}		-	-	150	µA
Partial Refresh Current	I_{SBP}[1)]	$\overline{MRS}$≤0.2V, $\overline{CS}$≥V_{CCQ}-0.2V Other inputs=Vss to V_{CCQ}	3/4 Block	-	-	TBD	µA
			1/2 Block	-	-	TBD	
			1/4 Block	-	-	TBD	
Deep Power Down	I_{SBD}	$\overline{MRS}$≤0.2V, $\overline{CS}$≥V_{CCQ}-0.2V, Other inputs=Vss to V_{CCQ}		-	-	20	µA

1. Full Array Partial Refresh Current(I_{SBP}) is same as Standby Current(I_{SB1}).

DEVICE OPERATION

The device has several modes : Synchronous Burst Read mode, Asynchronous Write mode, Standby mode, Deep Power Down(DPD) mode and Partial Array Refresh(PAR) mode.
Deep Power Down(DPD) mode and Partial Array Refresh(PAR) mode are defined through Mode Register Set(MRS) option. Mode Register Set(MRS) option also defines Burst Length, Burst Type and First Access Latency Count at Synchronous Burst Read mode. To set Mode Register, the system must drive CS, ADV, WE and MRS to V_{IL} and drive OE to V_{IH} during valid address. To get into the Standby mode, the system must drive CS to V_{IH}. To get into the Deep Power Down(DPD) mode, the system must drive CS to CMOS V_{IH}(VCC-0.2V) and MRS to CMOS V_{IL}(0.2V).

Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of UtRAM. It programs Partial Array Refresh(PAR), Deep Power Down(DPD) mode, Burst Length, Burst Type, First Access Latency Count and various vendor specific options to make UtRAM useful for a variety of different applications. The default values of mode register are defined, therefore unless user specifies the specific modes, the device runs at default modes. If user wants to set modes other than default modes, user should write specific mode value on mode register after power up. The mode register is written by driving CS, ADV, WE and MRS to V_{IL} and driving OE to V_{IH} during valid address. The mode register is divided into various fields depending on the fields of functions. The Partial Array Refresh(PAR) field uses A0~A3, Deep Power Down(DPD) field uses A4, Burst Length field uses A6~A7, Burst Type uses A8 and First Access Latency Count uses A9~A11. Refer to the Table below for detailed Mode Register Setting.

Mode Register Setting according to field of function

Address	An~A16	A15	A14~A12	A11~A9	A8	A7~A6	A5	A4	A3	A2	A1~A0
Function	RFU	MS	RFU	Latency	BT	BL	RFU	DPD	PAR	PARA	PARS

NOTE : RFU(Reserved for Future Use), BT(Burst Type), BL(Burst Length), DPD(Deep Power Down), PAR(Partial Array Refresh), PARA(Partial Array Refresh Array), PARS(Partial Array Refresh Size), MS(Mode Select)

Mode Select		First Access Latency Count				Burst Type		Burst Length		
A15	Async./Sync.	A11	A10	A9)	Latency	A8	Type	A7	A6	Length
0	**Async. Mode**	0	0	0	Reserved	0	Linear	0	0	4
1	Sync. Mode	0	0	1	3	1	Interleave	0	1	8
		0	1	0	4			1	0	16
		0	1	1	5			1	1	Reserved
		1	0	0	6					
		1	0	1	Reserved					
		1	1	0	Reserved					
		1	1	1	Reserved					

Deep power Down		Partial Array Refresh		PAR Array		PAR Size		
A4	DPD	A3	PAR	A2	PARA	A1	A0	PARS
0	**DPD Enable**	0	PAR Enable	0	Bottom Array	0	0	Full Array
1	DPD Disable	1	Reserved	1	Top Array	0	1	48Mb Array
						1	0	32Mb Array
						1	1	16Mb Array

NOTE : Default mode(when user does not write any specific value to the mode register) is Async. mode and DPD enable.
Even though the device used to work in the sync. mode, once the device gets out of DPD mode, all the register settings are initialized into the default mode.But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up or after getting out of DPD mode.
DPD mode has a higher priority to PAR mode.

Asynchronous Read Operation

Asynchronous read operation starts when $\overline{CS}$, $\overline{OE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to V_{IL} under the valid address.($\overline{MRS}$ and $\overline{WE}$ should be driven to V_{IH} during asynchronous read operation)

Asynchronous Write Operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to V_{IL} under the valid address.($\overline{MRS}$ and $\overline{OE}$ should be driven to V_{IH} during write operation.)

Asynchronous Write Operation in Synchronous Mode

A write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ & $\overline{LB}$ are driven to V_{IL} under the valid address. Clock input does not have any affect to the write operation.(MRS and OE should be driven to V_{IH} during write operation. ADV can be toggling for address latch or can be driven to V_{IL})

Synchronous Burst Read Operation

The device supports Linear Synchronous Burst Read mode and Interleave Synchronous Burst Read mode.
For the optimized Burst Mode to each system, the system should determine how many clock cycles are desirable for the initial word of each burst access(First Access Latency Count), how many words the device outputs at an access(Burst Length) and which type of burst operation(Burst Type : Linear or Interleave) is desired.(See Table "Mode Register Set")

Clock(CLK)

The clock input is used as the reference for synchronous burst read operation of UtRAM. Synchronous burst read operation is synchronized to the rising edge of the clock. The clock transitions must swing between V_{IL} and V_{IH}.

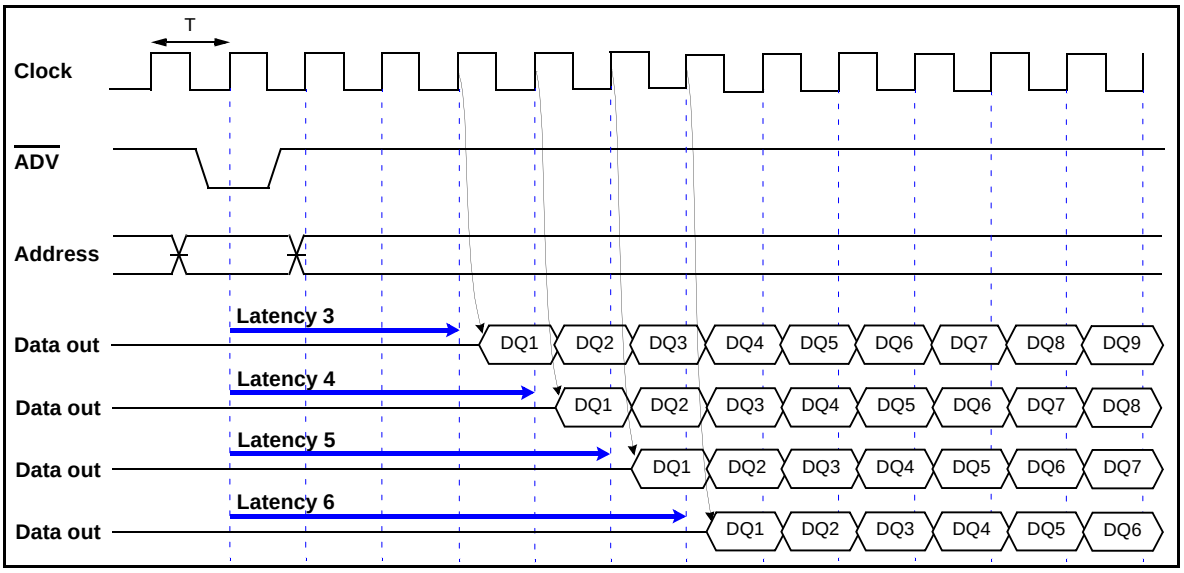
First Access Latency Count

The First Access Latency Count configuration tells the device how many clocks must elapse from $\overline{ADV}$ de-assertion(V_{IH}) before the first data word should be driven onto its data pins. This value depends on the input clock frequency.
The supported Latency Count is as follows.

Latency Count support : 3, 4, 5, 6

Clock Frequency	Upto 54MHz	Upto 40MHz
Latency Count	**4**, 5, 6	**3**, 4, 5, 6

First Access Latency Configuration



NOTE : Other First Access Latency Configuration settings are reserved.
Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse

Burst Sequence

Start Address	Burst Address Sequence					
	4 word Burst		8 word Burst		16 word Burst	
	Linear	Interleave	Linear	Interleave	Linear	Interleave
0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4...14-15	0-1-2-3-4...14-15
1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4...14-15-0	1-0-3-2-5...15-14
2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4...14-15-0-1	2-3-0-1-6...12-13
3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5...15-0-1-2	3-2-1-0-7...13-12
4			4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6...15-0-1-2-3	4-5-6-7-0...10-11
5			5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6...15-0-1-2-3-4	5-4-7-6-1...11-10
6			6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7...15-0-1-2-3-4-5	6-7-4-5-2...8-9
7			7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8...15-0-1...5-6	7-6-5-4-3...9-8
~					~	~
14					14-15-0-1...12-13	14-15-12-13-10...0-1
15					15-0-1...12-13-14	15-14-13-12-11...1-0

Burst Stop

Burst stop is used when the system wants to stop burst operation on special purpose. If driving $\overline{CS}$ to V_{IH} during burst read operation, then burst operation will be stopped. During burst read operation, the new burst operation by ADV can not be issued. The new burst operation can be issued only after the previous burst operation is finished.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load: C_L=50pF

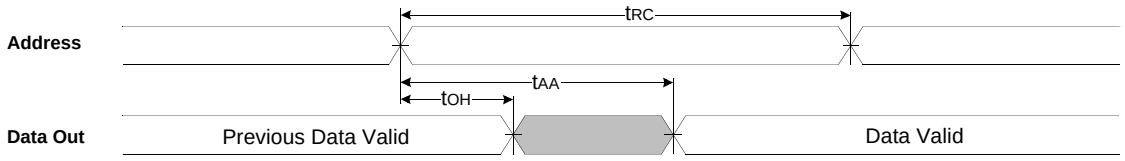
ASYNCHRONOUS AC CHARACTERISTICS (V_{CC}=2.7~3.1V, V_{CCQ}=1.7~2.0V, T_A=-40 to 85°C)

Parameter List		Symbol	Speed		Units
			Min	Max	
Async. Read	Read Cycle Time	t_{RC}	85	-	ns
	Address Access Time	t_{AA}	-	85	ns
	Chip Select to Output	t_{CO}	-	85	ns
	Output Enable to Valid Output	t_{OE}	-	40	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	40	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold	t_{OH}	10	-	ns
Async. Write	Write Cycle Time	t_{WC}	85	-	ns
	Chip Select to End of Write	t_{CW}	70	-	ns
	Address Set-up Time to Beginning of Write	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	70	-	ns
	Write Pulse Width	t_{WP}	60[1)]	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Data to Write Time Overlap	t_{DW}	35	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
MRS	$\overline{MRS}$ Enable to Register Write Start	t_{MW}	0	500	ns
	Register Write Recovery Time	t_{RWR}	5	-	ns
	End of Write to $\overline{MRS}$ Disable	t_{WU}	0	-	ns

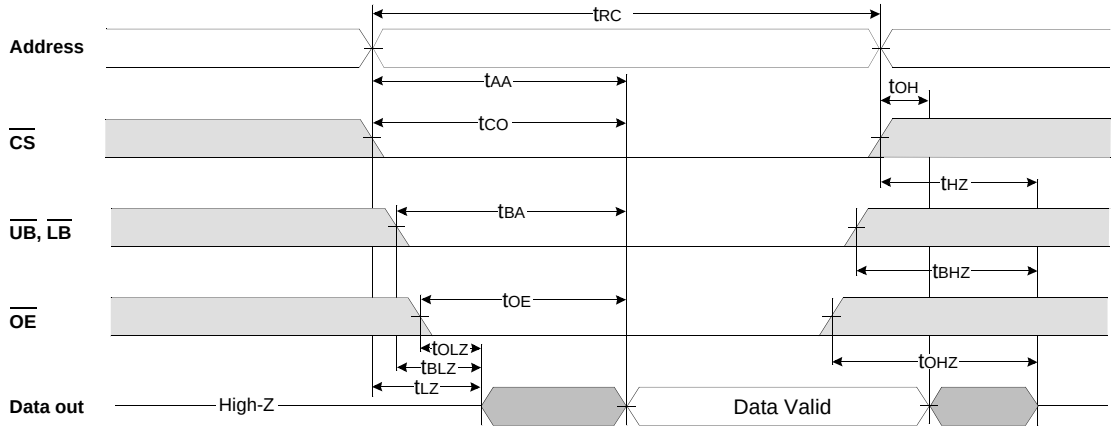
1. t_{WP}(min)=85ns for continuous write operation over 50 times.

ASYNCHRONOUS READ TIMING WAVEFORM

TIMING WAVEFORM OF ASYNCHRONOUS READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{MRS}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF ASYNCHRONOUS READ CYCLE(2)($\overline{MRS}$=$\overline{WE}$=V_{IH})

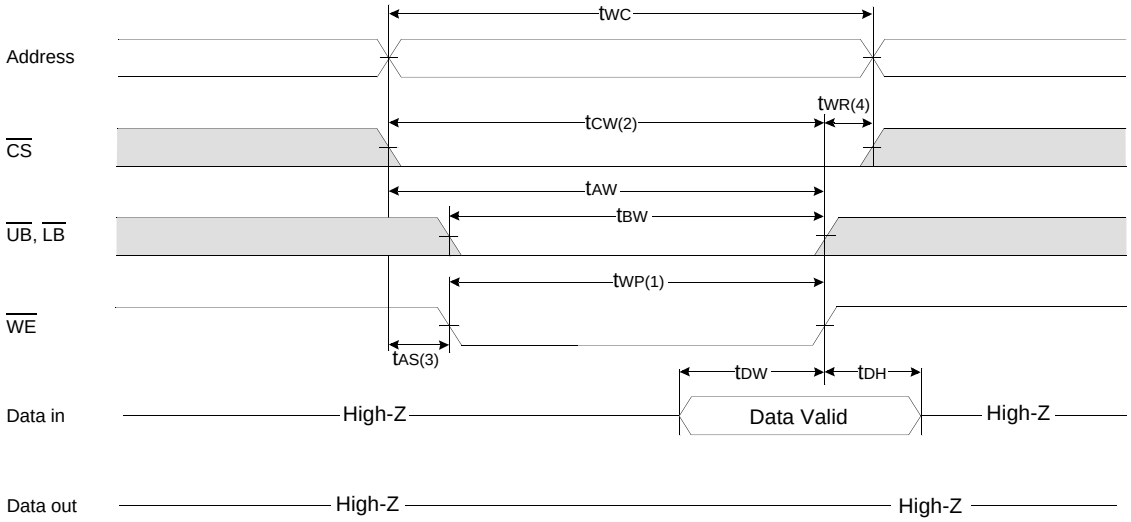


(ASYNCHRONOUS READ CYCLE)

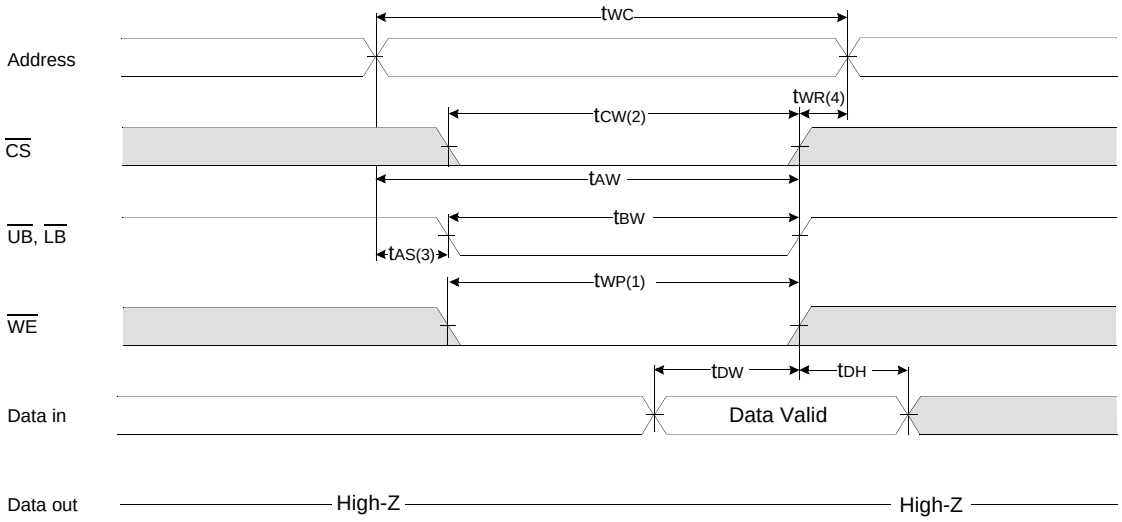
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.
5. In asynchronous mode, Clock and ADV are ignored.

ASYNCHRONOUS WRITE TIMING WAVEFORM

TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{UB}$ & $\overline{LB}$ Controlled)



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. In asynchronous mode, Clock and $\overline{ADV}$ are ignored.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load: C_L=50pF

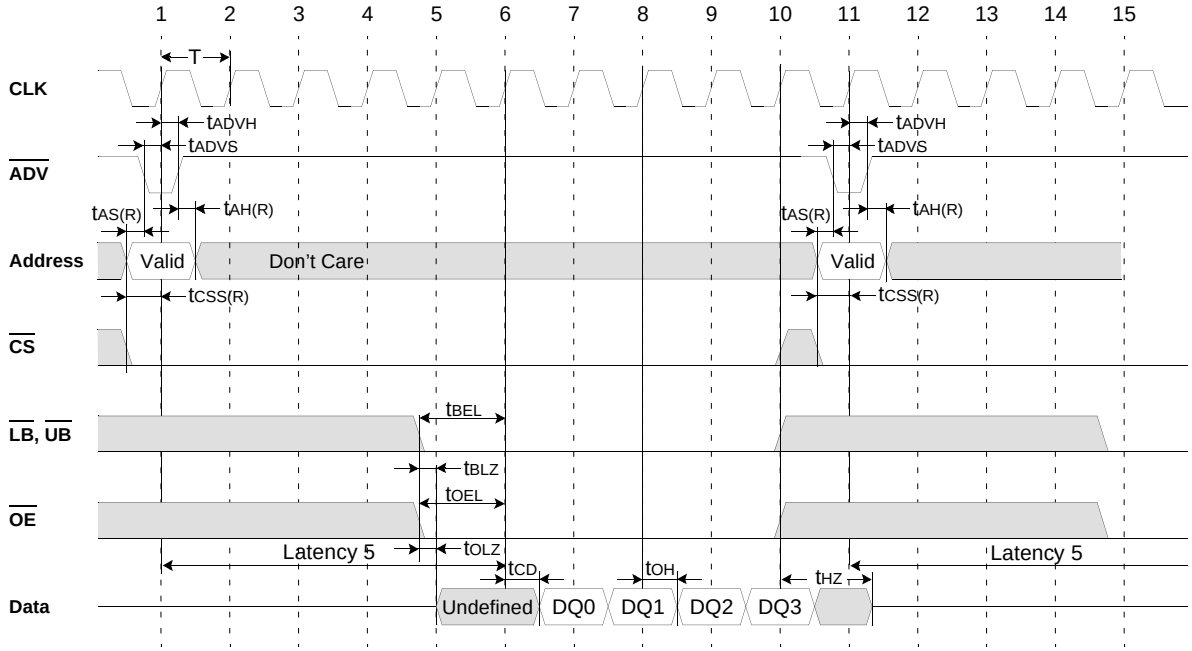
SYNCHRONOUS AC CHARACTERISTICS (V_{CC}=2.7~3.1V, V_{CCQ}=1.7~2.0V, T_A=-40 to 85°C, Maximum Main Clock Frequency=54MHz)

Parameter List		Symbol	Speed		Units
			Min	Max	
Sync. Burst Read	Clock Cycle Time	T	18.5	200	ns
	Address Set-up Time to $\overline{ADV}$ Falling	$t_{AS(R)}$	0	-	ns
	Address Hold Time from $\overline{ADV}$ Rising	$t_{AH(R)}$	7	-	ns
	$\overline{ADV}$ Setup Time	t_{ADVS}	7	-	ns
	$\overline{ADV}$ Hold Time	t_{ADVH}	7	-	ns
	$\overline{CS}$ Setup Time to Clock Rising	$t_{CSS(R)}$	7	-	ns
	$\overline{CS}$ Low Hold Time from Clock	t_{CSLH}	5	-	ns
	$\overline{CS}$ High Pulse Width	t_{CSHP}	5	-	ns
	$\overline{ADV}$ High Pulse Width	t_{ADHP}	5	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Latency	t_{BEL}	1	-	Clock
	Output Enable to End of Latency	t_{OEL}	1	-	Clock
	$\overline{UB}$, $\overline{LB}$ Valid to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Latency Clock Rising Edge to Data Output	t_{CD}	-	12	ns
	Output Hold	t_{OH}	3	-	ns
	Output High-Z	t_{HZ}	-	10	ns
Async. Write	Write Cycle Time	t_{WC}[2]	85	-	ns
	Address Set-up Time to $\overline{ADV}$ Falling	$t_{AS(W)}$	0	-	ns
	Address Hold Time from $\overline{ADV}$ Rising	$t_{AH(W)}$	7	-	ns
	$\overline{CS}$ Setup Time to $\overline{ADV}$ Rising	$t_{CSS(W)}$	10	-	ns
	Address Set-up Time to Beginning of Write	t_{AS}	0	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Burst Read End Clock to Next ADV Falling	t_{BEWA}	3	-	ns
	Chip Select to End of Write	t_{CW}	70	-	ns
	Address Valid to End of Write	t_{AW}	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	70	-	ns
	Write Pulse Width	t_{WP}	60[1]	-	ns
	$\overline{WE}$ High Pulse Width	t_{WHP}	5 ns	Latency-1 clock	-
	Data to Write Time Overlap	t_{DW}	35	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
MRS	$\overline{MRS}$ Enable to Register Write Start	t_{MW}	0	500	ns
	Register Write Recovery Time	t_{RWR}	5	-	ns
	End of Write to $\overline{MRS}$ Disable	t_{WU}	0	-	ns

1. t_{WP}(min)=85ns for continuous write operation over 50 times.
2. In ADDRESS LATCH TYPE WRITE TIMING, t_{WC} is same as t_{AW}.

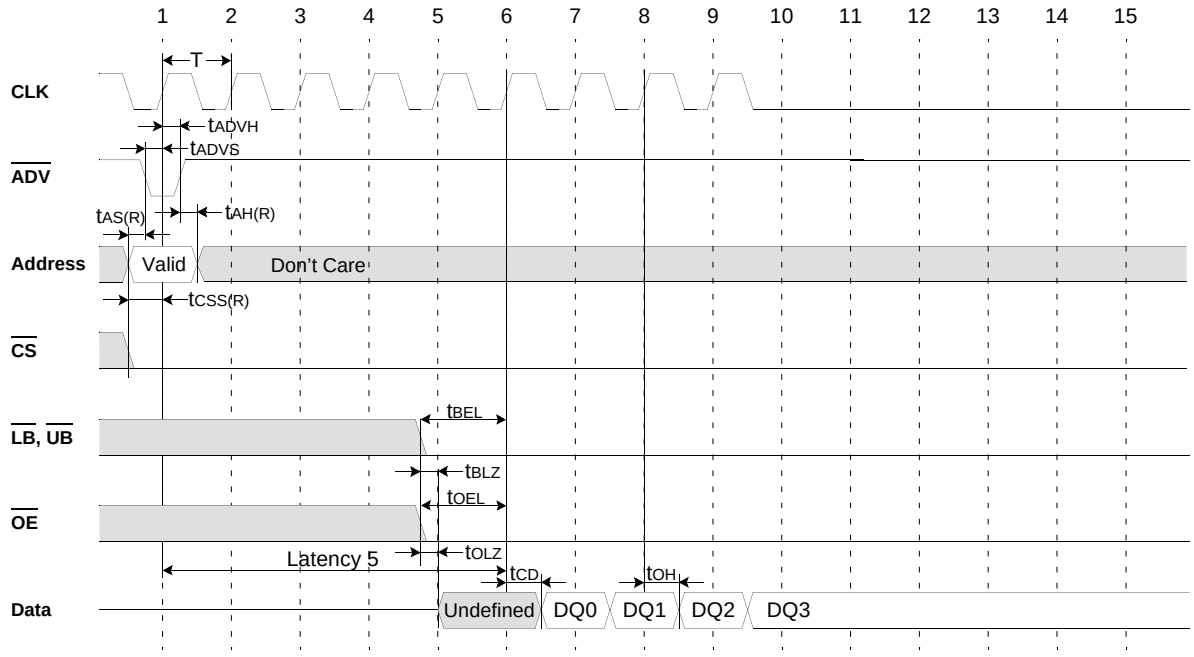
SYNCHRONOUS BURST READ TIMING WAVEFORM

TIMING WAVEFORM OF BURST READ CYCLE(1) [Latency=5, Burst Length=4] ($\overline{WE}$=V_{IH}, $\overline{MRS}$=V_{IH})



(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The new burst operation can be issued only after the previous burst operation is finished.

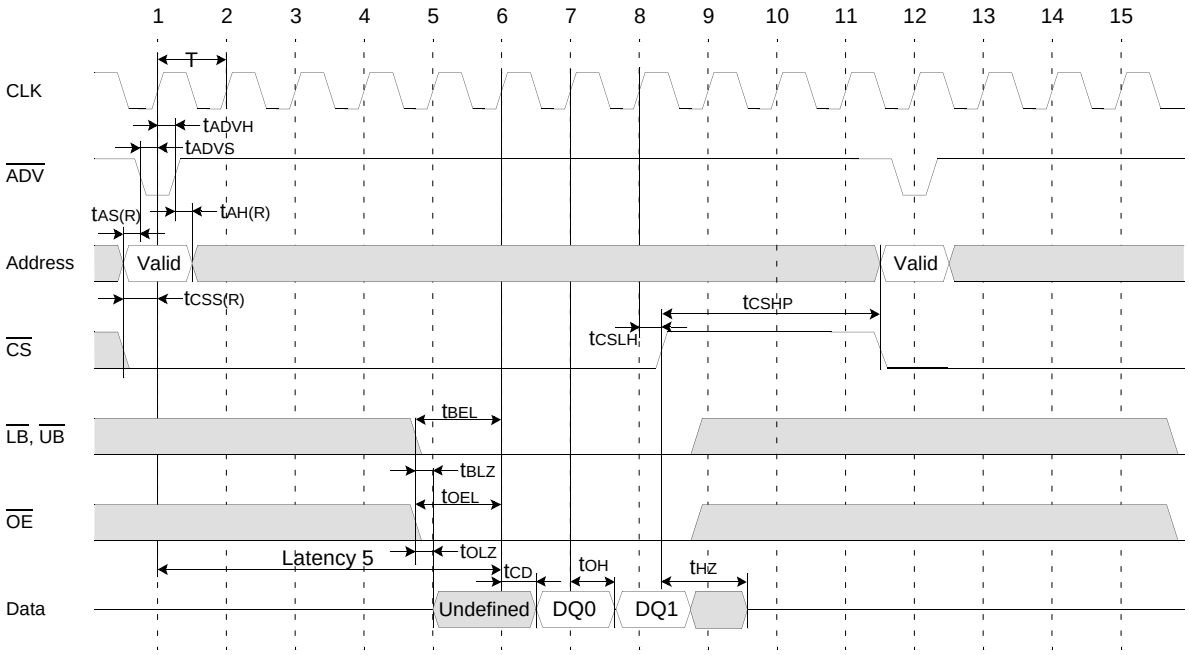
TIMING WAVEFORM OF BURST READ CYCLE(2) [Latency=5, Burst Length=4] ($\overline{WE}$=V_{IH}, $\overline{MRS}$=V_{IH})



(SYNCHRONOUS BURST READ CYCLE)
1.Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.

BURST STOP TIMING WAVEFORM

TIMING WAVEFORM OF BURST STOP by $\overline{CS}$ [Latency=5, Burst Length=4] ($\overline{WE}$=V_{IH}, $\overline{MRS}$=V_{IH})

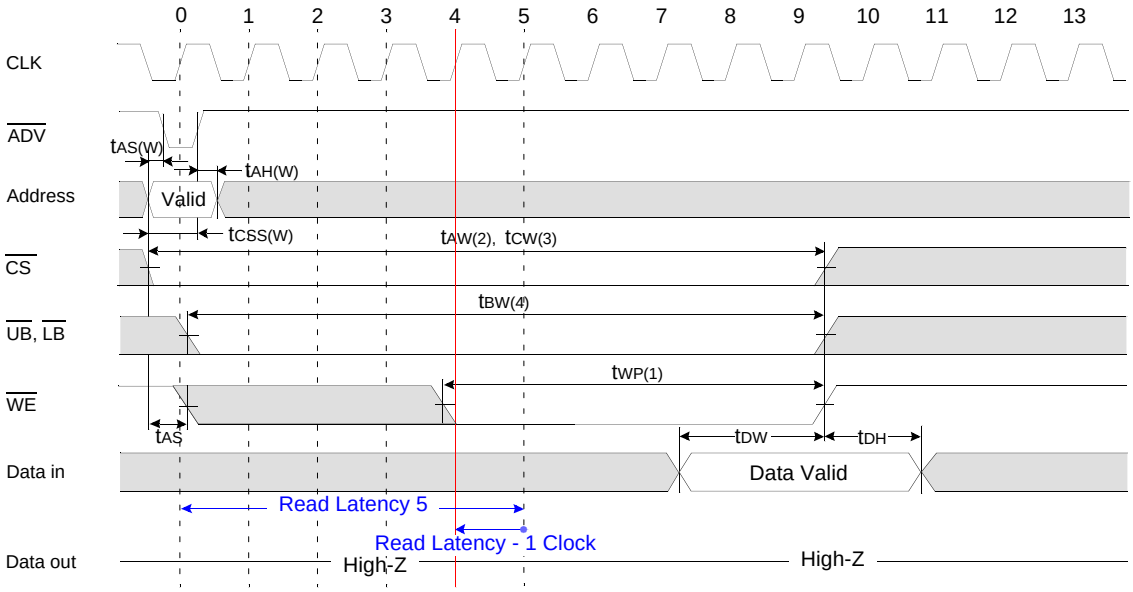


(SYNCHRONOUS BURST STOP)

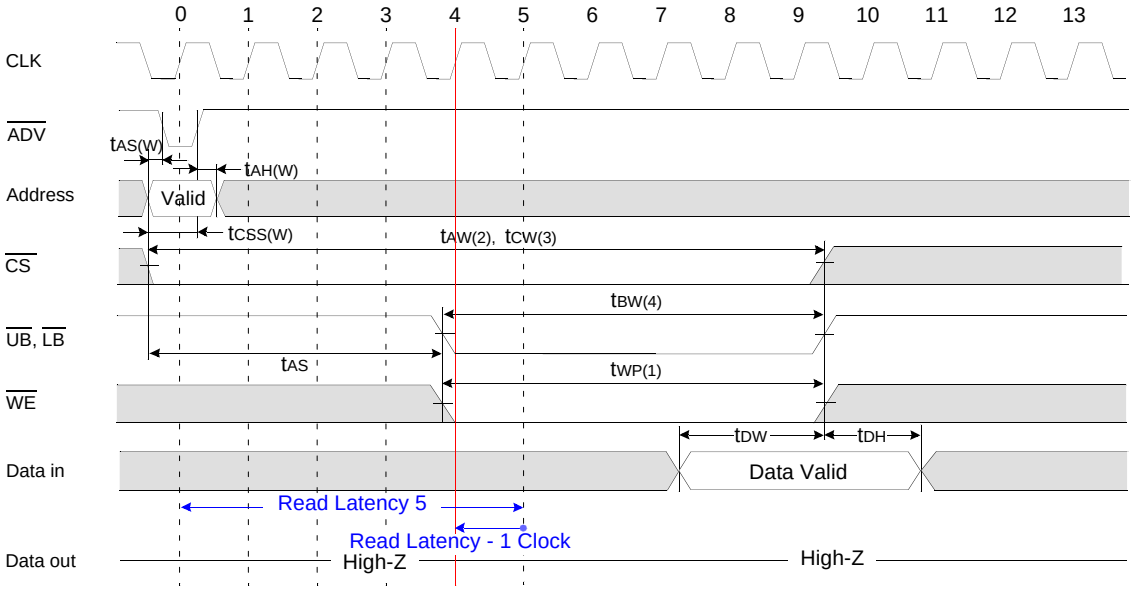
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type) ($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type) ($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{UB}$ & $\overline{LB}$ Controlled)

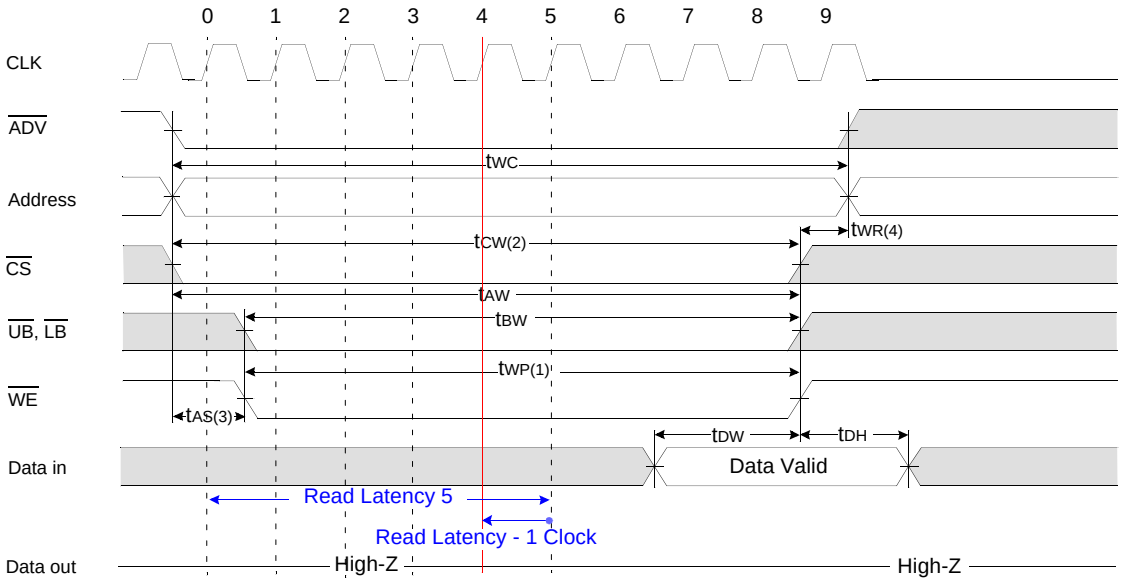


(ADDRESS LATCH TYPE WRITE CYCLE)

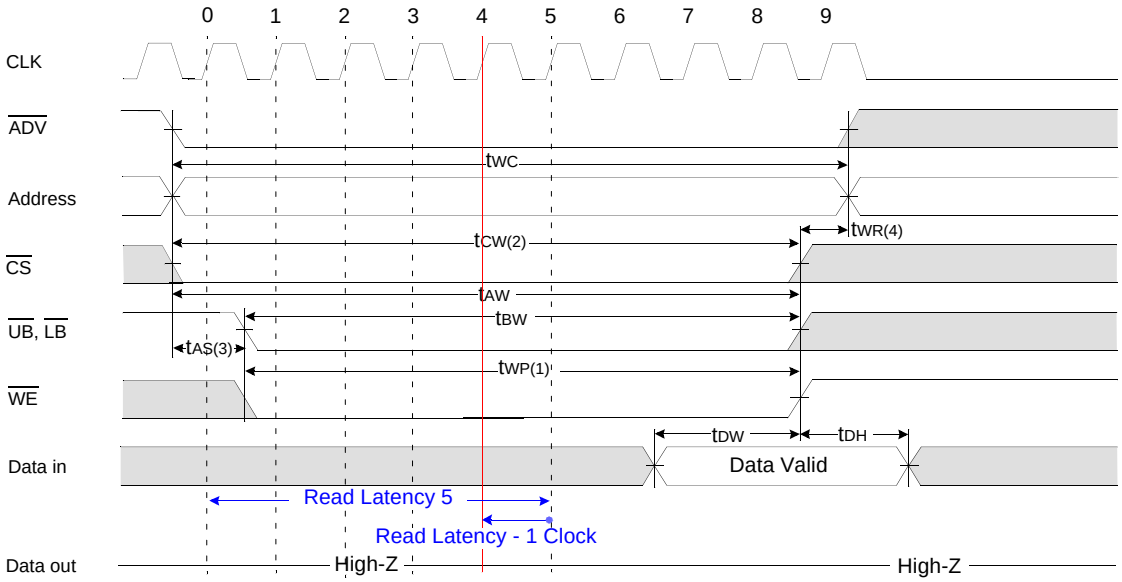
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting UB or LB for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW}.
3. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4. t_{BW} is measured from the $\overline{UB}$ and $\overline{LB}$ going low to the end of write.
5. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

TIMING WAVEFORM OF WRITE CYCLE(Low $\overline{ADV}$ Type) ($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(Low $\overline{ADV}$ Type) ($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{UB}$ & $\overline{LB}$ Controlled)

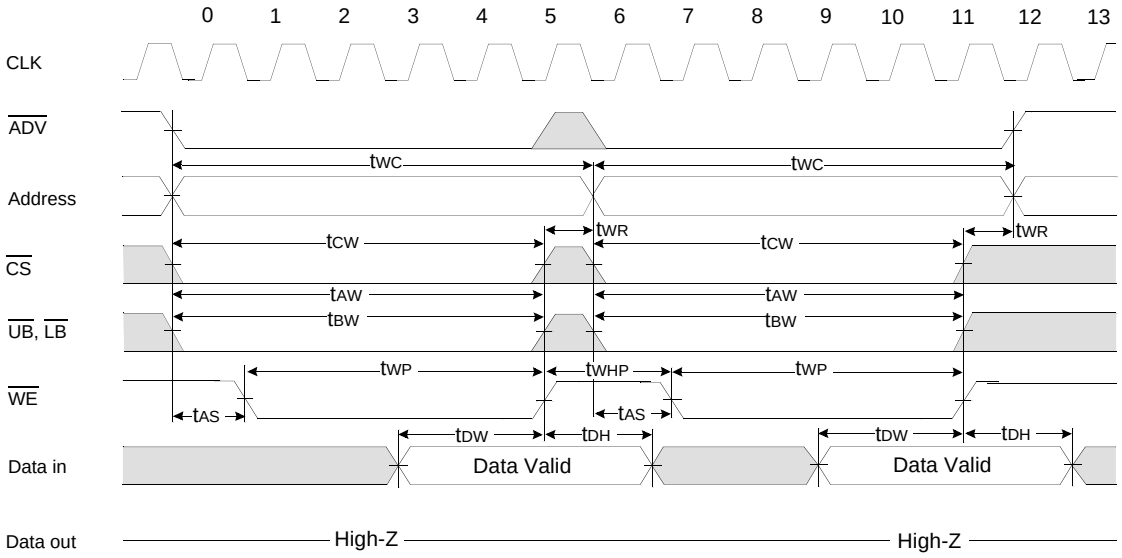


(LOW $\overline{ADV}$ TYPE WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

TIMING WAVEFORM OF CONTINUOUS WRITE CYCLE(Low $\overline{ADV}$ Type) ($\overline{MRS}$=V_{IH}, $\overline{OE}$=V_{IH}, $\overline{WE}$ Controlled)

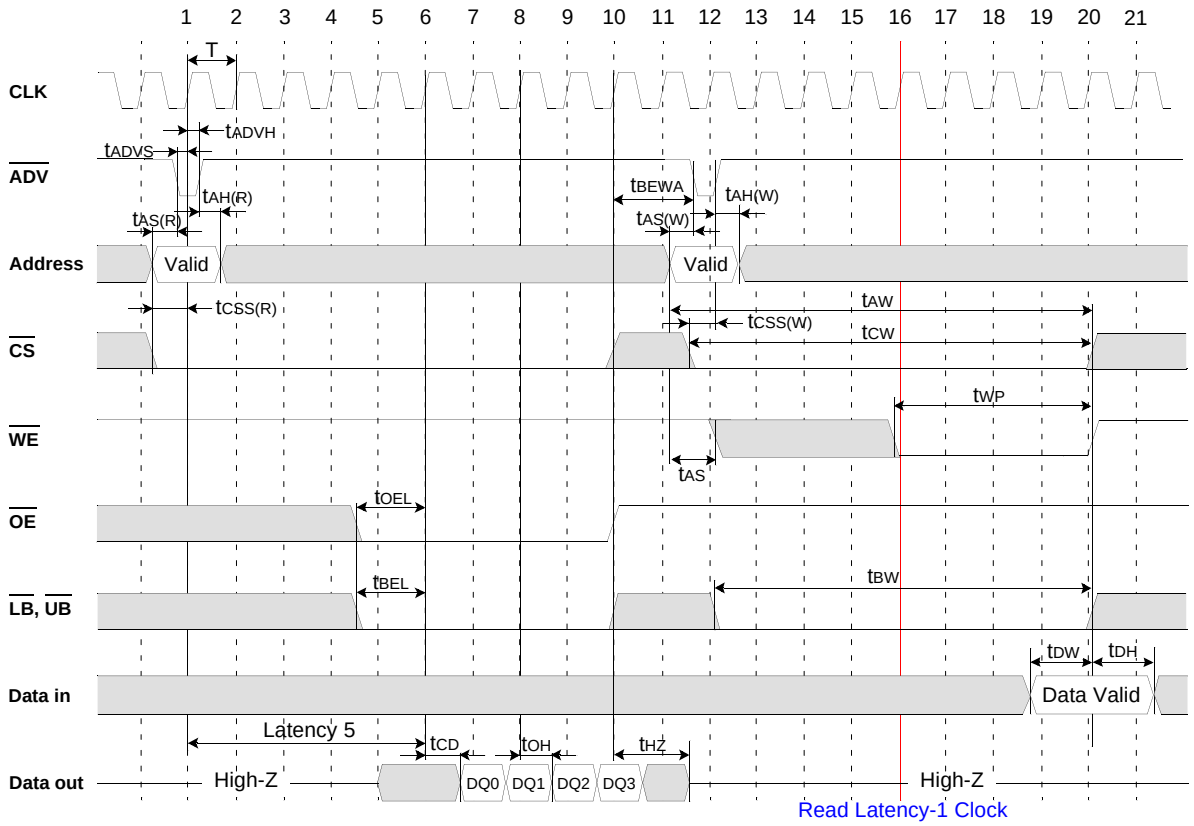


(LOW $\overline{ADV}$ TYPE CONTINUOUS WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. Clock input does not have any affect to the continuous write operation if t_{WHP} is shorter than (Read Latency - 1) clock duration.
6. t_{WP}(min)=85ns for continuous write operation over 50 times.

SYNCH. BURST READ to ASYNCH. WRITE(Address Latch Type) TIMING WAVEFORM

[Latency=5, Burst Length=4] ($\overline{MRS}$=V_{IH})

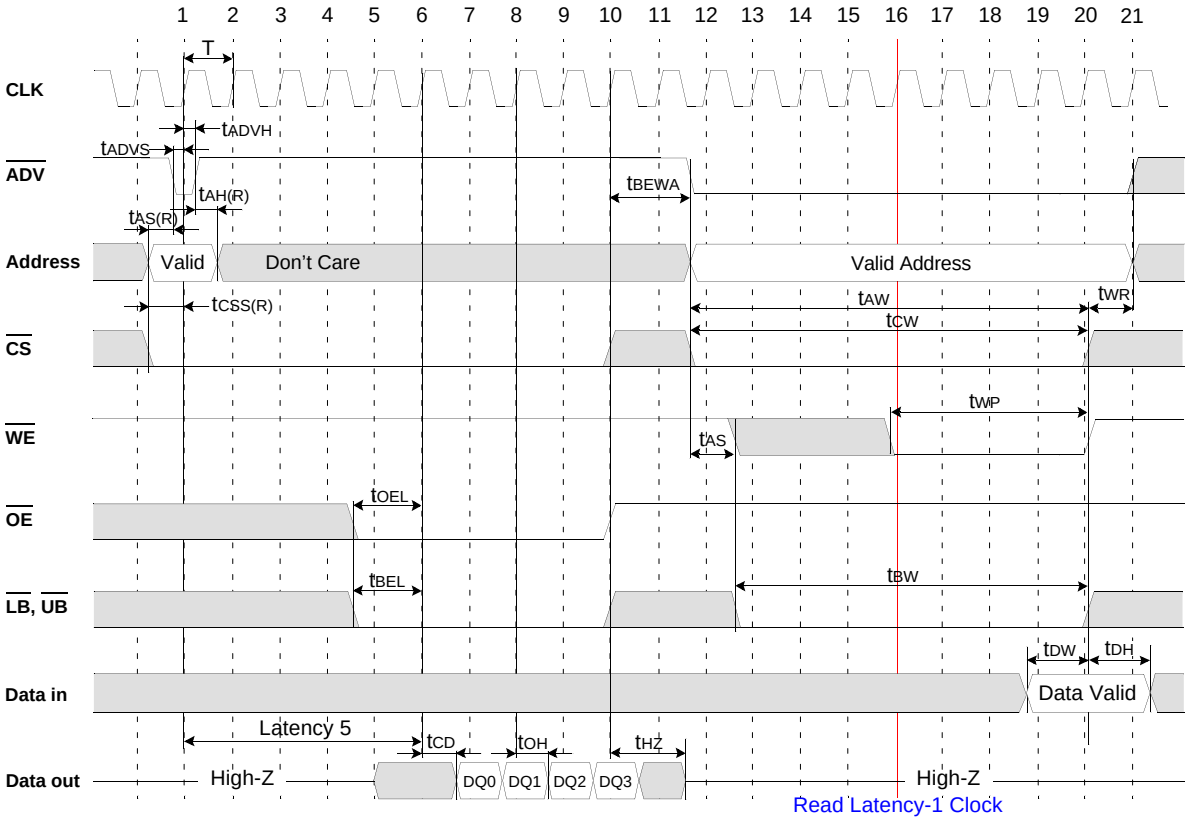


(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

SYNCH. BURST READ to ASYNCH. WRITE(Low $\overline{ADV}$ Type) TIMING WAVEFORM

[Latency=5, Burst Length=4] ($\overline{MRS}$=V_{IH})

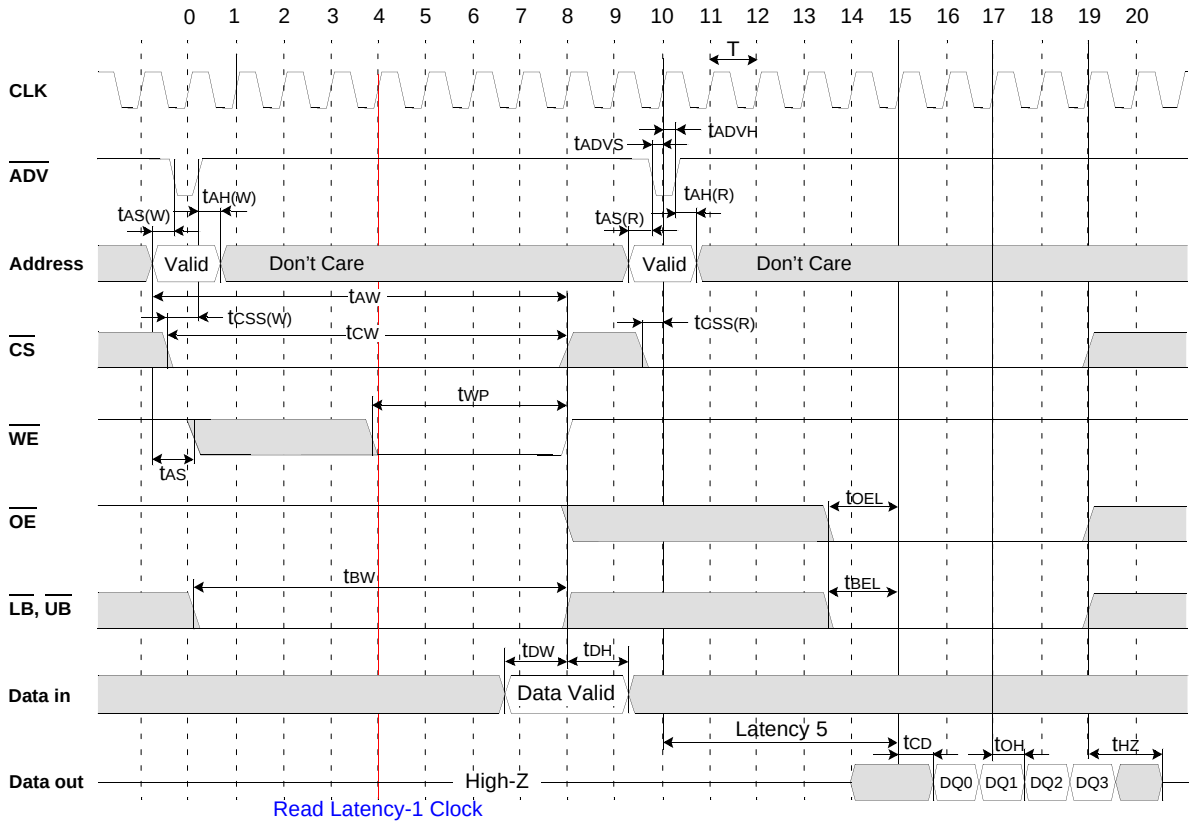


(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

(LOW $\overline{ADV}$ TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

ASYNCH. WRITE(Address Latch Type) to SYNCH. BURST READ TIMING WAVEFORM

[Latency=5, Burst Length=4]($\overline{MRS}$=V_{IH})



(SYNCHRONOUS BURST READ CYCLE)

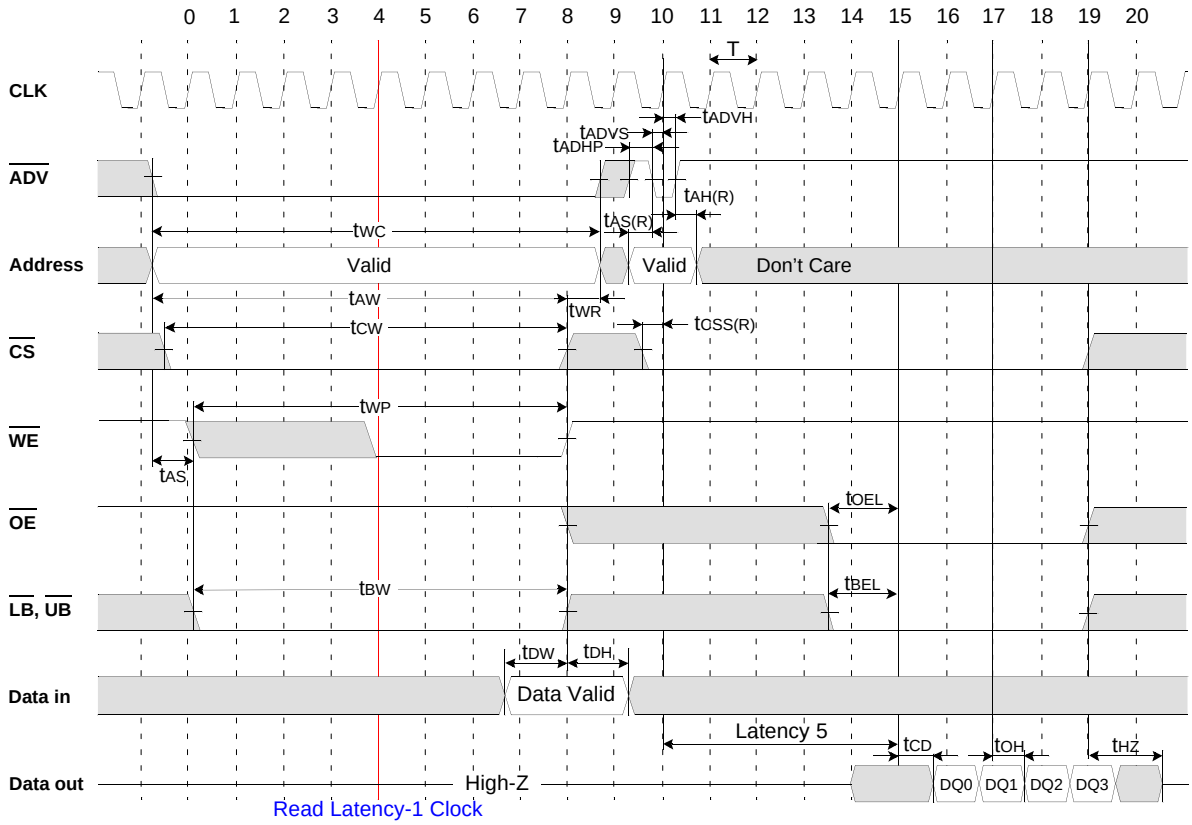
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)

1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

ASYNCH. WRITE(Low $\overline{ADV}$ Type) to SYNCH. BURST READ TIMING WAVEFORM

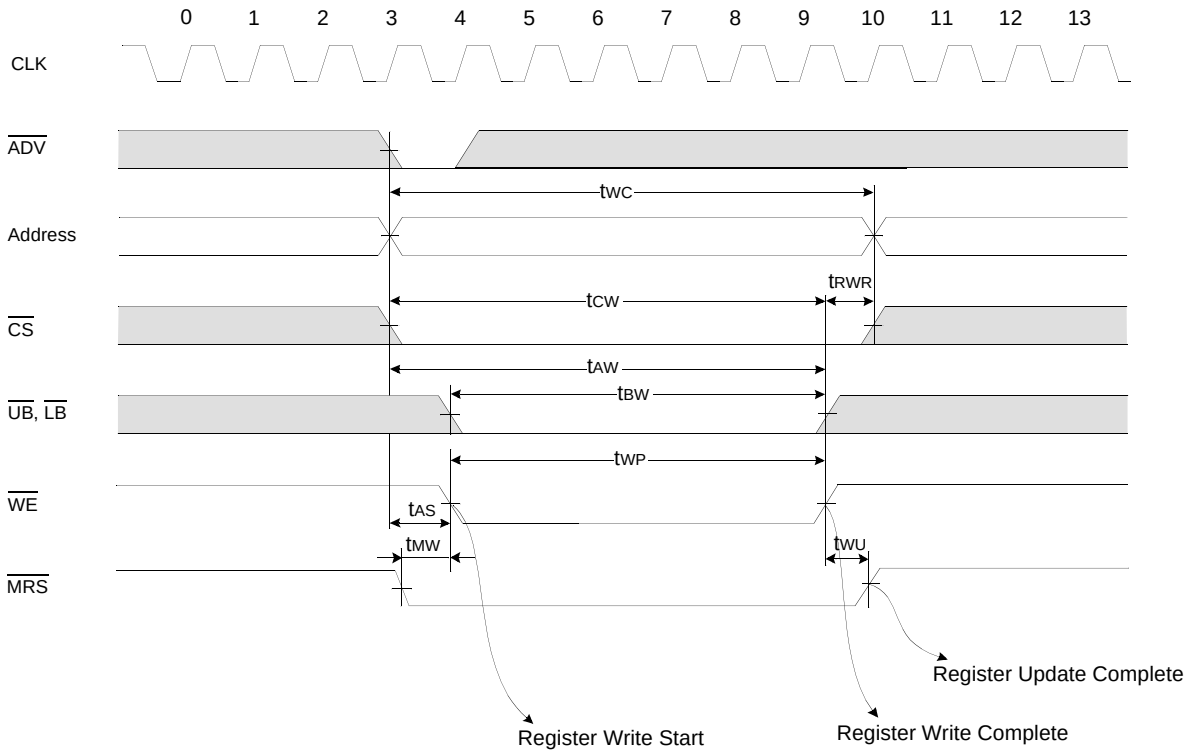
[Latency=5, Burst Length=4] ($\overline{MRS}$=V_{IH})



(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

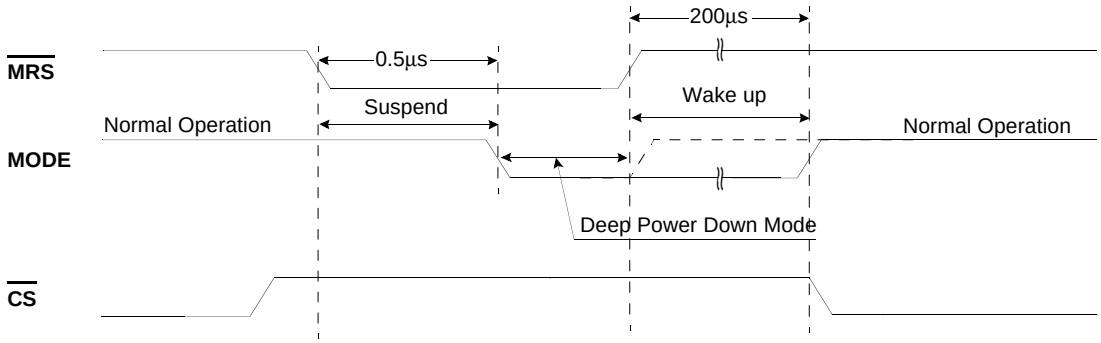
(LOW $\overline{ADV}$ TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

TIMING WAVEFORM OF MRS MODE SETTING ($\overline{OE}$=V_{IH})



(MRS SETTING TIMING)
1. Clock input does not have any affect to the register write operation.

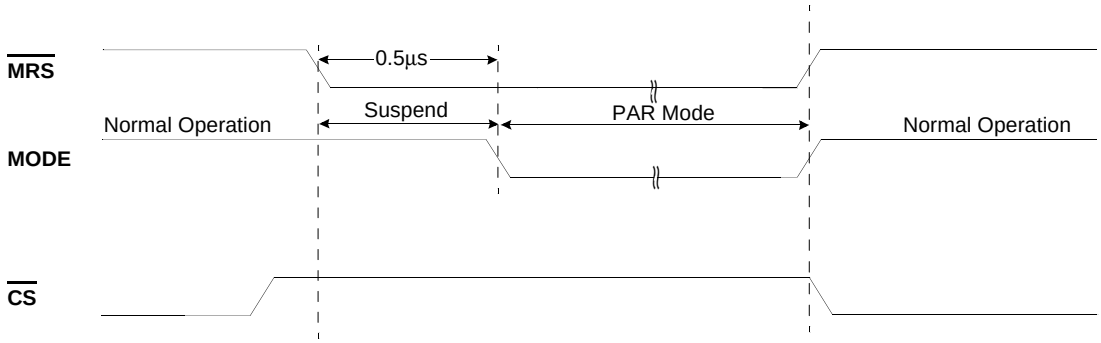
TIMING WAVEFORM OF DEEP POWER DOWN MODE ENTRY AND EXIT



(DEEP POWER DOWN MODE)

1. When $\overline{MRS}$ pin is driven to low under the standby state, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. In this case, the stanby state is achieved by toggling $\overline{CS}$ pin high.
3. To return to normal operation, the device needs Wake Up period.
4. Wake Up sequence is just the same as Power Up sequence.

TIMING WAVEFORM OF PARTIAL ARRAY REFRESH MODE ENTRY AND EXIT



(PARTIAL ARRAY REFRESH MODE)

1. When $\overline{MRS}$ pin is driven to low under the standby state, the device gets into the Partial Array Refresh mode after 0.5µs suspend period.
2. In this case, the stanby state is achieved by toggling $\overline{CS}$ pin high.
3. The device gets back to the normal operation mode after $\overline{MRS}$ pin is driven to high.

256Mb(16M x 16)
Mobile SDRAM E-Die

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 2.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 2.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTES:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C ~ 85°C for Extended, -25°C ~ 70°C for Commercial

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	1.65	1.8	1.95	V	
	V_{DDQ}	1.65	1.8	1.95	V	
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V_{OH}	V_{DDQ} -0.2	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.2	V	I_{OL} = 0.1mA
Input leakage current	I_{LI}	-10	-	10	uA	3

NOTES :
1. VIH (max) = 2.2V AC.The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -1.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
4. Dout is disabled, 0V ≤ VOUT ≤ VDDQ.

CAPACITANCE (V_{DD} = 1.8V, T_A = 23°C, f = 1MHz, V_{REF} =0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	TBD	TBD	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	TBD	TBD	pF	
Address	C_{ADD}	TBD	TBD	pF	
DQ_0 ~ DQ_{15}	C_{OUT}	TBD	TBD	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C ~ 85°C for Extended, -25°C ~ 70°C for Commercial)

Parameter	Symbol	Test Condition		Version		Unit	Note
				-IL	-15		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		40	40	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		0.3		mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		0.3			
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		10		mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		1			
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5		mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1			
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20		mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		5		mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		60	50	mA	1
Refresh Current	I_{CC5}	$t_{ARFC} \geq t_{ARFC}$(min)		65	65	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	**TCSR**	**Max 40°C**	**Max 85°C**	**°C**	
			4 Banks	200	480	uA	
			2 Banks	160	300		
			1 Bank	130	220		

NOTES:

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ).

AC OPERATING TEST CONDITIONS (V_{DD} = 1.8V ± 0.15V, T_A = -25°C ~ 85°C for Extended, -25°C ~ 70°C for Commer-

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.9 x V_{DDQ} / 0.2	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	0.5 x V_{DDQ}	V
Output load condition	See Figure 2	

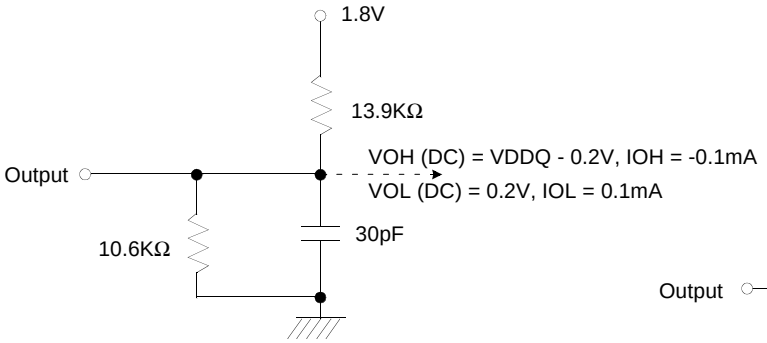


Figure 1. DC Output Load Circuit

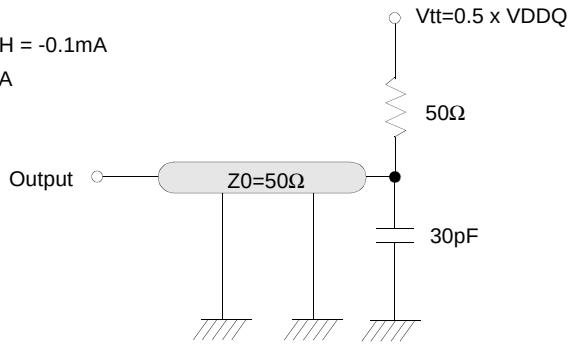


Figure 2. AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-IL	-15		
Row active to row active delay		t_{RRD}(min)	19	30	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	28.5	26	ns	1
Row precharge time		t_{RP}(min)	28.5	26	ns	1
Row active time		t_{RAS}(min)	57	65	ns	1
		t_{RAS}(max)	100		us	
Row cycle time		t_{RC}(min)	85.5	91	ns	1
Last data in to row precharge		t_{RDL}(min)	2		CLK	2
Last data in to Active delay		t_{DAL}(min)	tRDL + tRP		-	3
Last data in to new col. address delay		t_{CDL}(min)	1		CLK	2
Last data in to burst stop		t_{BDL}(min)	1		CLK	2
Auto refresh cycle time		t_{ARFC}(min)	105		ns	
Exit self refresh to active command		t_{SRFX}(min)	120		ns	
Col. address to col. address delay		t_{CCD}(min)	1		CLK	4
Number of valid output data	CAS latency=3		2		ea	5
Number of valid output data	CAS latency=2		1			
Number of valid output data	CAS latency=1		0			

NOTES:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum 3CLK of tDAL(= tRDL + tRP) is required because it need minimum 2CLK for tRDL and minimum 1CLK for tRP.
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	-1L		-15		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	9.5	1000	13	1000	ns	1
CLK cycle time	CAS latency=2	tCC			13			
CLK cycle time	CAS latency=1	tCC			30			
CLK to valid output delay	CAS latency=3	tSAC		7		7	ns	1,2
CLK to valid output delay	CAS latency=2	tSAC				9		
CLK to valid output delay	CAS latency=1	tSAC				24		
Output data hold time	CAS latency=3	tOH	2.5		2.5		ns	2
Output data hold time	CAS latency=2	tOH	2.5		2.5			
Output data hold time	CAS latency=1	tOH	2.5		2.5			
CLK high pulse width		tCH	3.0		3.5		ns	3
CLK low pulse width		tCL	3.0		3.5		ns	3
Input setup time		tSS	2.0		2.5		ns	3
Input hold time		tSH	1.5		2.0		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7		7	ns	
	CAS latency=2					9		
	CAS latency=1					24		

NOTES :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11,A12 A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

NOTES :

1. OP Code : Operand Code
   A0 ~ A12 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
   Partial self refresh can be issued only after setting partial self refresh mode of EMRS.
4. BA0 ~ BA1 : Bank select addresses.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1[*1]	A12 ~ A10/AP	A9[*2]	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

Full Page Length x16 : 64Mb(256), 128Mb(512),256Mb(512),512Mb(1024)

Register Programmed with Extended MRS

Address	BA1	BA0	A12 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU				DS		RFU		PASR		

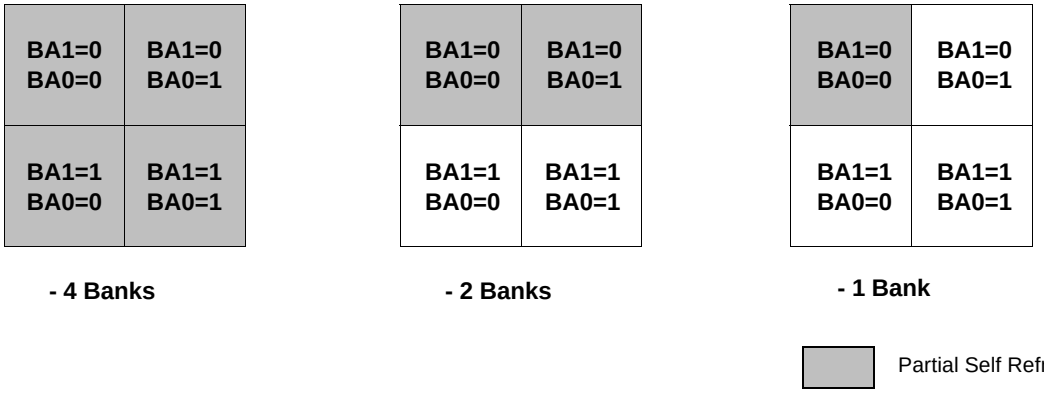
EMRS for PASR(Partial Array Self Ref.) & DS(Driver Strength)

Mode Select			Driver Strength			PASR			
BA1	BA0	Mode	A6	A5	Driver Strength	A2	A1	A0	# of Banks
0	0	Normal MRS	0	0	Full	0	0	0	4 Banks
0	1	Reserved	0	1	1/2	0	0	1	2 Banks
1	0	EMRS for Mobile SDRAM	1	0	1/4	0	1	0	1 Bank
1	1	Reserved	1	1	1/8	0	1	1	Reserved
Reserved Address						1	0	0	Reserved
A12~A10/AP	A9	A8	A7	A4	A3	1	0	1	Reserved
0	0	0	0	0	0	1	1	0	Reserved
						1	1	1	Reserved

NOTES:
1.RFU(Reserved for future use) should stay "0" during MRS cycle.
2.If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.

Partial Array Self Refresh

1. In order to save power consumption, Mobile SDRAM has PASR option.
2. Mobile SDRAM supports 3 kinds of PASR in self refresh mode : 4 Banks, 2 Banks and 1 Bank.



Internal Temperature Compensated Self Refresh (TCSR)

Note :

1. In order to save power consumption, Mobile DDR SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range ; Max. 40 °C, Max. 85 °C.
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (Icc 6)			Unit
	4 Banks	2 Banks	1 Bank	
Max. 40 °C	200	160	130	uA
Max. 85 °C	480	300	220	

B. POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used.
The default state without EMRS command issued is half driver strength, all 4 banks refreshed.
The device is now ready for the operation selected by EMRS.
For operating with DS or PASR , set DS or PASR mode in EMRS setting stage.
In order to adjust another mode in the state of DS or PASR mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

C. BURST SEQUENCE

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

D. DEVICE OPERATIONS

ADDRESSES of 256Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 16

This SDRAM is organized as four independent banks of 4,194,304 words x 16 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 32

This SDRAM is organized as four independent banks of 2,097,152 words x 32 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 16

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA0 ~ BA1 during read or write command.

: In case x 32

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A0 ~ A11). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA0 ~ BA1 during read or write command.

ADDRESSES of 512Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 16

This SDRAM is organized as four independent banks of 8,388,608 words x 16 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 32

This SDRAM is organized as four independent banks of 4,194,304 words x 32 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 16

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA0 ~ BA1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA0 ~ BA1 during read or write command.

: In case x 32

The 22 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA0 ~ BA1 during read or write command.

D. DEVICE OPERATIONS (continued)

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock in order to function well Q perform and ICC specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time are the same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + tSS" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interruptions of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0 ~ An and BA0 ~ BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on the fields of functions. The burst length field uses A0 ~ A2, burst type uses A3, CAS latency (read latency from column address) use A4 ~ A6, vendor specific options or test mode use A7 ~ A8, A10/AP ~ An and BA0 ~ BA1. The write burst length is programmed using A9. A7 ~ A8, A10/AP ~ An and BA0 ~ BA1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

D. DEVICE OPERATIONS (continued)

EXTENDED MODE REGISTER SET (EMRS)

The extended mode register stores the data for selecting driver strength and partial self refresh. EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used. The default state without EMRS command issued is half driver strength and all 4 banks refreshed. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA1 ,low on BA0(The SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 - A2 are used for partial self refresh , A5 - A6 are used for Driver strength, "Low" on BA1 and "High" on BA0 are used for EMRS. All the other address pins except A0,A1,A2, BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.

BANK ACTIVATE.

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer.

The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high, requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

D. DEVICE OPERATIONS (continued)

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on CS, CAS and WE with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

ALL BANKS PRECHARGE

All banks can be precharged at the same time by using Precharge all command. Asserting low on CS, RAS, and WE with high on A10/AP after all banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge to all the banks, all banks are in idle state.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on CS, RAS, WE and A10/AP with valid BA0 ~ BA1 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A10/AP. If burst read or burst write by asserting high on A10/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

AUTO REFRESH

The storage cells of 64Mb, 128Mb, 256Mb and 512Mb SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on CS, RAS and CAS with high on CKE and WE. The auto refresh command can only be asserted with all banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RC}(min). The minimum number of clock cycles required can be calculated by driving t_{RC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The 64Mb and 128Mb SDRAM's auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms. The 256Mb and 512Mb SDRAM's auto refresh cycle can be performed once in 7.8us or a burst of 8192 auto refresh cycles once in 64ms.

D. DEVICE OPERATIONS(continued)

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

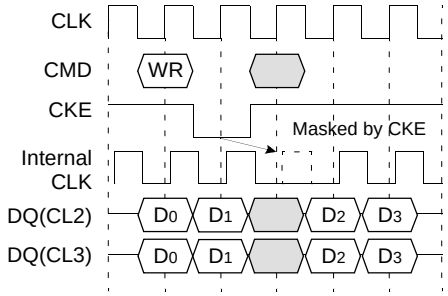
The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of tSRFX before the SDRAM reaches idle state to begin normal operation. In case that the system uses burst auto refresh during normal operation, it is recommended to use burst 8192 auto refresh cycles for 256Mb and 512Mb, and burst 4096 auto refresh cycles for 128Mb and 64Mb immediately before entering self refresh mode and after exiting in self refresh mode. On the other hand, if the system uses the distributed auto refresh, the system only has to keep the refresh duty cycle.

E. BASIC FEATURE AND FUNCTION DESCRIPTIONS

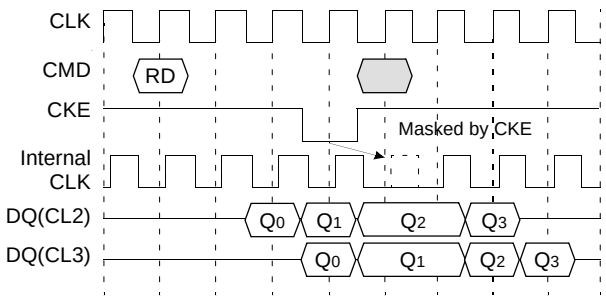
1. CLOCK Suspend

1) Clock Suspended During Write



Not Written

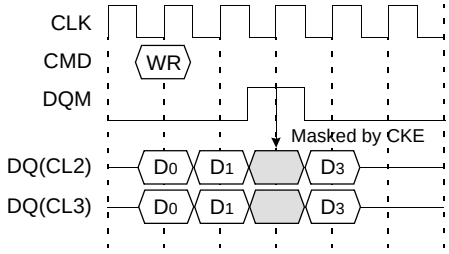
2) Clock Suspended During Read (BL=4)



Suspended Dout

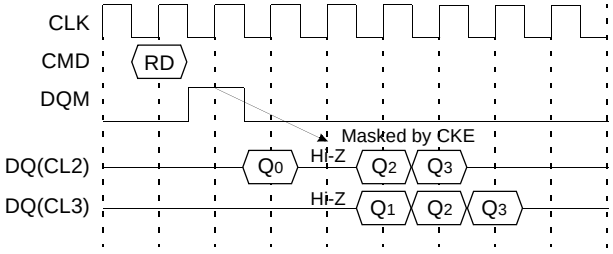
2. DQM Operation

1) Write Mask (BL=4)



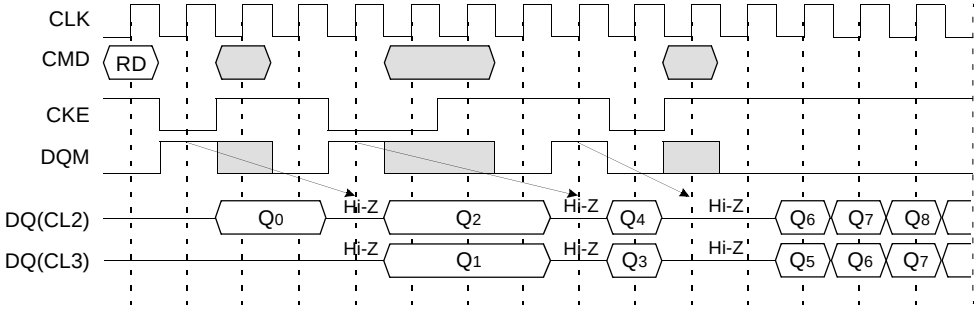
DQM to Data-in Mask = 0

2) Read Mask (BL=4)



DQM to Data-out Mask = 2

3) DQM with Clock Suspended (Full Page Read) *2

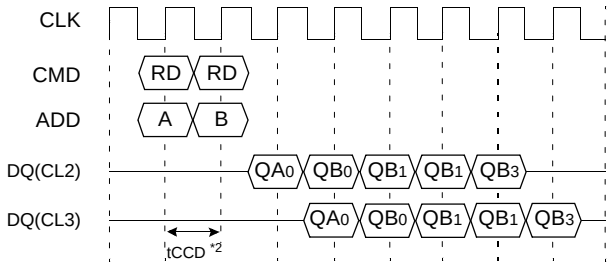


***NOTE :**

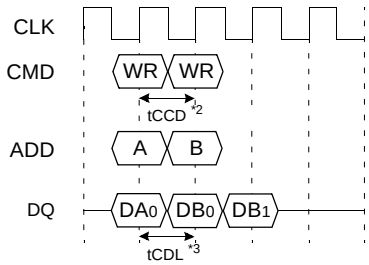
1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)

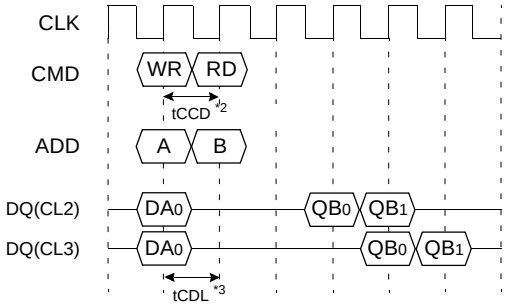
1) Read interrupted by Read (BL=4) *1



2) Write interrupted by Write (BL=2)



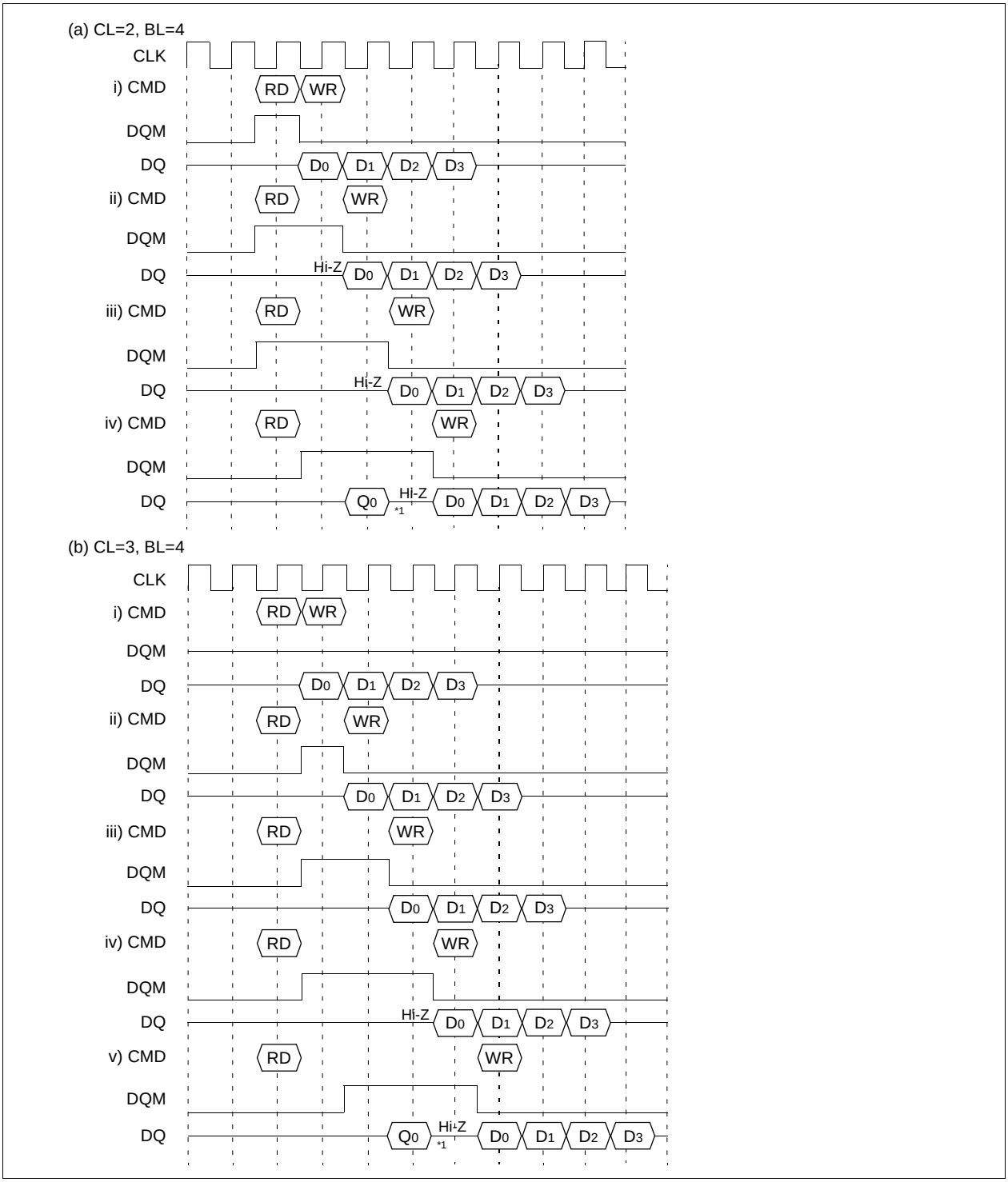
3) Write interrupted by Read (BL=2)



***NOTE:**

1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
   By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.
2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

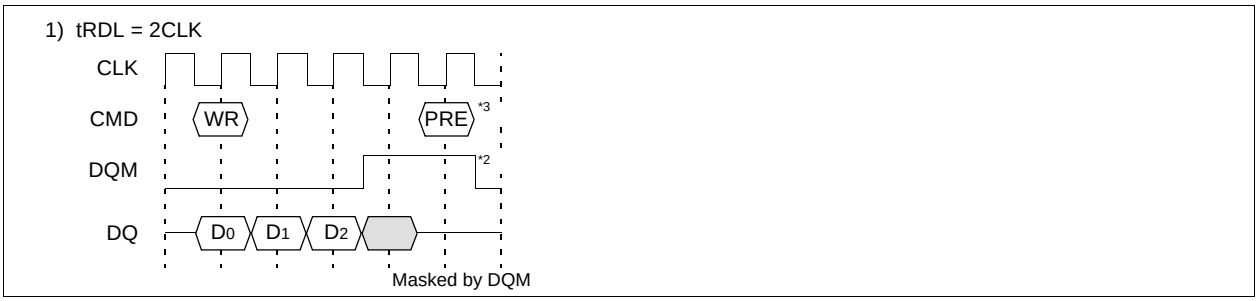
4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM



***NOTE:**

1. To prevent bus contention, there should be at least one gap between data in and data out.

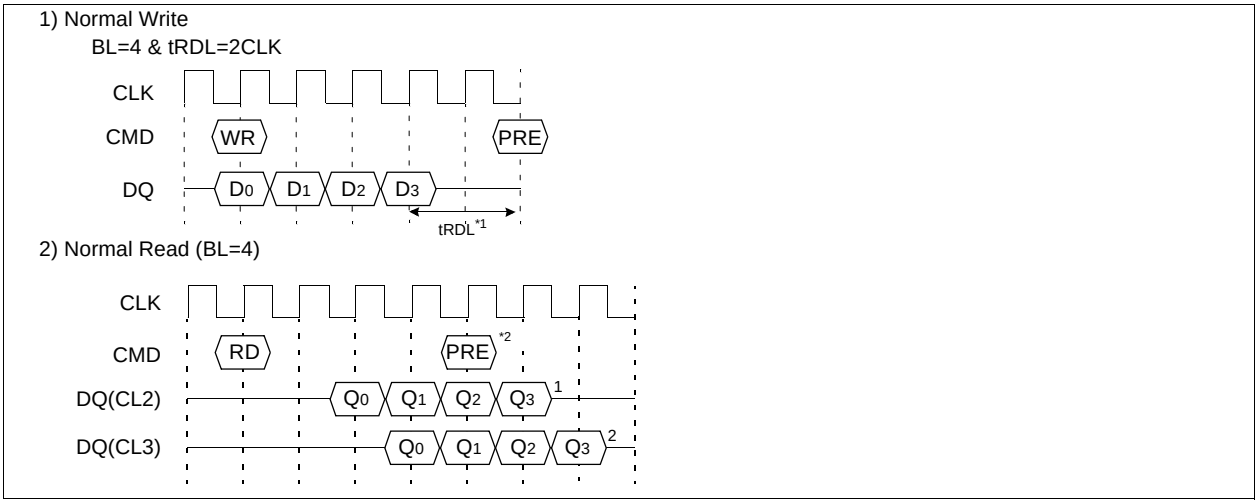
5. Write Interrupted by Precharge & DQM



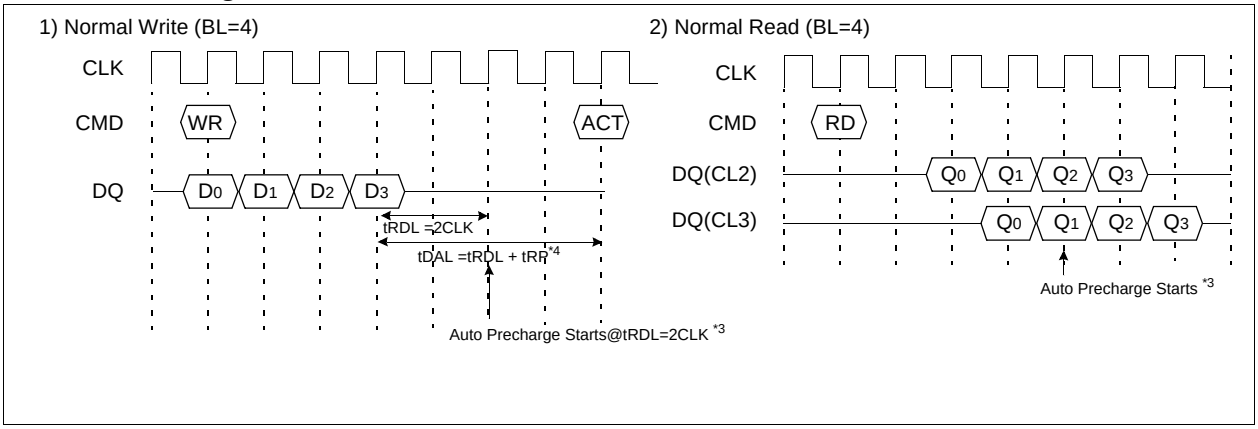
***NOTE:**

1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge



7. Auto Precharge



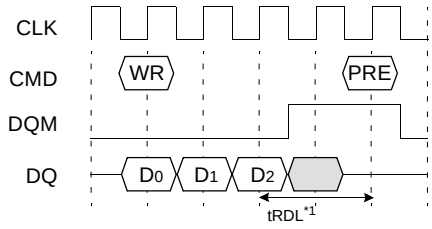
***NOTE:**

1. SAMSUNG can support tRDL=1CLK and tRDL=2CLK for all memory devices. SAMSUNG recommends tRDL=2 CLK.
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
   The new read/write command of other activated bank can be issued from this point.
   At burst read/write with auto precharge, CAS interrupt of the same bank is illegal
4. tDAL defined Last data in to Active delay. SAMSUNG can support tDAL=tRDL+ tRP .

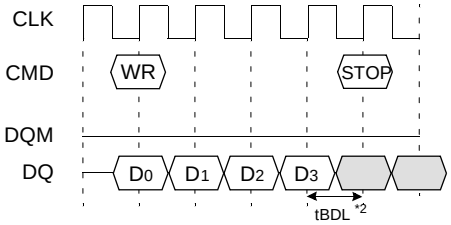
8. Burst Stop & Interrupted by Precharge

1) Normal Write

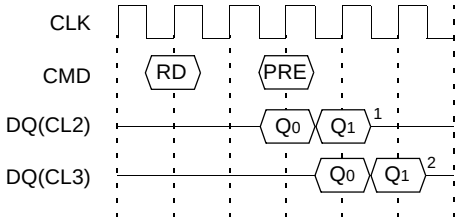
BL=4 & tRDL=2CLK



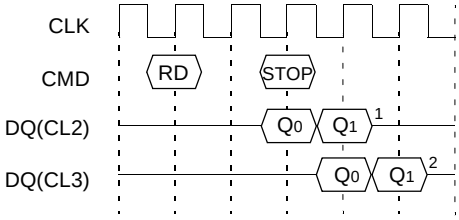
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

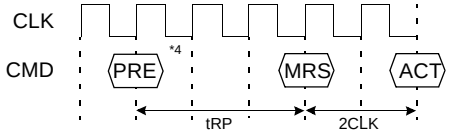


4) Read Burst Stop (BL=4)



9. MRS

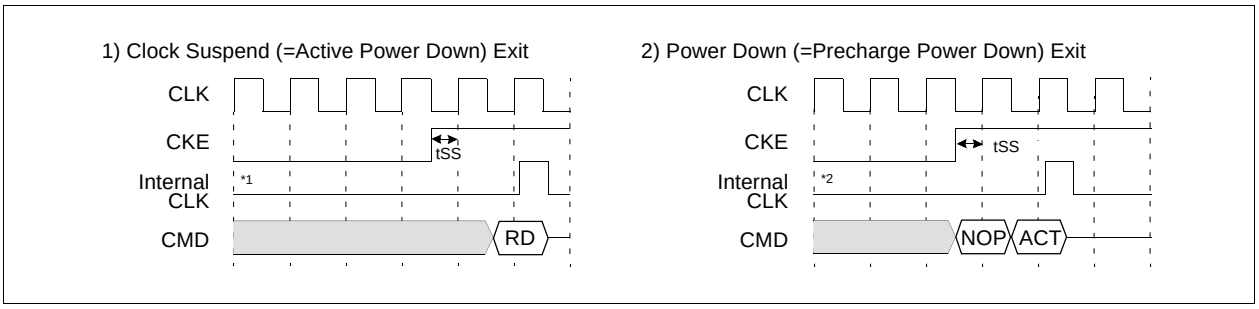
1) Mode Register Set



***NOTE:**

1. SAMSUNG can support tRDL=2 CLK.
2. tBDL : 1 CLK ; Last data in to burst stop delay.
   Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectively.
4. PRE : All banks precharge is necessary.
   MRS can be issued only at all banks precharge state.

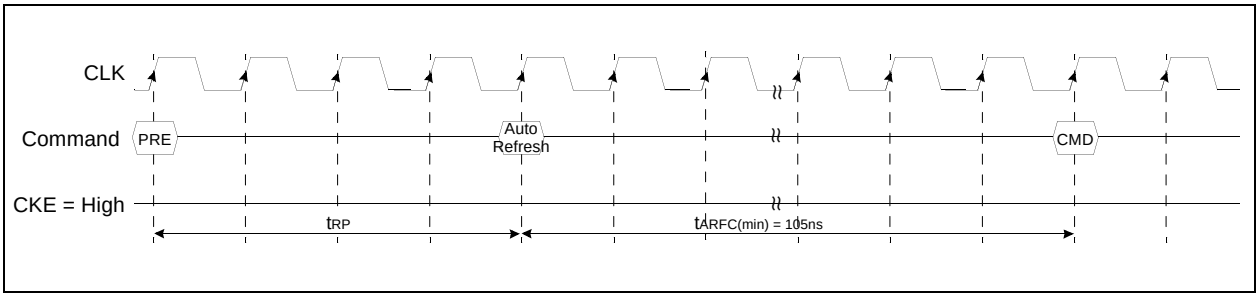
10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh

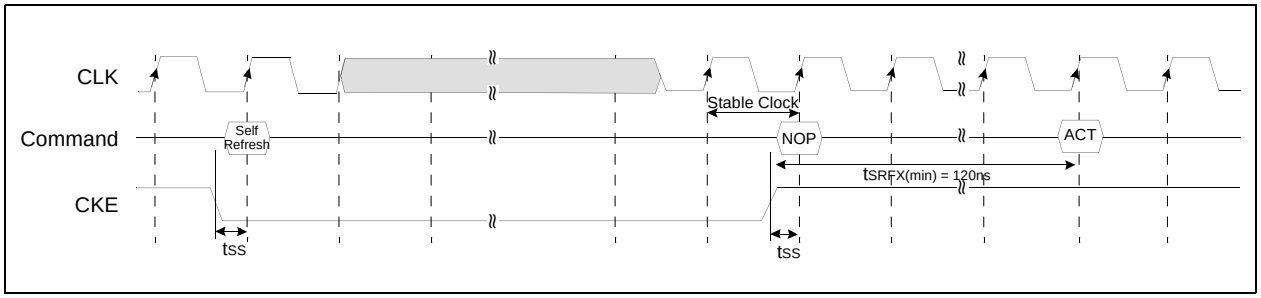
Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CLK). All banks must be precharged and idle for t_{RP}(min) before the auto refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{ARFC}(min).



Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CLK) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. To exit the Self Refresh mode, supply stable clock input before returning CKE high, assert deselect or NOP command and then assert CKE high. In case that the system uses burst auto refresh during normal opreation, it is recommended to use burst 4096 auto refresh cycle immediately before entering self refresh mode and after exiting in self refresh mode. On the other hand, if the system uses the distributed auto refresh, the system only has to keep the refresh duty cycle.



12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting.
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". Wrap around mode(infinite burst length) should be stopped by burst stop. $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt.
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1. At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 2 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A_{10}/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Begin Read ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A_{10}/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A_{10}/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A_{10}/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA_{10}	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	

FUNCTION TRUTH TABLE (TABLE 1)

Current	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
Precharging	H	X	X	X	X	X	NOP --> Idle after t_{RP}	
	L	H	H	H	X	X	NOP --> Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	NOP --> Idle after t_{RP}	4
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***NOTE:**

1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Note
Self Refresh	H	X	X	X	X	X	X	Exit Self Refresh --> Idle after t_{SRFX}(ABI)	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{SRFX} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{SRFX} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

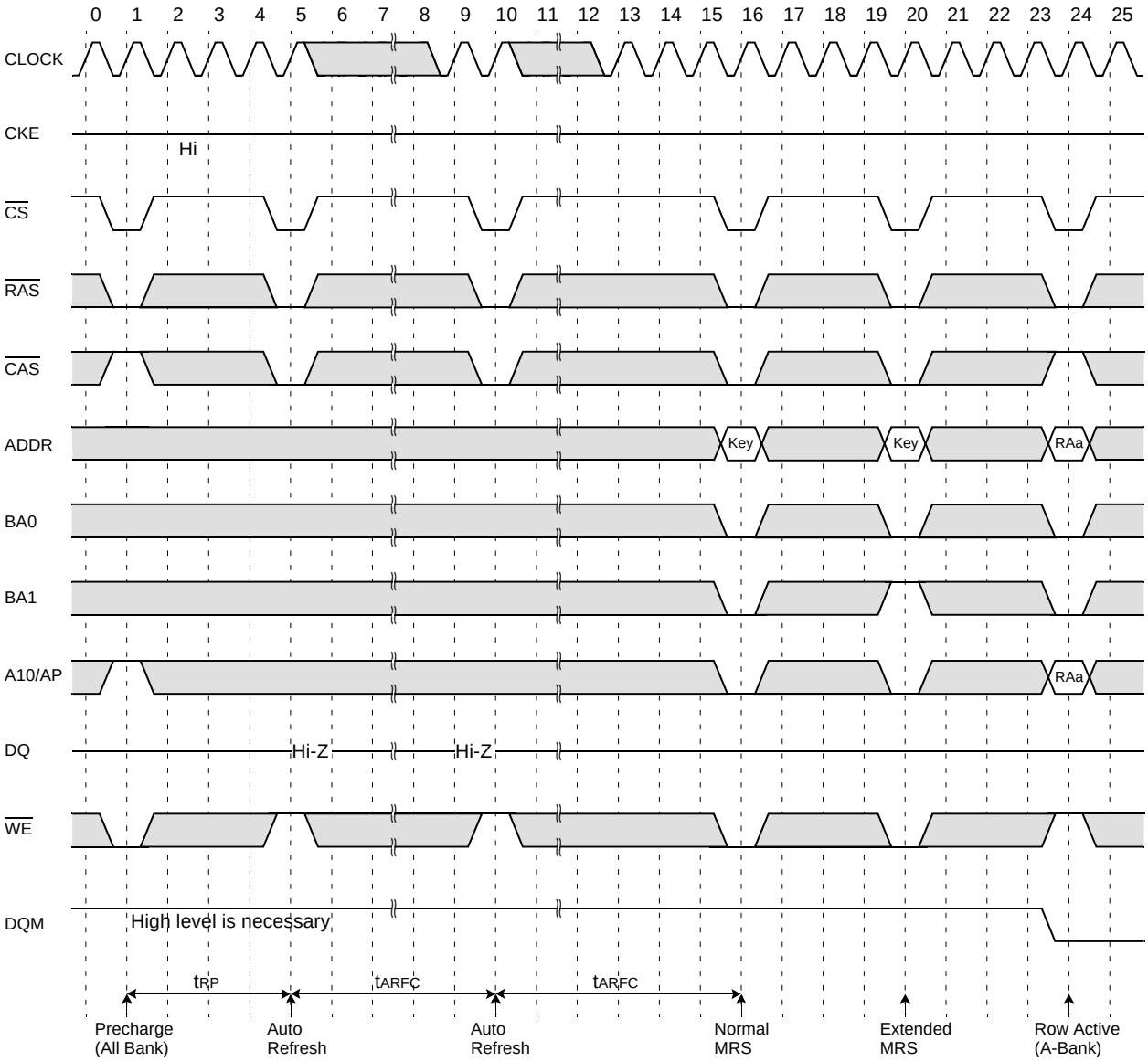
Abbreviations : ABI = All Banks Idle, RA = Row Address

***NOTE:**

6. CKE low to high transition is asynchronous.
7. CKE low to high transition is asynchronous if restarts internal clock.
   A minimum setup time 1CLK + t_{SS} must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the all banks idle state.
9. Must be a legal command.

Power Up Sequence
Single Bit Read - Write - Read Cycle(Same Page) @CAS Latency=3, Burst Length=1
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read Cycle at Different Bank @Burst Length=4
Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK
Read & Write Cycle at Different Bank @Burst Length=4
Read & Write Cycle With Auto Precharge I @Burst Length=4
Read & Write Cycle With Auto Precharge II @Burst Length=4
Clock Suspension & DQM Operation Cycle @CAS Letency=2, Burst Length=4
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK
Burst Read Single bit Write Cycle @Burst Length =2
Active/precharge Power Dower Down Mode @CAS Latency=2 Burst Length=4
Self Refresh Entry & Exit Cycle & Exit Cycle
Mode Register Set Cycle and Auto Refresh Cycle
Extended Mode Register Set Cycle

Power Up Sequence for Mobile SDRAM

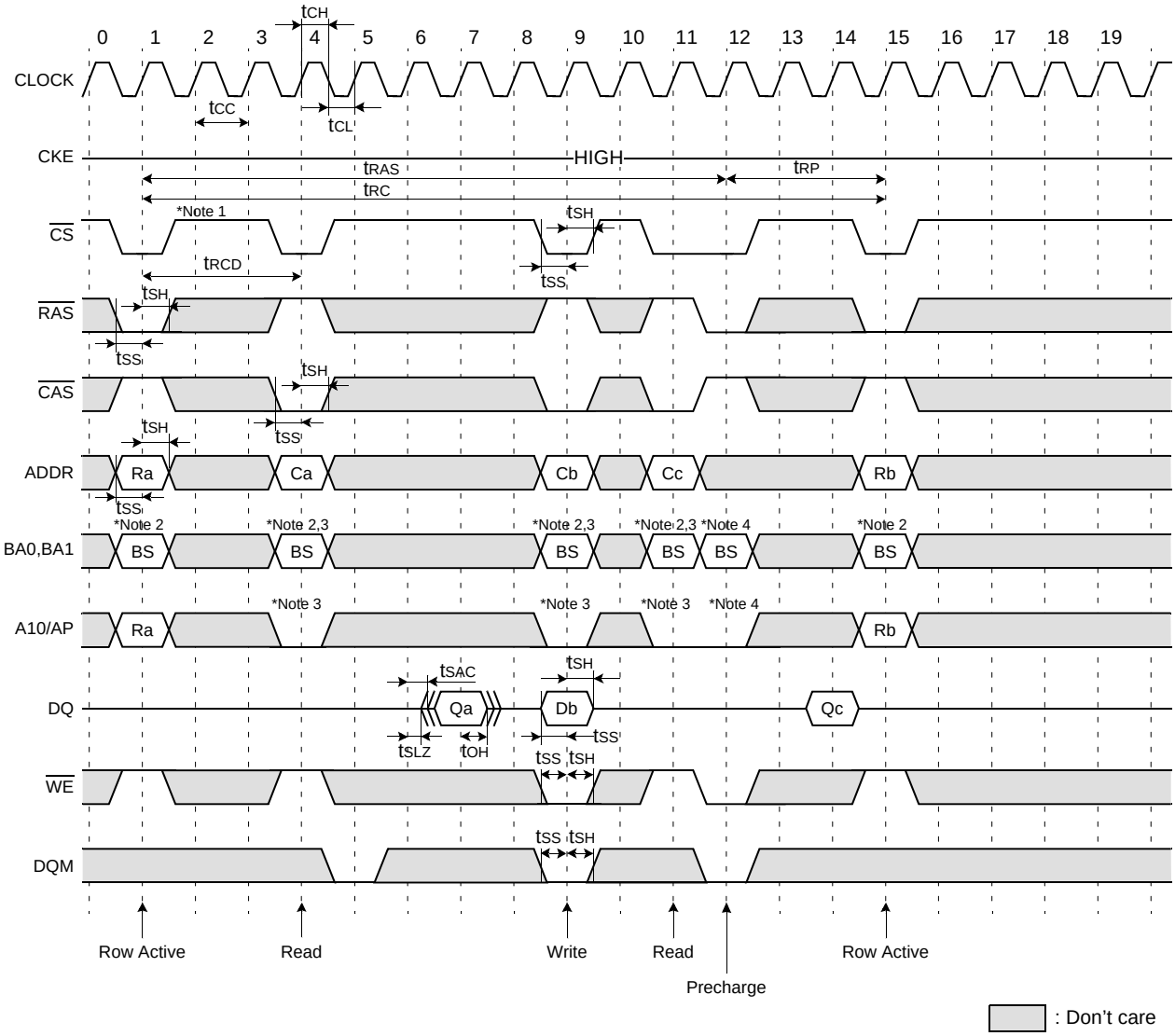


***NOTE:**

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply V_{DD} before or at the same time as V_{DDQ}.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used.
The default state without EMRS command issued is half driver strength, all 4 banks refreshed.
The device is now ready for the operation selected by EMRS.
For operating with DS or PASR, set DS or PASR mode in EMRS setting stage.
In order to adjust another mode in the state of DS or PASR mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

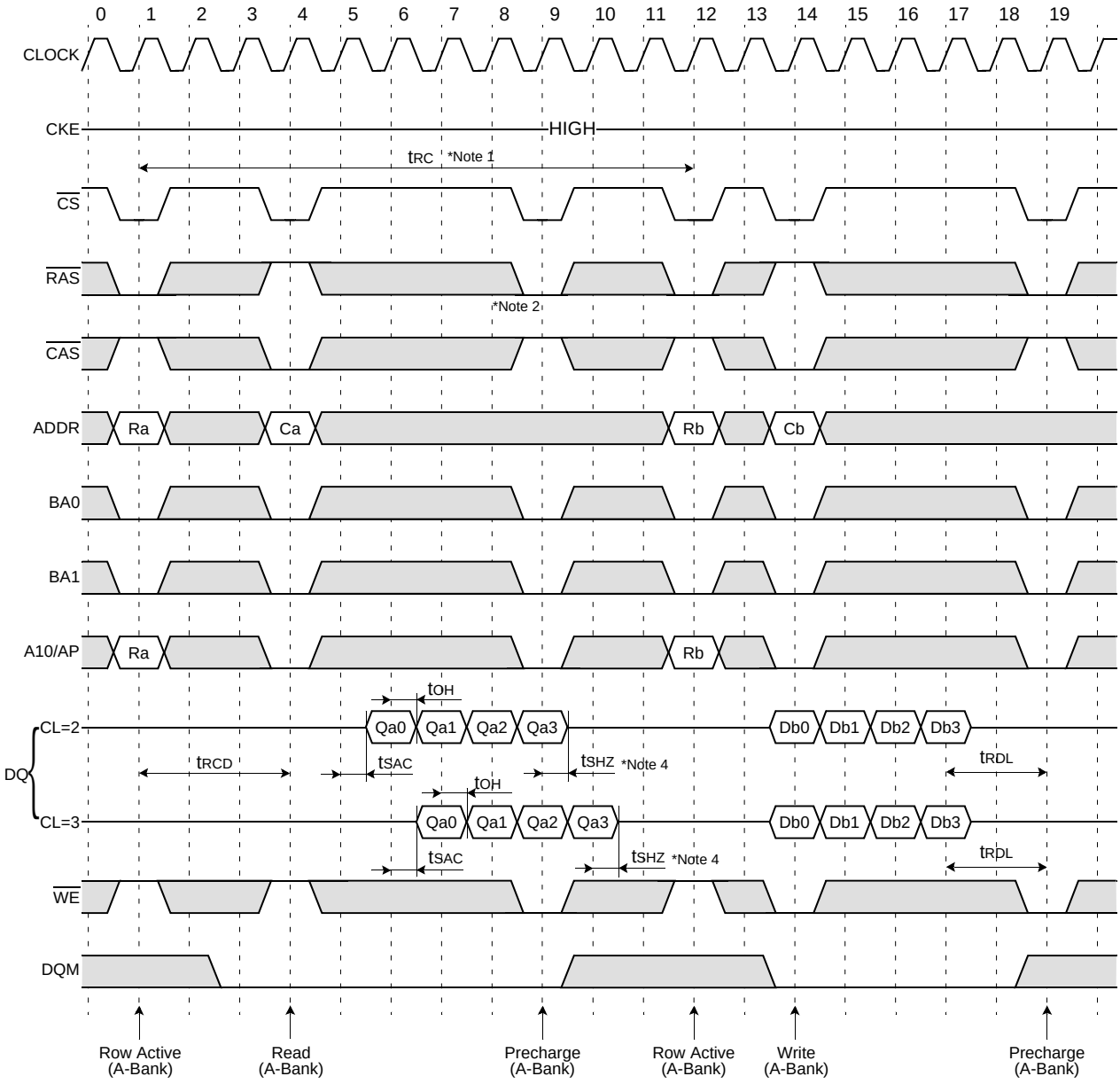
Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



***NOTE:**

1. All input except CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0,BA1.

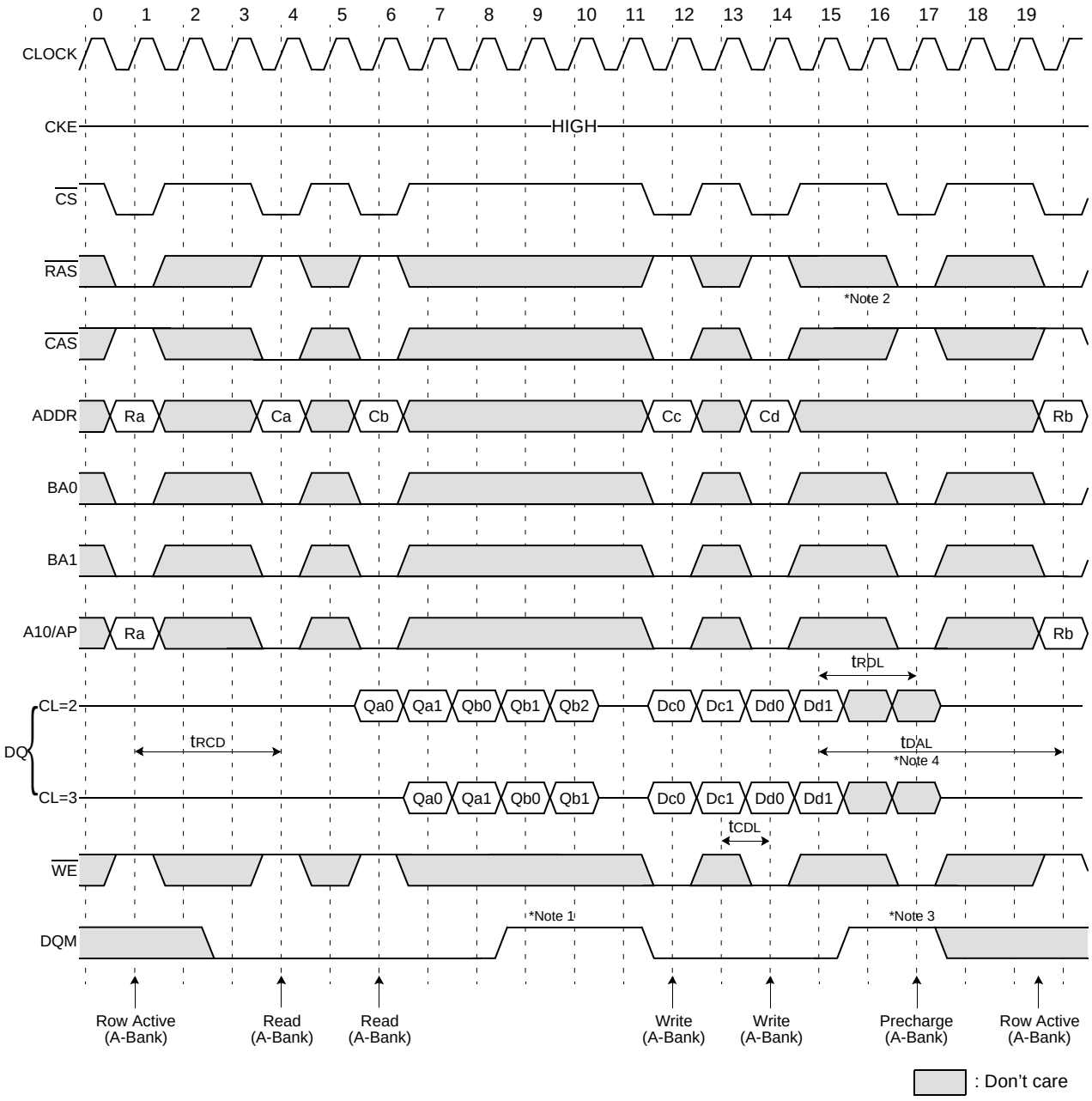
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



***NOTE:**

1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

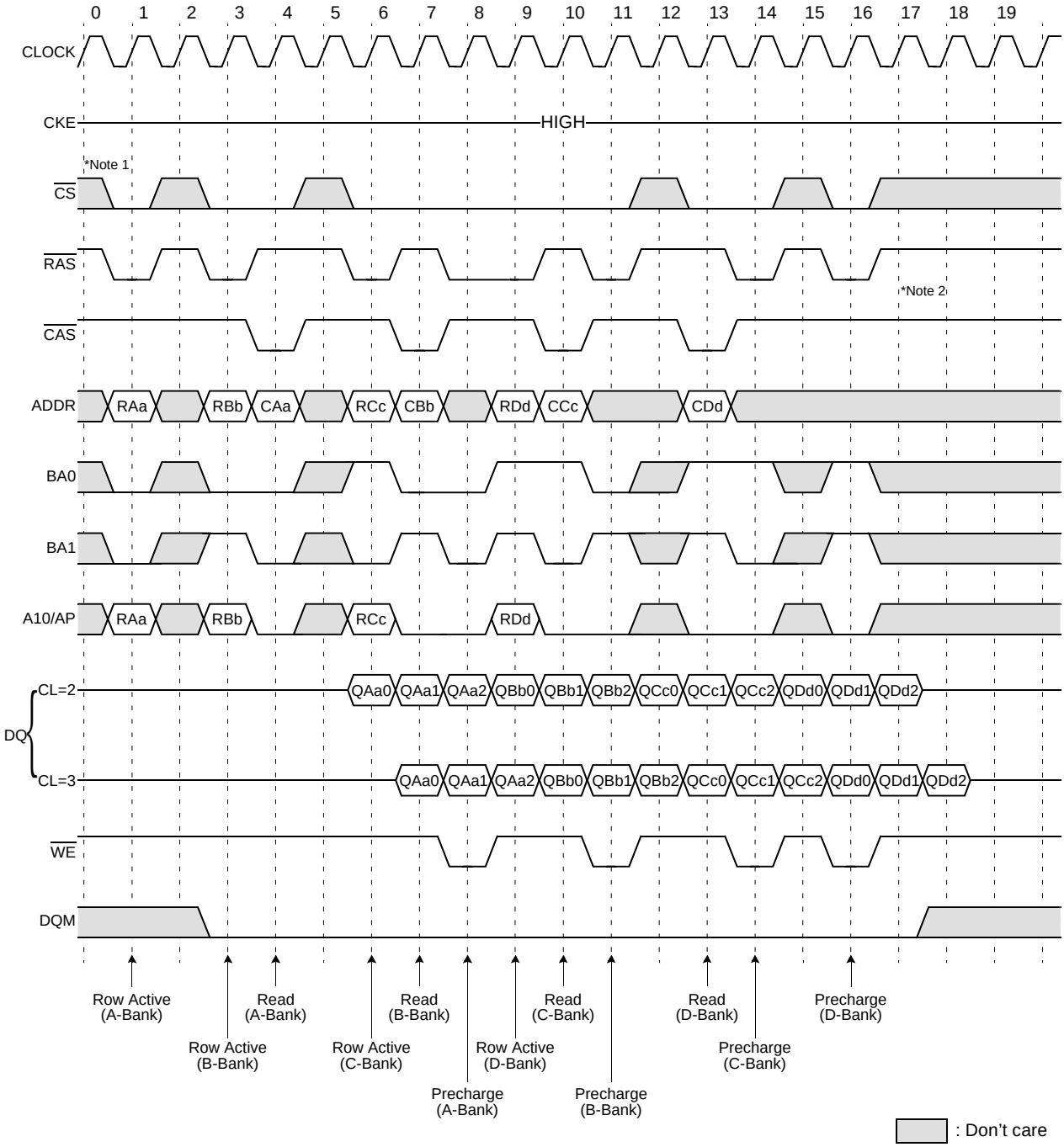
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



***NOTE:**

1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. t_{DAL} ,last data in to active delay, is 2CLK + t_{RP}.

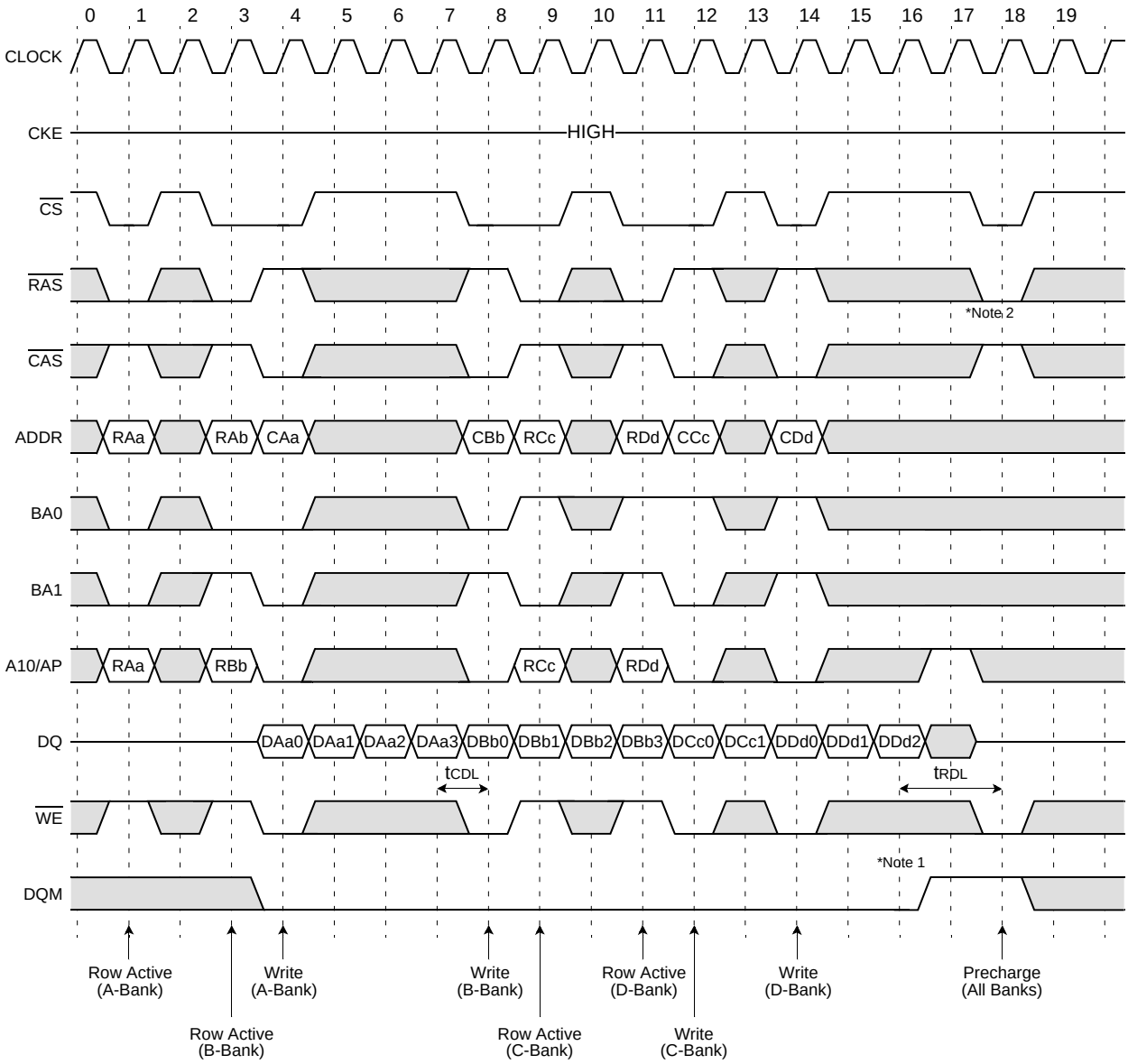
Page Read Cycle at Different Bank @Burst Length=4



***NOTE:**

1. CS can be don't cared when RAS, CAS and WE are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

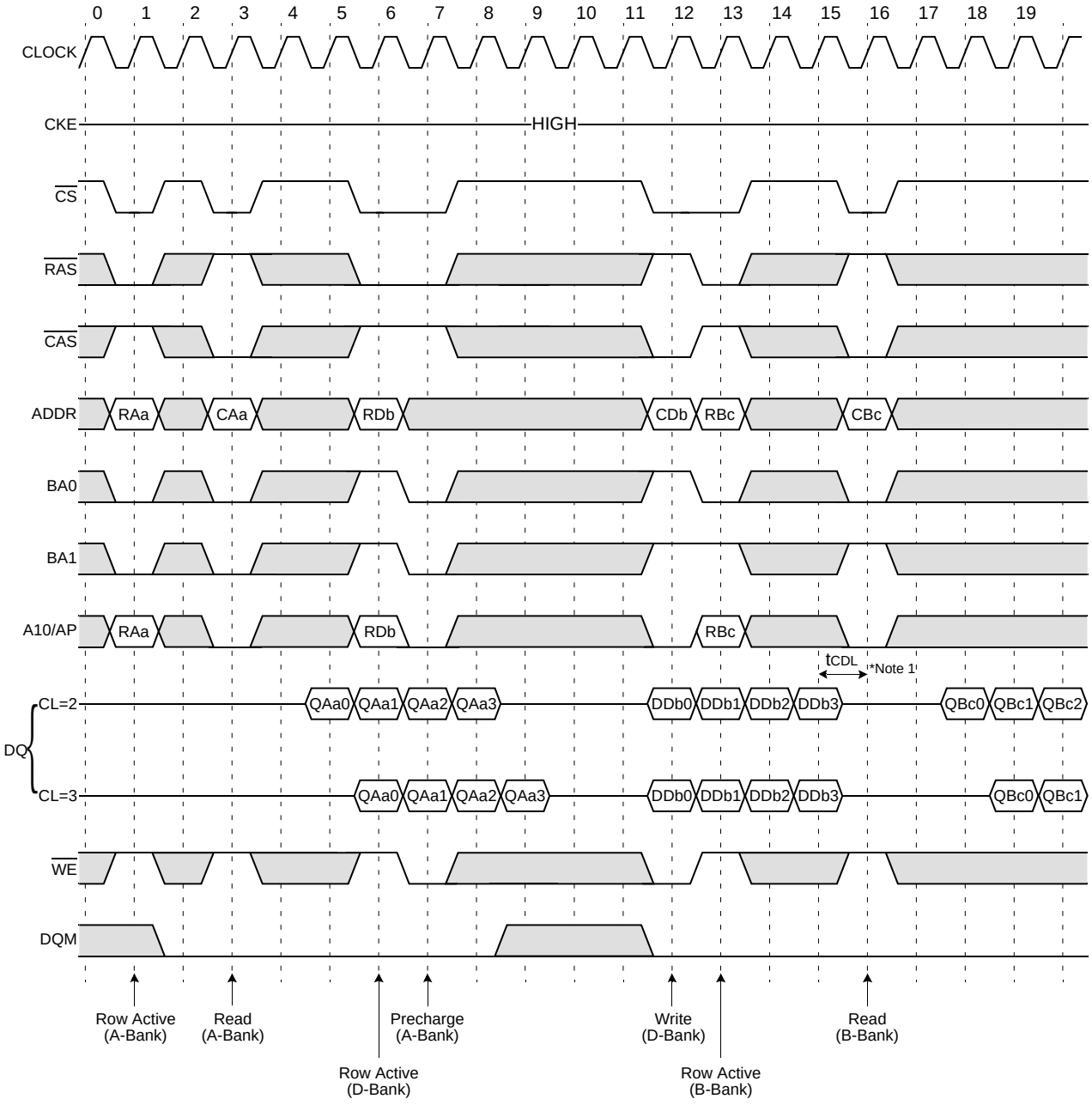
Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK



***NOTE:**

1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

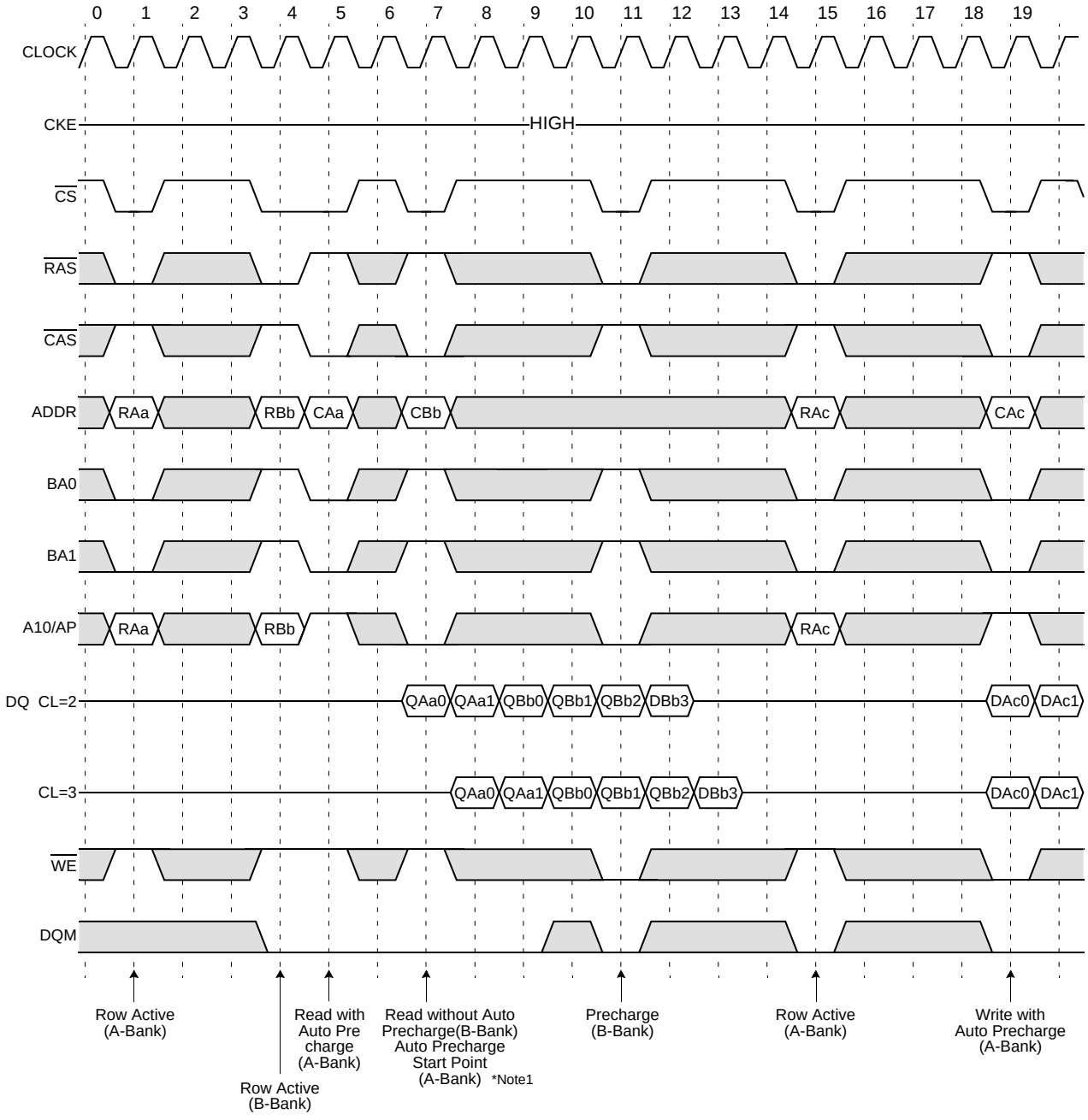
Read & Write Cycle at Different Bank @Burst Length=4



***NOTE:**

1. t_{CDL} should be met to complete write.

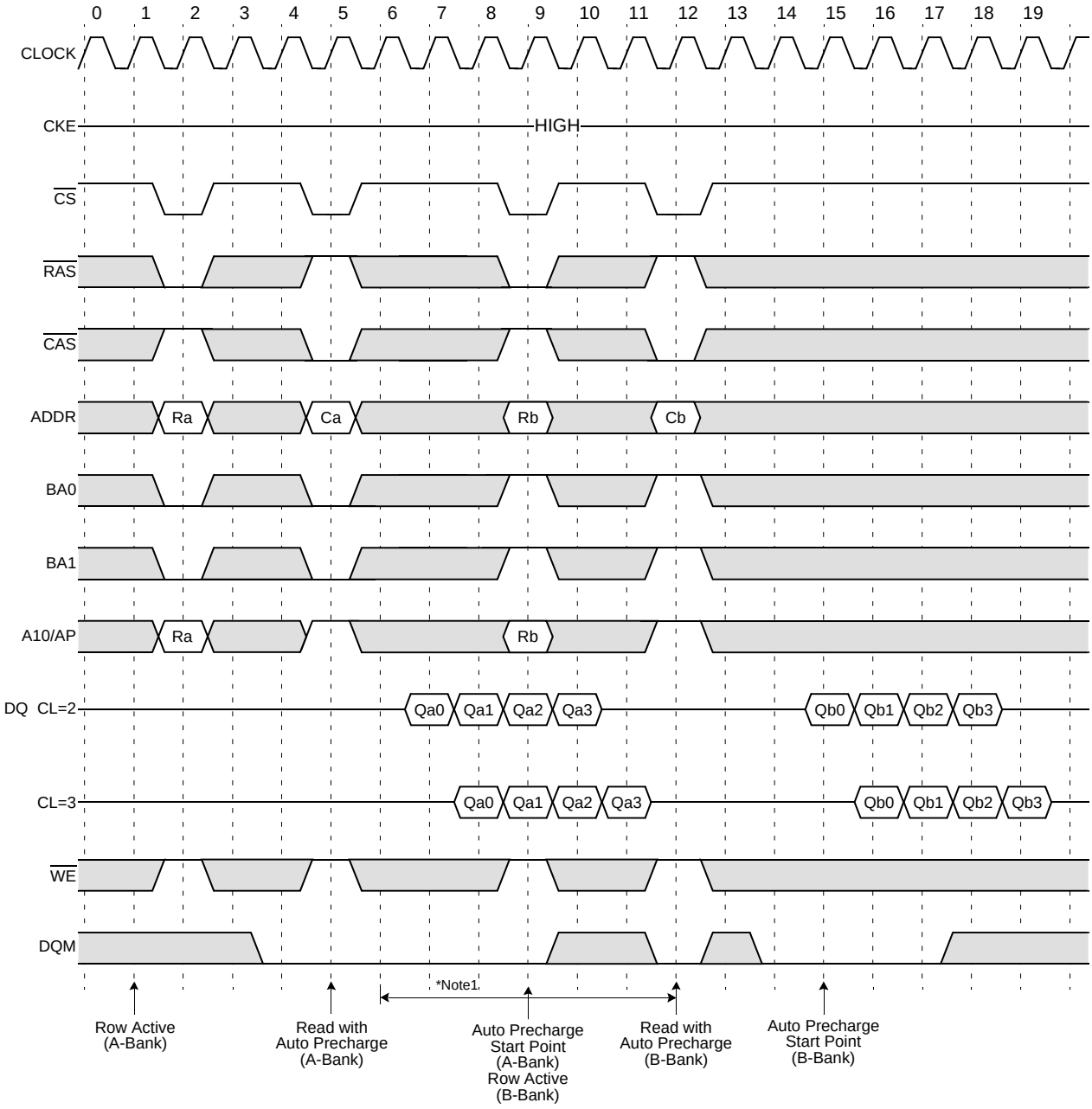
Read & Write Cycle with Auto Precharge I @Burst Length=4



***NOTE:**

1. When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
   - if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point .
   - any command can not be issued at A-Bank during t_{RP} after A-Bank auto precharge starts.

Read & Write Cycle with Auto Precharge II @Burst Length=4

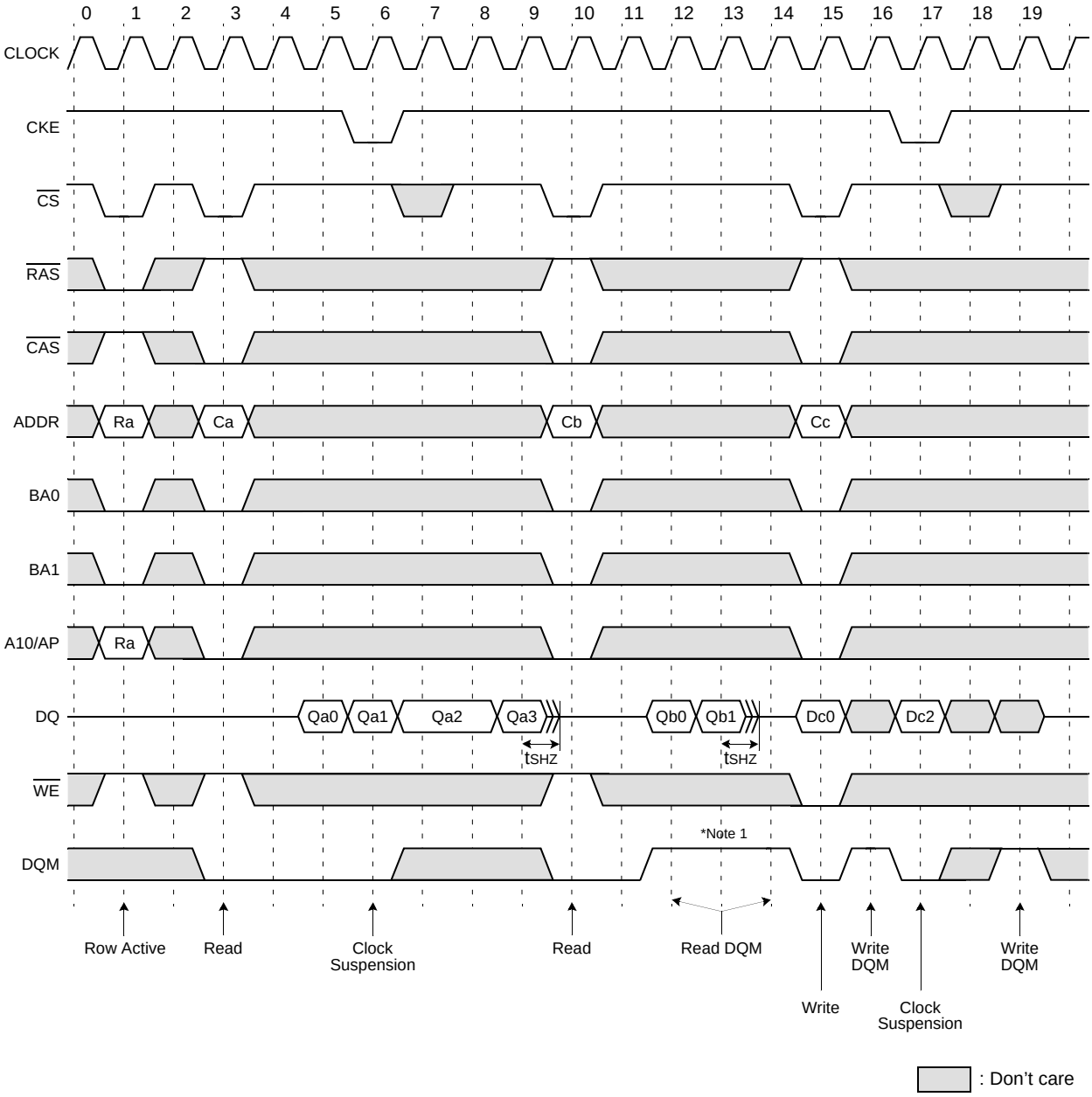


: Don't care

***NOTE:**

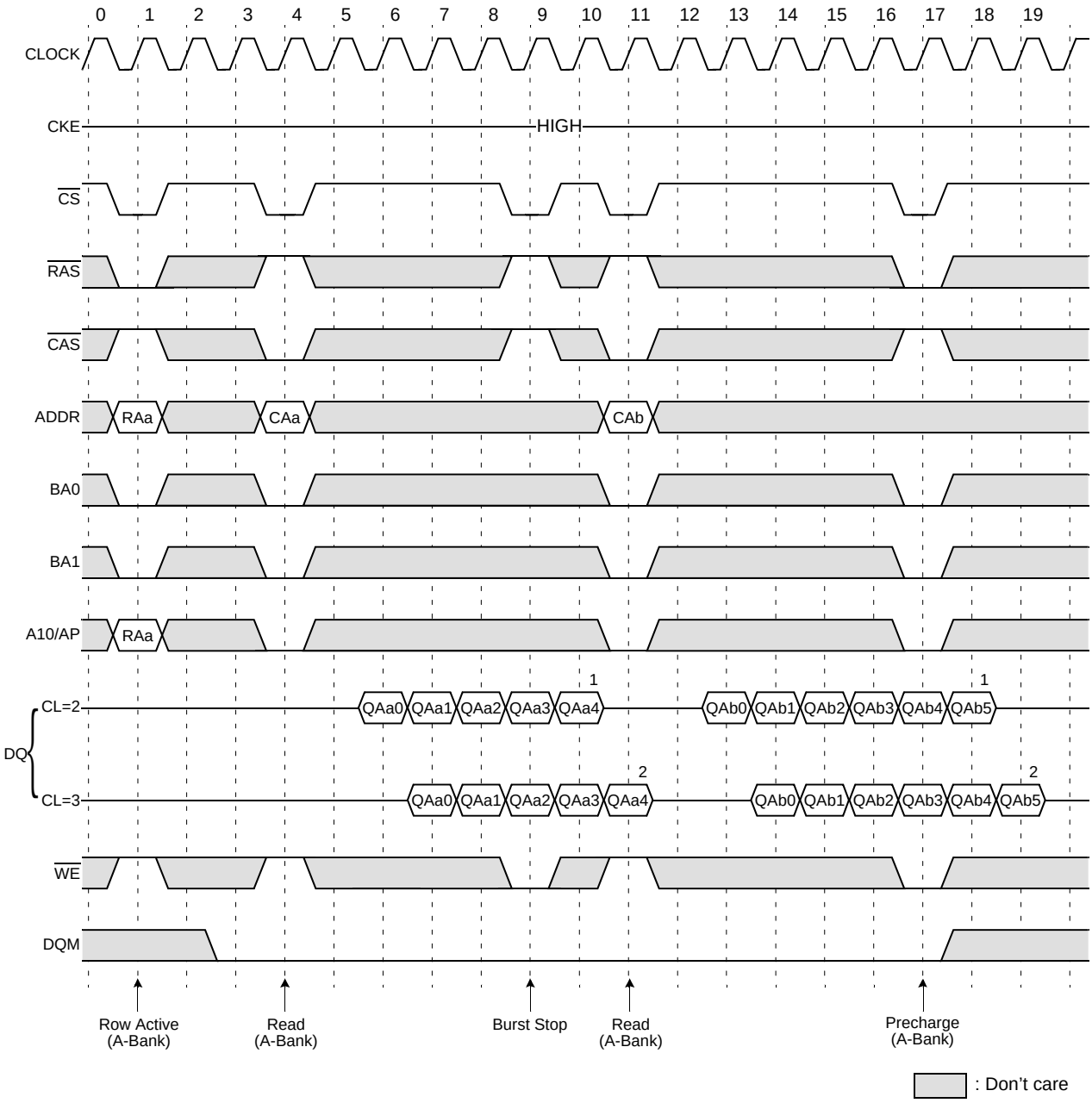
1. Any command to A-bank is not allowed in this period.
   t_{RP} is determined from at auto precharge start point

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



***NOTE:**
1. DQM is needed to prevent bus contention.

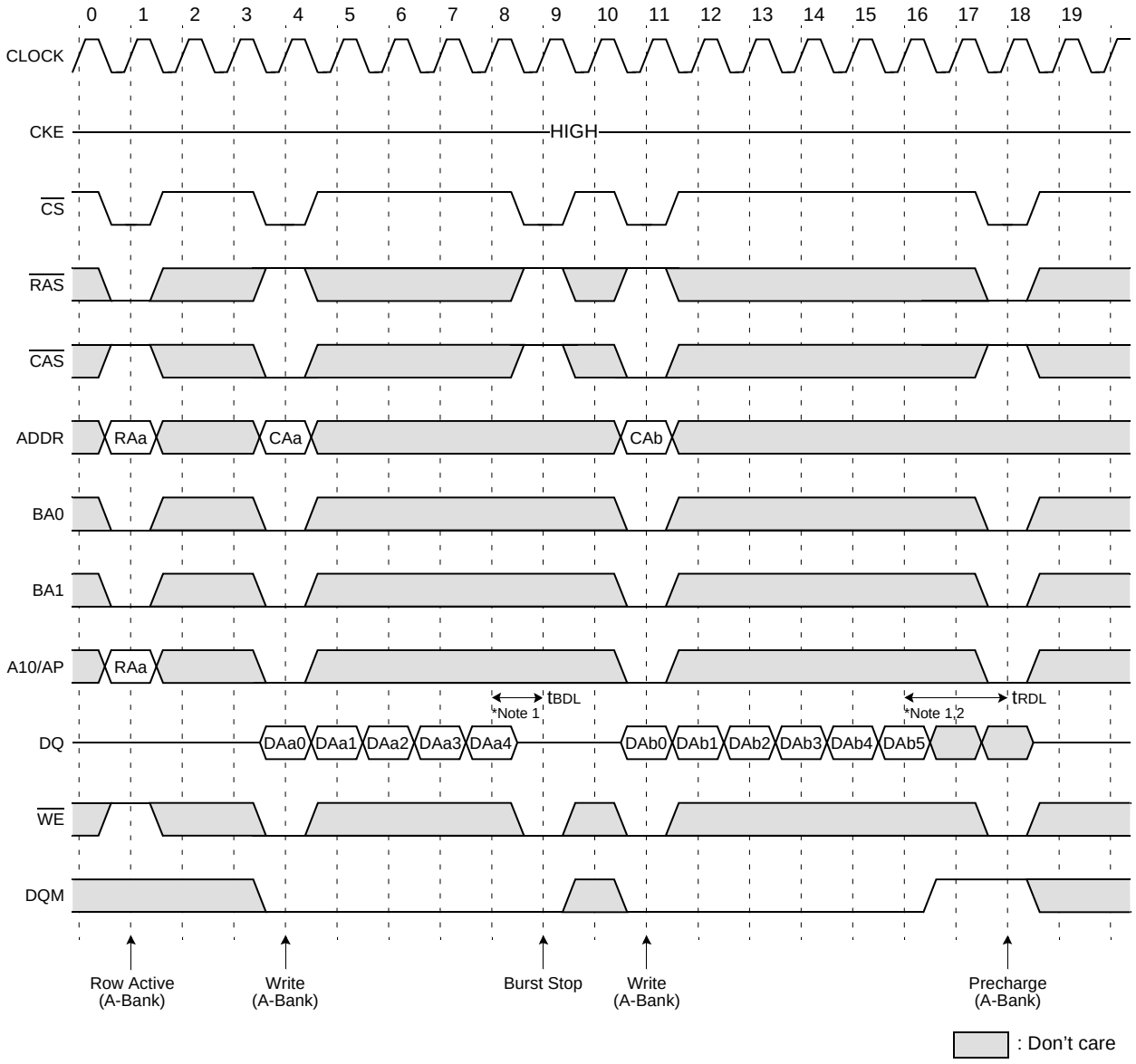
Read Interrupted by Precharge Command & Read Burst Stop Cycle @Full Page Burst



***NOTE:**

1. At full page mode, burst is finished by burst stop or precharge.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
   Both cases are illustrated above timing diagram. See the label 1, 2 on them.
   But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

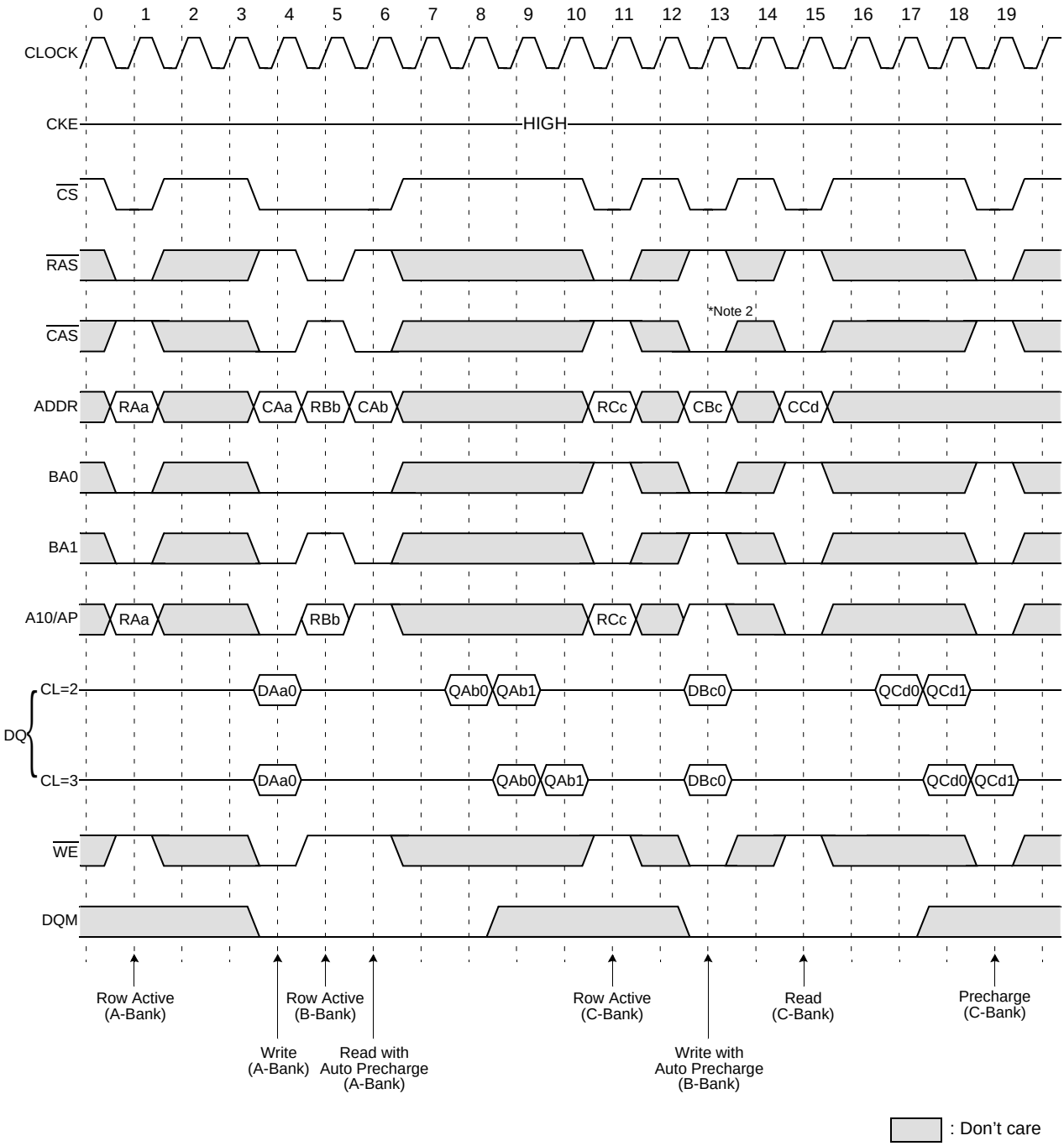
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK



***NOTE:**

1. At full page mode, burst is finished by burst stop or precharge.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

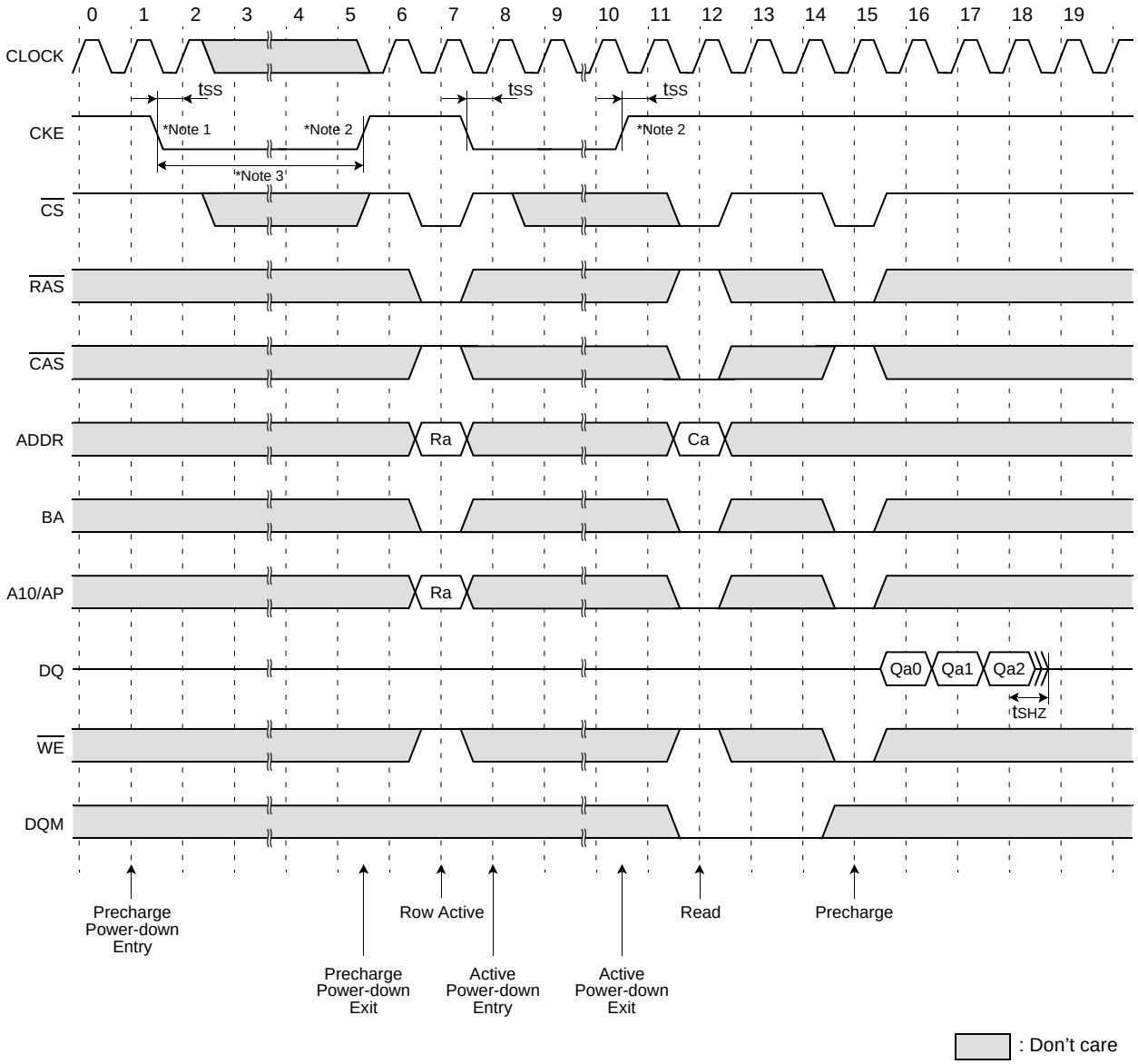
Burst Read Single bit Write Cycle @Burst Length=2



***NOTE:**

1. BRSW modes is enabled by setting A9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
   Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
   the next cycle starts the precharge.

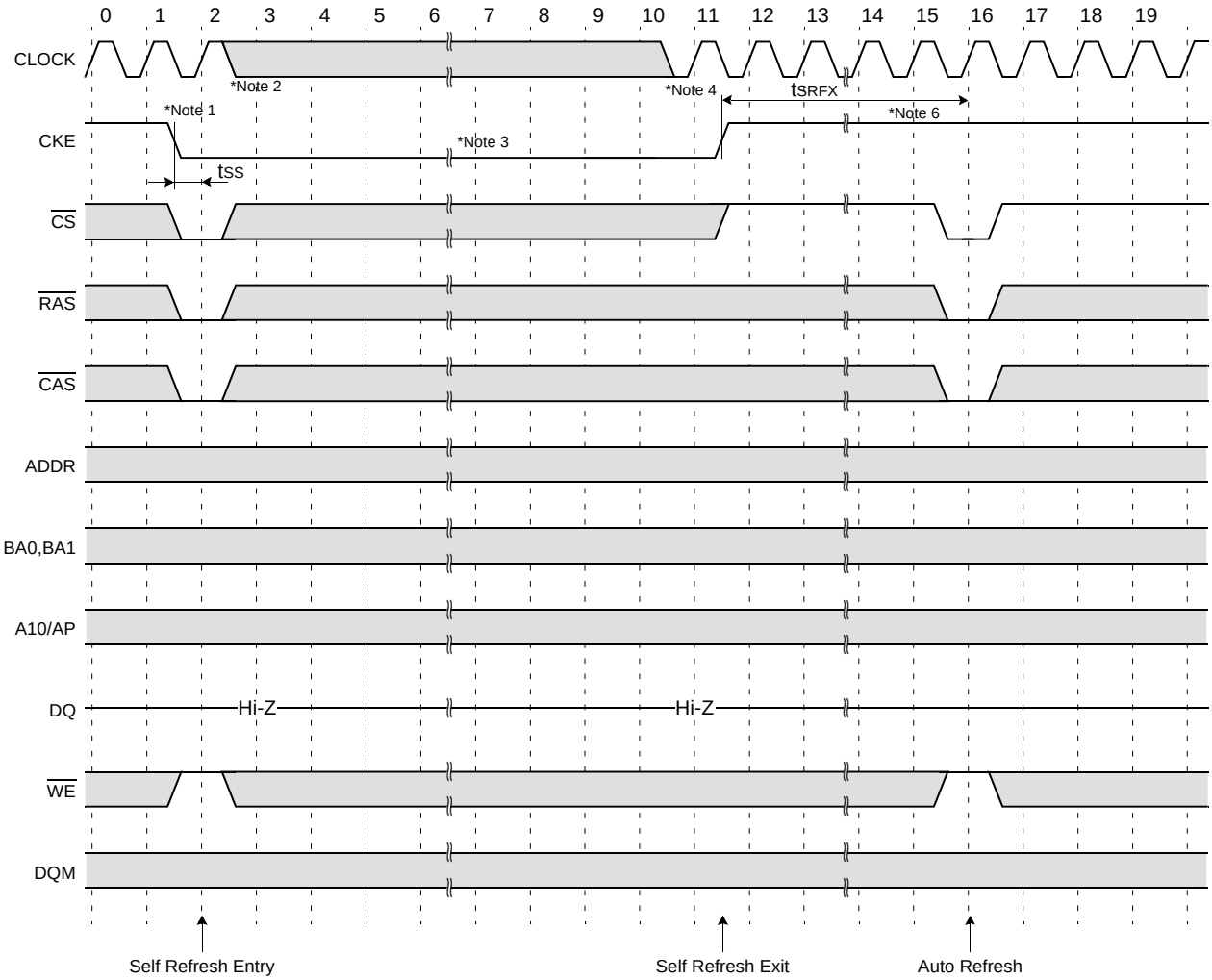
Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



***NOTE:**

1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tSS prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



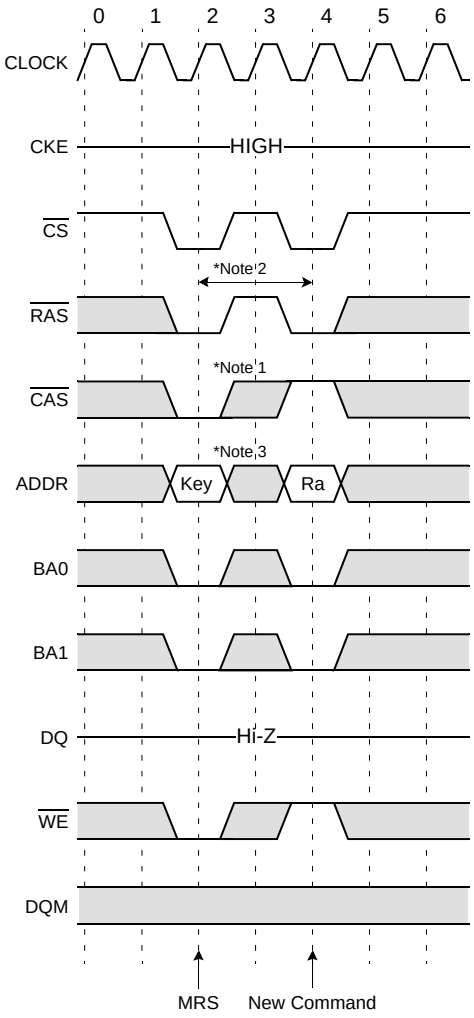
***NOTE:**
TO ENTER SELF REFRESH MODE

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

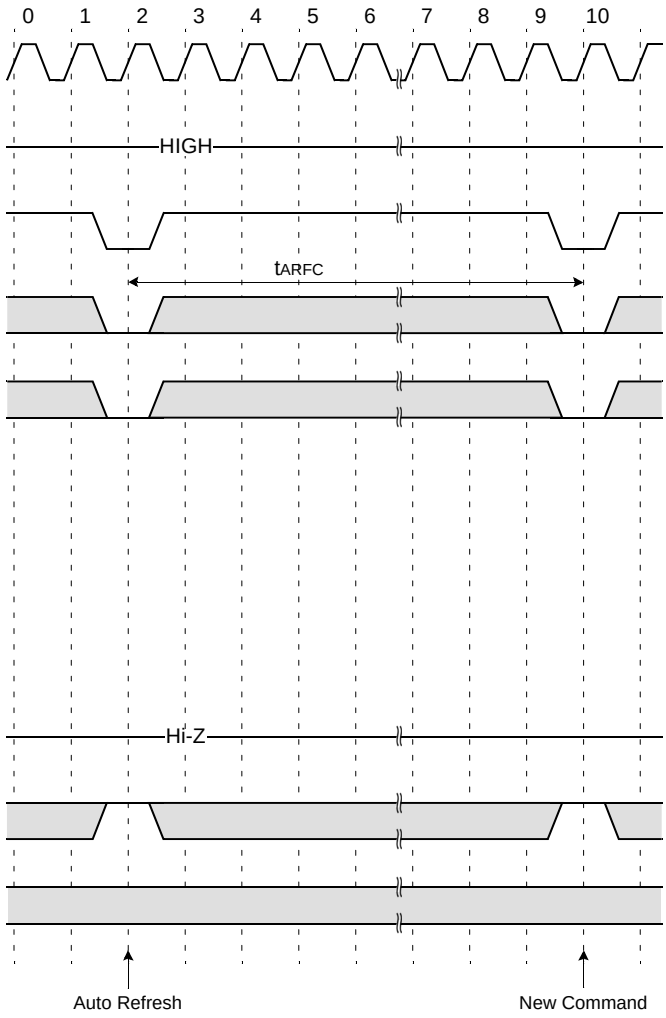
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K cycle(64Mb ,128Mb) or 8K cycle(256Mb, 512Mb) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle

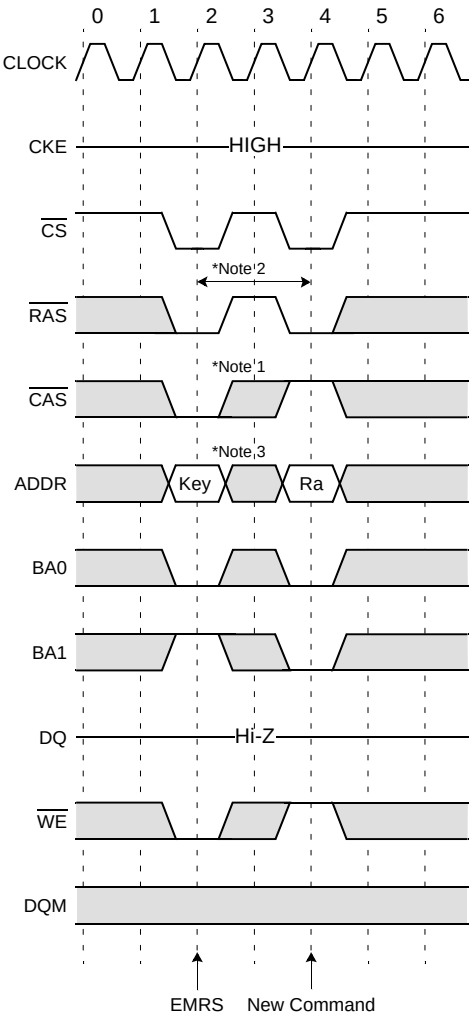


* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

: Don't care

***NOTE:**
MODE REGISTER SET CYCLE
1. CS, RAS, CAS, BA0, BA1 & WE activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new RAS activation.
3. Please refer to Mode Register Set table.

Extended Mode Register Set Cycle



: Don't care

***NOTE:**
EXTENDED MODE REGISTER SET CYCLE
1. CS, RAS, CAS, BA0, BA1 & WE activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new RAS activation.
3. Please refer to Mode Register Set table.

PACKAGE DIMENSION

137-Ball Fine pitch Ball Grid Array Package (measured in millimeters)

Units:millimeters