## Document Title

**Multi-Chip Package MEMORY**

***256M Bit (16Mx16) Nand Flash / 64M Bit (4Mx16) Burst UtRAM***

## Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Initial Draft<br>- 256Mb NAND C-Die_Ver 2.6<br>- 64Mb UtRAM B-Die(Burst)_Ver 0.4 | September 20, 2003 | Preliminary |
| 0.1 | Revised<br><UtRAM><br>- Deleted PAR support in 64Mb UtRAM<br>- Changed $I_{SB1}$ from 150μA into 180μA<br>- Changed $I_{SBD}$ from 20μA into 25μA<br>- Changed tCSLH in SYNCHRONOUS AC CHARACTERISTICS from 5ns into 10ns<br><NAND Flash><br>- Changed NVB(Valid Block Number)from 2013(Min) Blocks to 2018(Min) Blocks<br>- Changed tWC from 45(min)ns to 50(min)ns | November 19, 2003 | Preliminary |

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

## Multi-Chip Package MEMORY
## *256M Bit (16Mx16) Nand Flash / 64M Bit (4Mx16) Burst UtRAM*

## FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 111-ball FBGA Type - 10x11mm, 0.8mm pitch, 1.4mm (Max.) Thickness

<NAND>
- Power Supply Voltage : 1.7~1.95V
- Organization
  - Memory Cell Array : (16M + 512K)bit x16bit
  - Data Register : (256 + 8)bit x16bit
- Automatic Program and Erase
  - Page Program : (256 + 8)Word
  - Block Erase : (8K + 256)Word
- Page Read Operation
  - Page Size : (256 + 8)Word
  - Random Access : 10μs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back
- Unique ID for Copyright Protection

<U*t*RAM>
- Process Technology: CMOS
- Organization: 4M x16 bit
- Power Supply Voltage: $V_{CC}$ 2.7~3.1V / $V_{CCQ}$ 1.7~2.0V
- Three State Outputs
- Compatible with Low Power SRAM
- Supports MRS (Mode Register Set)
- Supports Asynchronous Read/Write Operation in Asynchronous-mode
- Supports Synchronous Burst Read and Asynchronous Write Operation in Synchronous mode
- Synchronous Burst Read Operation
  - Supports 4 word / 8 word / 16 word Burst Read mode
  - Supports Linear Burst type & Interleave Burst type
  - Latency support : 3, 4, 5, 6 (depends on clock frequency)
- Max. Burst Clock Frequency : 54MHz

## GENERAL DESCRIPTION

The K5Q5764G0M is a Multi Chip Package Memory which combines 256Mbit Nand Flash Memory, 64Mbit Unit Transistor CMOS RAM.

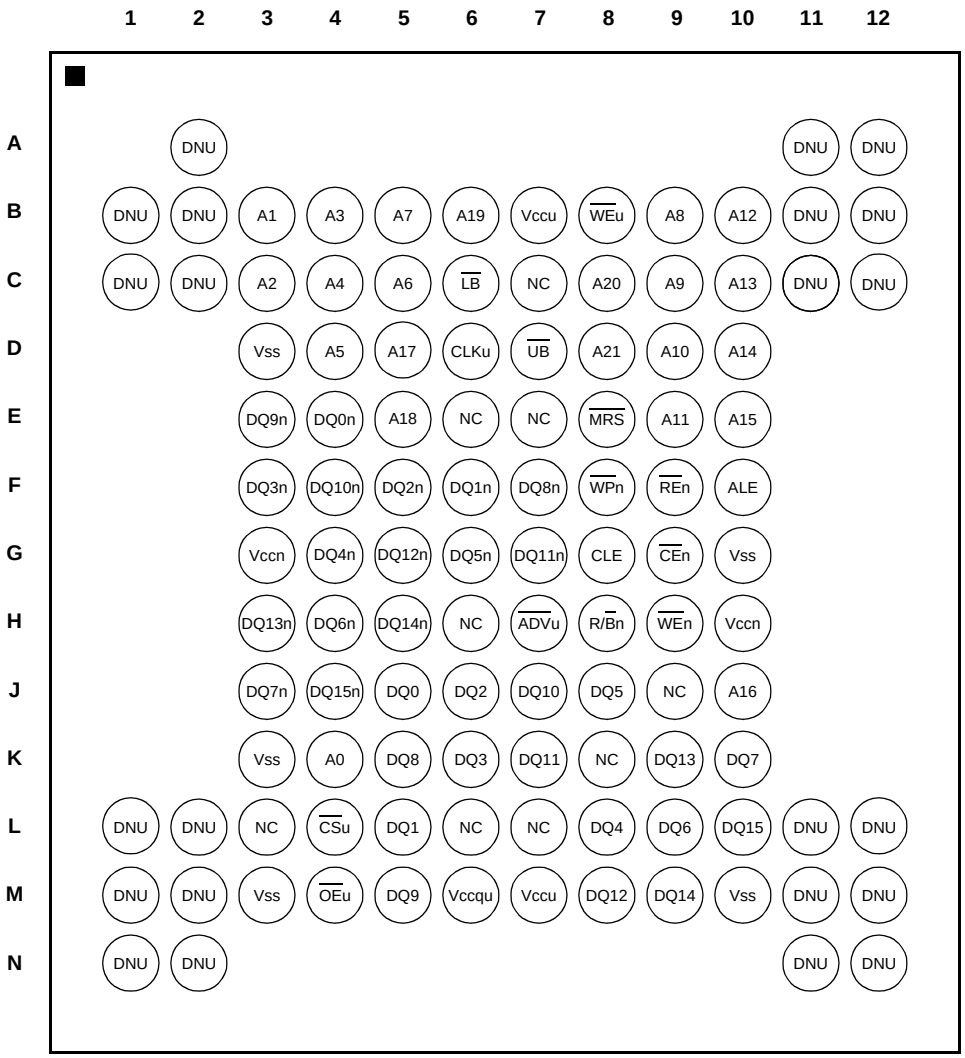
256Mbit NAND Flash memory is organized as 16M x16 bits and 64Mbit U*t*RAM is organized as 4M x16 bits.

In 256Mbit NAND Flash, a 264-word page program can be typically achieved within 200us and an 8K-word block erase can be typically achieved within 2ms. In serial read operation, a word can be read by 50ns. DQ pins serve as the ports for address and data input/output as well as command inputs. Even the write-intensive systems can take advantage of FLASH′s extended reliability of 100K program/erase cycles with real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications.

In 64Mb burst UtRAM, the device supports DPD(Deep Power Down) mode for power saving. DPD mode is controlled by $\overline{MRS}$ pin. The device supports MRS(Mode Register Set) and synchronous burst read mode.

The K5Q5764G0M is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 111-ball FBGA Type.

## PIN CONFIGURATION




**111-FBGA: Top View (Ball Down)**

## PIN DESCRIPTION

| Ball Name | Description | Ball Name | Description |
|---|---|---|---|
| $A_0$ to $A_{21}$ | Address Input Balls (UtRAM) | $R/\overline{B}_n$ | Ready/Busy (Flash Memory) |
| $DQ_{0n}$ to $DQ_{15n}$ | Data Input/Output Balls (Flash Memory) | $\overline{MRS}$ | Mode Register Set (UtRAM) |
| $DQ_0$ to $DQ_{15}$ | Data Input/Output Balls (UtRAM) | $\overline{CE}_n$ | Chip Enable (Flash Memory) |
| $\overline{WP}_n$ | Write Protection (Flash Memory) | $\overline{CS}_u$ | Chip Select (UtRAM) |
| $V_{ccn}$ | Power Supply (Flash Memory) | $CLK_u$ | Clock (UtRAM) |
| $V_{ccu}$ | Power Supply (UtRAM) | $\overline{ADV}_u$ | Address Input Valid (UtRAM) |
| $V_{ccqu}$ | Data Out Power (UtRAM) | $\overline{WE}_n$ | Write Enable (Flash Memory) |
| $V_{ss}$ | Ground (Common) | $\overline{WE}_u$ | Write Enable (UtRAM) |
| $\overline{UB}$ | Upper Byte Enable (UtRAM) | $\overline{OE}_u$ | Output Enable (UtRAM) |
| $\overline{LB}$ | Lower Byte Enable (UtRAM) | $\overline{RE}_n$ | Read Enable (Flash Memory) |
| ALE | Address Latch Enable (Flash Memory) | NC | No Connection |
| CLE | Command Latch Enable (Flash Memory) | DNU | Do Not Use |

## ORDERING INFORMATION

**K 5 Q 57 64 G 0 M - F 0 18**

**Samsung**
**MCP(2 Chip) Memory**

**Device Type**
NAND Flash + UtRAM

**NAND Flash Density , Org.**
**57 :** 256Mbit, x16

**UtRAM Density , Org.**
**64 :** 64Mbit, x16(Burst)

**Operating Voltage**
**G :** 1.8V/1.8V(NAND Flash), 3.0V/1.8V(UtRAM)

**Flash Boot Block Mode**
**0 :** None

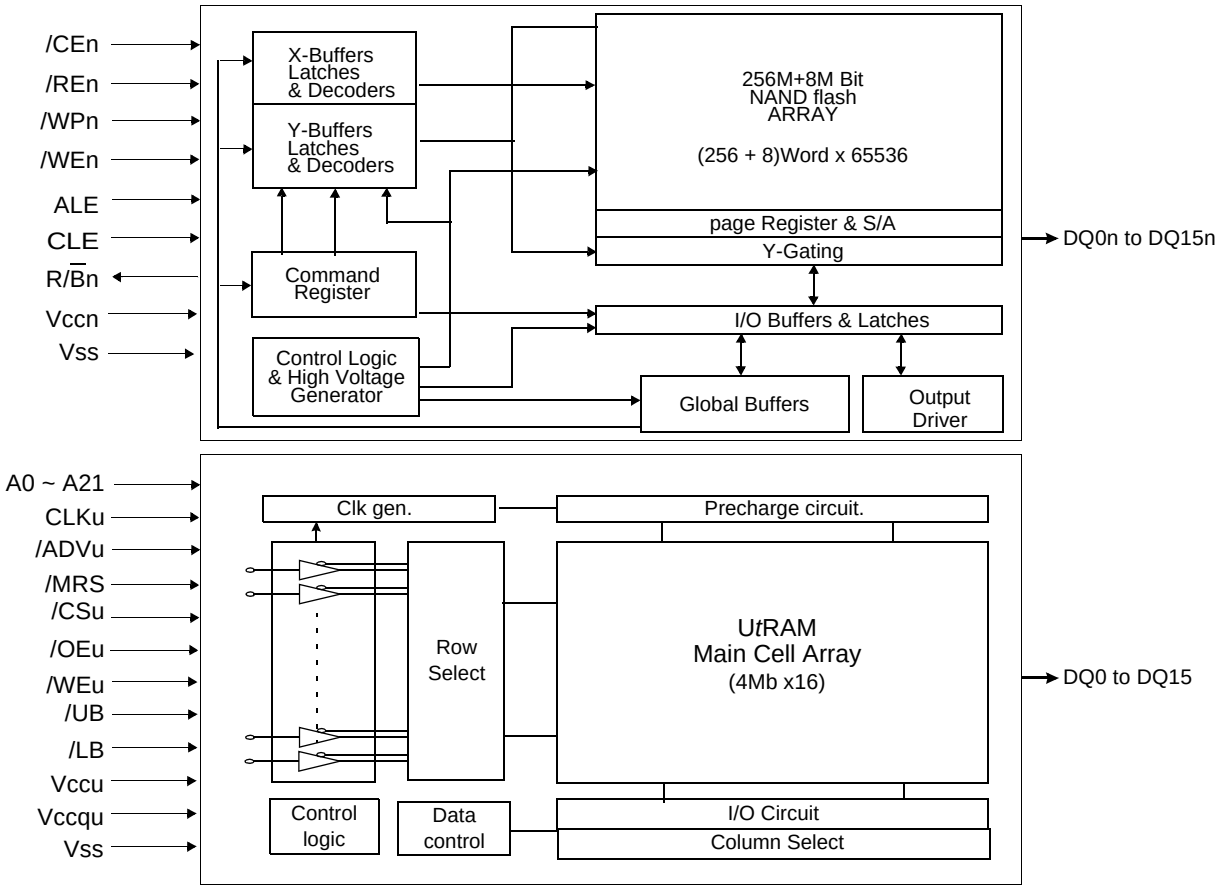
**Version**
**M :** 1st Generation

**Package**
**F :** FBGA

**NAND Flash Speed**
**0 :** NONE

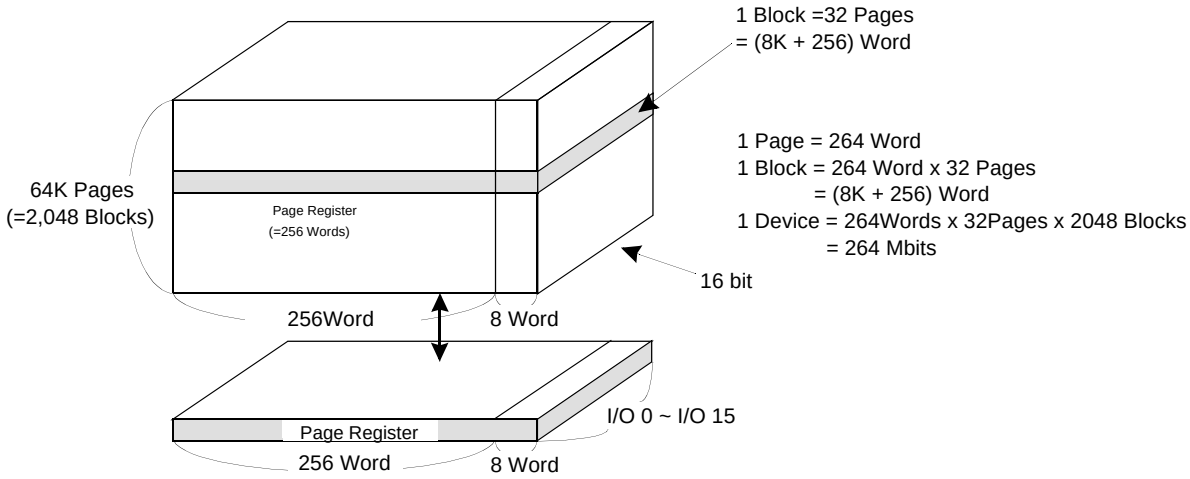
**UtRAM Speed**
**18:** 18.5ns(54MHz)

## FUNCTIONAL BLOCK DIAGRAM



# 256Mb(16M x 16)
# NAND Flash C-Die

## Figure 1. NAND Flash ARRAY ORGANIZATION




| | I/O 0 | I/O 1 | I/O 2 | I/O 3 | I/O 4 | I/O 5 | I/O 6 | I/O 7 | I/O8 to 15 | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1st Cycle | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | L* | **Column Address** |
| 2nd Cycle | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_{16}$ | L* | **Row Address (Page Address)** |
| 3rd Cycle | $A_{17}$ | $A_{18}$ | $A_{19}$ | $A_{20}$ | $A_{21}$ | $A_{22}$ | $A_{23}$ | $A_{24}$ | L* | |

**NOTE** : Column Address : Starting Address of the Register.

* L must be set to "Low".

## PRODUCT INTRODUCTION

The NAND Flash is a 264Mbit(276,824,064 bit) memory organized as 131,072 rows(pages) by 264 columns. Spare eight columns are located from column address of 256~263. A 264-word data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 16 cells. Total 135168 NAND cells reside in a block. The array organization is shown in Figure 1. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4096 separately erasable 8K-Word blocks. It indicates that the bit by bit erase operation is prohibited on the NAND Flash.

The NAND Flash has addresses multiplexed into lower 8 IO's. The NAND Flash allows sixteen bit wide data transport into and out of page registers. This scheme dramatically reduces pin counts while providing high performance and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through IO′s by bringing $\overline{WE}$ to low while $\overline{CE}$n is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the IO pins. Some commands require one bus cycle. For example, Reset command, Read command, Status Read command, etc require just one cycle bus. Some other commands like Page Program and Copy-back Program and Block Erase, require two cycles: one cycle for setup and the other cycle for execution. The 32M-word physical space requires 25 addresses, thereby requiring four cycles for word-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the NAND Flash.

### Table 1. COMMAND SET

| Function | 1st. Cycle | 2nd. Cycle | Acceptable Command during Busy |
|---|---|---|---|
| Read 1 | 00h | - | |
| Read 2 | 50h | - | |
| Read ID | 90h | - | |
| Reset | FFh | - | O |
| Page Program | 80h | 10h | |
| Copy-Back Program | 00h | 8Ah | |
| Block Erase | 60h | D0h | |
| Read Status | 70h | - | O |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN/OUT}$ | -0.6 to + 2.45 | V |
| | $V_{CC}$ | -0.2 to + 2.45 | |
| | $V_{CCQ}$ | -0.2 to + 2.45 | |
| Temperature Under Bias | $T_{BIAS}$ | -40 to +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |
| Short Circuit Current | Ios | 5 | mA |

**NOTE** :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is $V_{CC}$,+0.3V which, during transitions, may overshoot to $V_{CC}$+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, $T_A$=-25 to 85°C)

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 1.7 | 1.8 | 1.95 | V |
| Supply Voltage | $V_{CCQ}$ | 1.7 | 1.8 | 1.95 | V |
| Supply Voltage | $V_{SS}$ | 0 | 0 | 0 | V |

## DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Current | Sequential Read | $I_{CC1}$ | tRC=50ns, $\overline{CE}$=$V_{IL}$, $I_{OUT}$=0mA | - | 8 | 15 | mA |
| | Program | $I_{CC2}$ | - | - | 8 | 15 | |
| | Erase | $I_{CC3}$ | - | - | 8 | 15 | |
| Stand-by Current(TTL) | | $I_{SB1}$ | $\overline{CE}$=$V_{IH}$, $\overline{WP}$=0V/$V_{CC}$ | - | - | 1 | |
| Stand-by Current(CMOS) | | $I_{SB2}$ | $\overline{CE}$=$V_{CC}$-0.2, $\overline{WP}$=0V/$V_{CC}$ | - | 10 | 50 | µA |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 to Vcc(max) | - | - | ±10 | |
| Output Leakage Current | | $I_{LO}$ | $V_{OUT}$=0 to Vcc(max) | - | - | ±10 | |
| Input High Voltage | | $V_{IH}$ | I/O pins | $V_{CCQ}$-0.4 | - | $V_{CCQ}$ +0.3 | V |
| | | | Except I/O pins | $V_{CC}$-0.4 | - | $V_{CC}$ +0.3 | |
| Input Low Voltage, All inputs | | $V_{IL}$ | - | -0.3 | - | 0.4 | |
| Output High Voltage Level | | $V_{OH}$ | $I_{OH}$=-100µA | VccQ-0.1 | - | - | |
| Output Low Voltage Level | | $V_{OL}$ | $I_{OL}$=100uA | - | - | 0.1 | |
| Output Low Current(R/$\overline{B}$) | | $I_{OL}$(R/$\overline{B}$) | $V_{OL}$=0.1V | 3 | 4 | - | mA |

**NOTE** : $V_{IL}$ can undershoot to -0.4V and $V_{IH}$ can overshoot to $V_{CC}$ +0.4V for durations of 20 ns or less.

## VALID BLOCK

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Valid Block Number | $N_{VB}$ | 2018 | - | 2048 | Blocks |

**NOTE** :
1. The NAND Flash may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K Program/Erase cycles.
3. Minimum 1004 valid blocks are guaranteed for each contiguous 128Mb memory space.

## AC TEST CONDITION

( Vcc=1.7V~1.95V , $T_A$=-25 to 85°C unless otherwise noted)

| Parameter | Value |
|---|---|
| Input Pulse Levels | 0V to VccQ |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | VccQ/2 |
| Output Load (VccQ:1.8V +/-10%) | 1 TTL GATE and CL=30pF |

## CAPACITANCE(TA=25°C, VCC=1.8V, f=1.0MHz)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input/Output Capacitance | $C_{I/O}$ | $V_{IL}$=0V | - | 10 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 10 | pF |

**NOTE** : Capacitance is periodically sampled and not 100% tested.

## MODE SELECTION

| CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | $\overline{WP}$ | Mode | |
|---|---|---|---|---|---|---|---|
| H | L | L | ↑ | H | X | Read Mode | Command Input |
| L | H | L | ↑ | H | X | | Address Input(4clock) |
| H | L | L | ↑ | H | H | Write Mode | Command Input |
| L | H | L | ↑ | H | H | | Address Input(4clock) |
| L | L | L | ↑ | H | H | Data Input | |
| L | L | L | H | ↓ | X | Data Output | |
| L | L | X | H | H | X | During Read(Busy) | |
| X | X | X | X | X | H | During Program(Busy) | |
| X | X | X | X | X | H | During Erase(Busy) | |
| X | X(1) | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/$V_{CC}$(2) | Stand-by | |

**NOTE** :
1. X can be VIL or VIH.
2. WP should be biased to CMOS high or CMOS low for standby.

## Program/Erase Characteristics

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Program Time | | $t_{PROG}$ | - | 200 | 500 | µs |
| Number of Partial Program Cycles in the Same Page | Main Array | Nop | - | - | 2 | cycles |
| | Spare Array | | - | - | 3 | cycles |
| Block Erase Time | | $t_{BERS}$ | - | 2 | 3 | ms |

## AC Timing Characteristics for Command / Address / Data Input

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CLE Set-up Time | $t_{CLS}$ | 0 | - | ns |
| CLE Hold Time | $t_{CLH}$ | 10 | - | ns |
| $\overline{CE}$ Setup Time | $t_{CS}$ | 0 | .- | ns |
| $\overline{CE}$ Hold Time | $t_{CH}$ | 10 | - | ns |
| $\overline{WE}$ Pulse Width | $t_{WP}$ | 25 (1) | - | ns |
| ALE Setup Time | $t_{ALS}$ | 0 | - | ns |
| ALE Hold Time | $t_{ALH}$ | 10 | - | ns |
| Data Setup Time | $t_{DS}$ | 20 | - | ns |
| Data Hold Time | $t_{DH}$ | 10 | - | ns |
| Write Cycle Time | $t_{WC}$ | 50 | - | ns |
| $\overline{WE}$ High Hold Time | $t_{WH}$ | 15 | - | ns |

**NOTE** :
1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

## AC Characteristics for Operation

| Parameter | Symbol | Min | Max | Uni |
|---|---|---|---|---|
| Data Transfer from Cell to Register | $t_R$ | - | 10 | µs |
| ALE to $\overline{RE}$ Delay | $t_{AR}$ | 10 | - | ns |
| CLE to $\overline{RE}$ Delay | $t_{CLR}$ | 10 | - | ns |
| Ready to $\overline{RE}$ Low | $t_{RR}$ | 20 | - | ns |
| $\overline{RE}$ Pulse Width | $t_{RP}$ | 25 | - | ns |
| $\overline{WE}$ High to Busy | $t_{WB}$ | - | 100 | ns |
| Read Cycle Time | $t_{RC}$ | 50 | - | ns |
| $\overline{CE}$ Access Time | $t_{CEA}$ | - | 45 | ns |
| $\overline{RE}$ Access Time | $t_{REA}$ | - | 35 | ns |
| $\overline{RE}$ High to Output Hi-Z | $t_{RHZ}$ | - | 30 | ns |
| $\overline{CE}$ High to Output Hi-Z | $t_{CHZ}$ | - | 20 | ns |
| $\overline{RE}$ or $\overline{CE}$ High to Output hold | $t_{OH}$ | 15 | - | ns |
| $\overline{RE}$ High Hold Time | $t_{REH}$ | 15 | - | ns |
| Output Hi-Z to $\overline{RE}$ Low | $t_{IR}$ | 0 | - | ns |
| $\overline{WE}$ High to $\overline{RE}$ Low | $t_{WHR}$ | 60 | - | ns |
| Device Resetting Time(Read/Program/Erase) | $t_{RST}$ | - | 5/10/500(1) | µs |

**NOTE** :
1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

## *NAND Flash Technical Notes*

### Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

### Identifying Invalid Block(s)

All device locations are erased(FFF) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st word in the spare area. Samsung makes sure that either the 1st or 2nd page sof every invalid block has non-FFFFh data at the column address of 256 and 261. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 2). Any intentional erasure of the original invalid block information is prohibited.

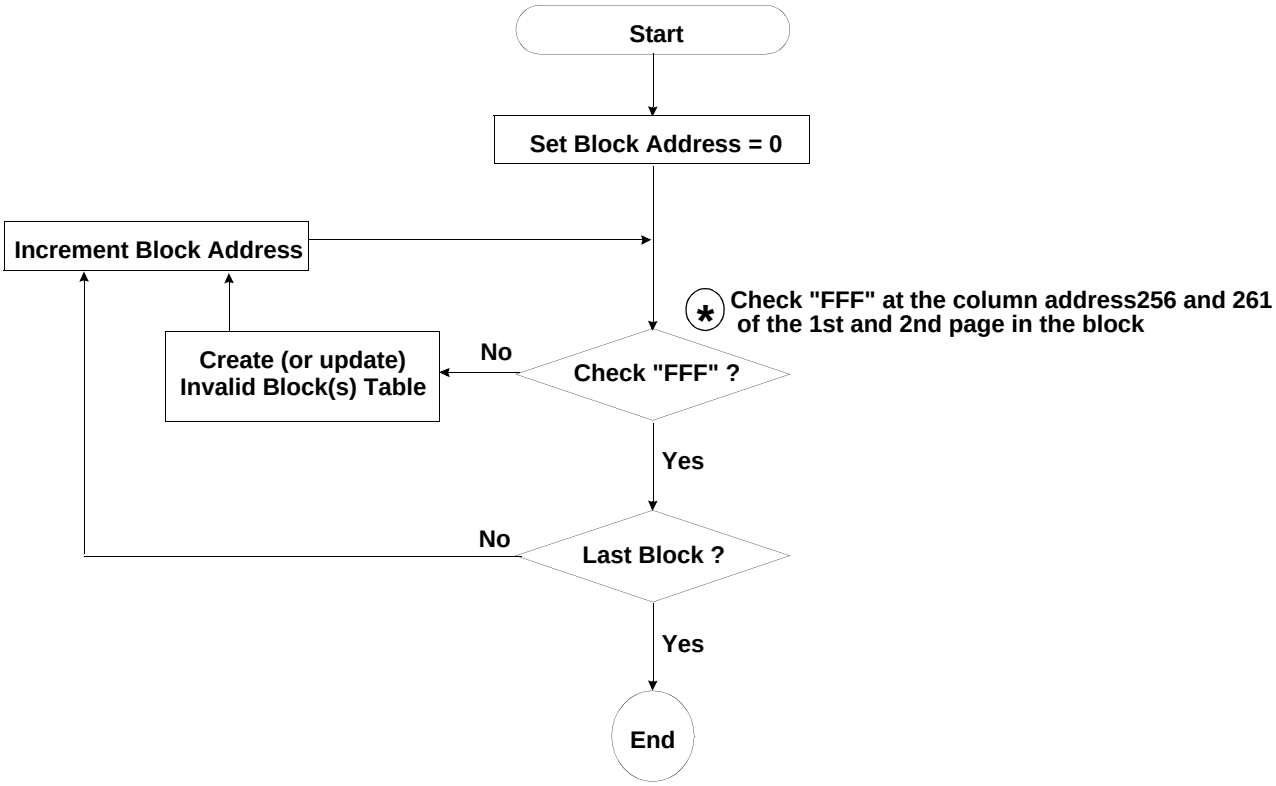



**Figure 2. Flow chart to create invalid block table.**

## *NAND Flash Technical Notes* *(Continued)*

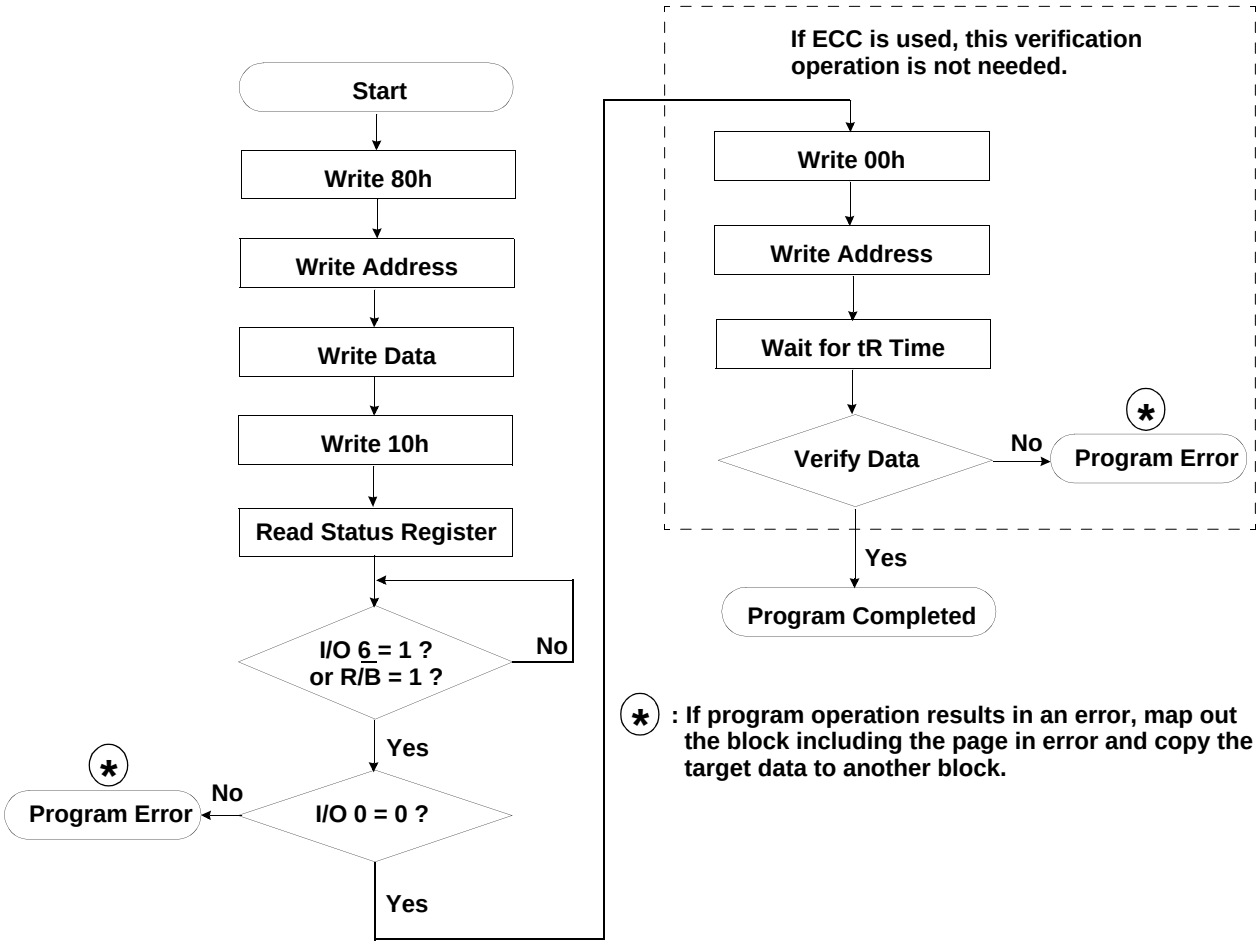
### Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

| Failure Mode | | Detection and Countermeasure sequence |
|---|---|---|
| Write | Erase Failure | Status Read after Erase --> Block Replacement |
| | Program Failure | Status Read after Program --> Block Replacement<br>Read back ( Verify after Program) --> Block Replacement<br>or ECC Correction |
| Read | Single Bit Failure | Verify ECC -> ECC Correction |

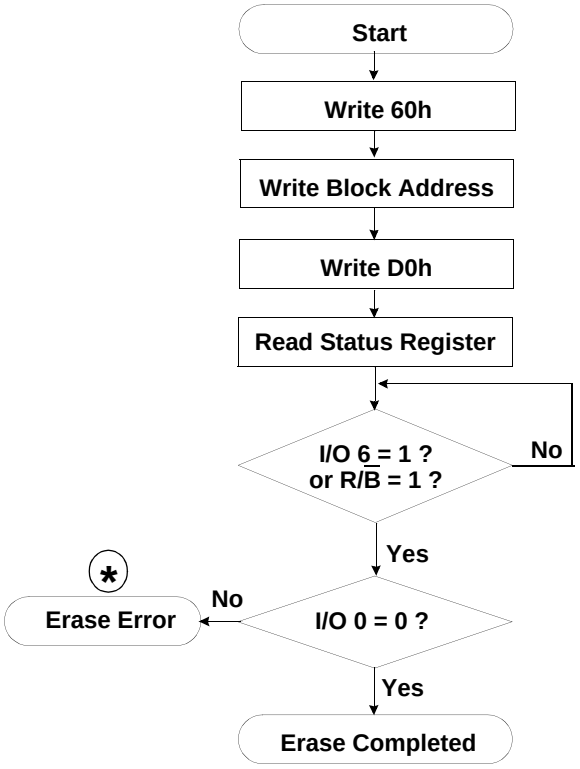
**ECC** : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

### Program Flow Chart

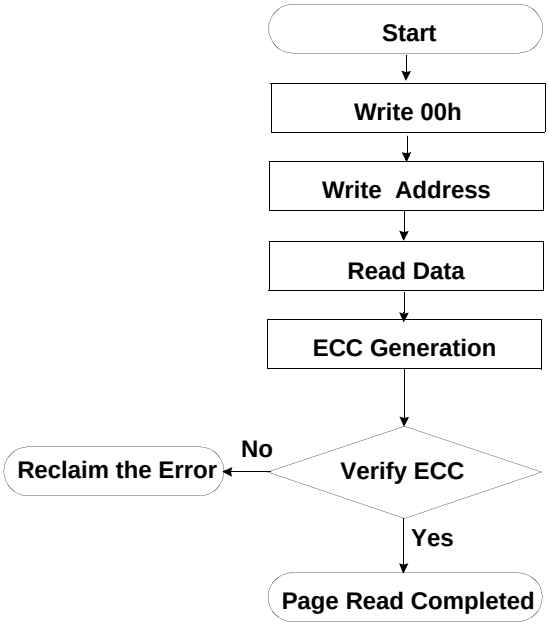


## *NAND Flash Technical Notes* *(Continued)*

### Erase Flow Chart

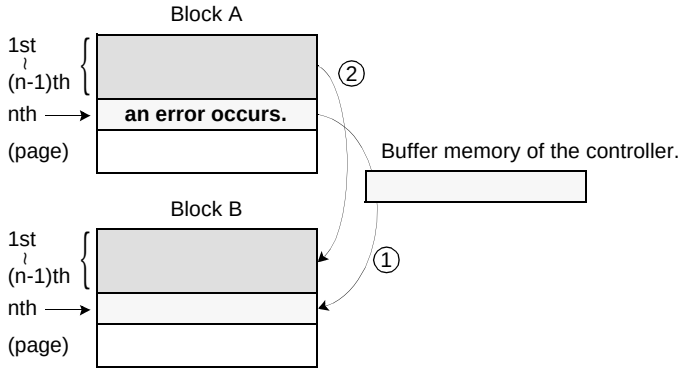



### Read Flow Chart




(*) : If erase operation results in an error, map out the failing block and replace it with another block.

### Block Replacement




* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

## Pointer Operation

Samsung NAND Flash has two address pointer commands as a substitute for the most significant column address. '00h' command sets the pointer to 'A' area(0~255word), and '50h' command sets the pointer to 'B' area(256~263word). With these commands, the starting column address can be set to any of a whole page(0~263word). '00h' or '50h' is sustained until another address pointer command is inputted. To program data starting from 'A' or 'B' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary.

### Table 2. Destination of the pointer

| Command | Pointer position | Area |
|---|---|---|
| 00h | 0 ~ 255 word | main array(A) |
| 50h | 256 ~ 263 word | spare array(B) |

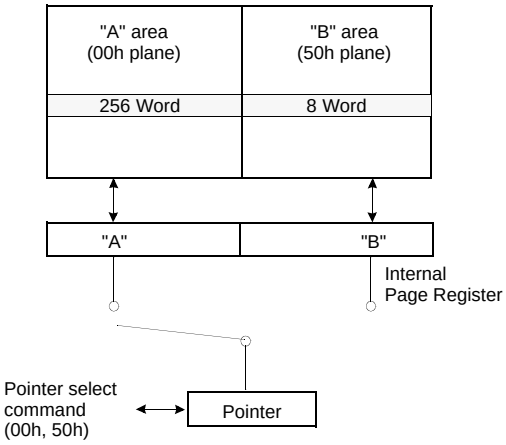
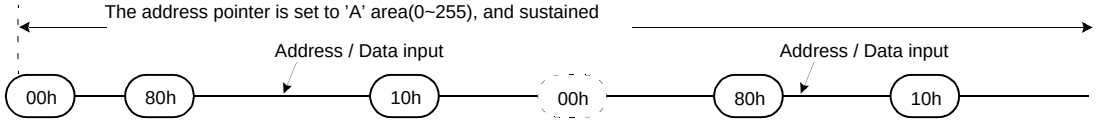



**Figure 3. Block Diagram of Pointer Operation**

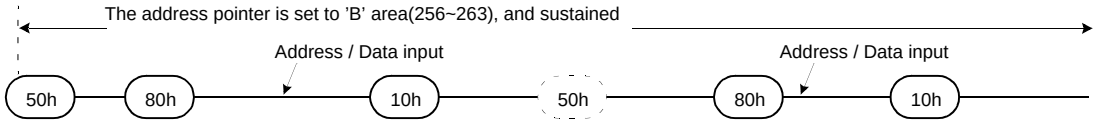
**(1) Command input sequence for programming 'A' area**




'A','B' area can be programmed.
It depends on how many data are inputted.

'00h' command can be omitted.

**(2) Command input sequence for programming 'B' area**



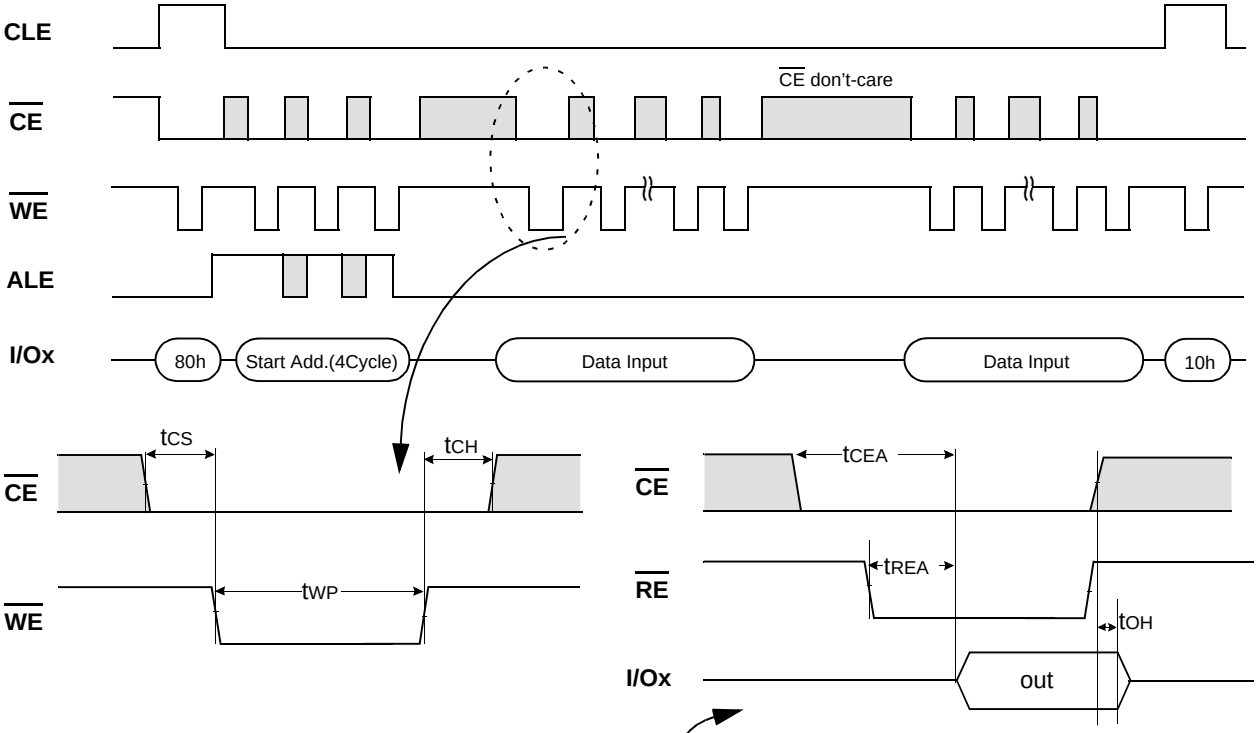

Only 'B' area can be programmed.

'50h' command can be omitted.

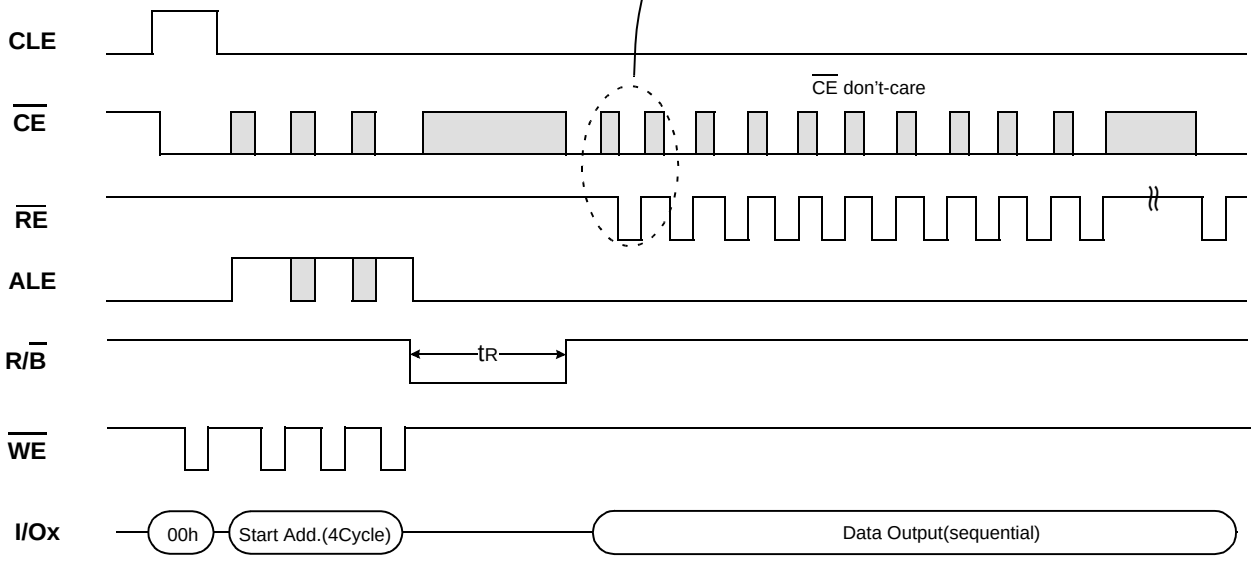
### System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 264word page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

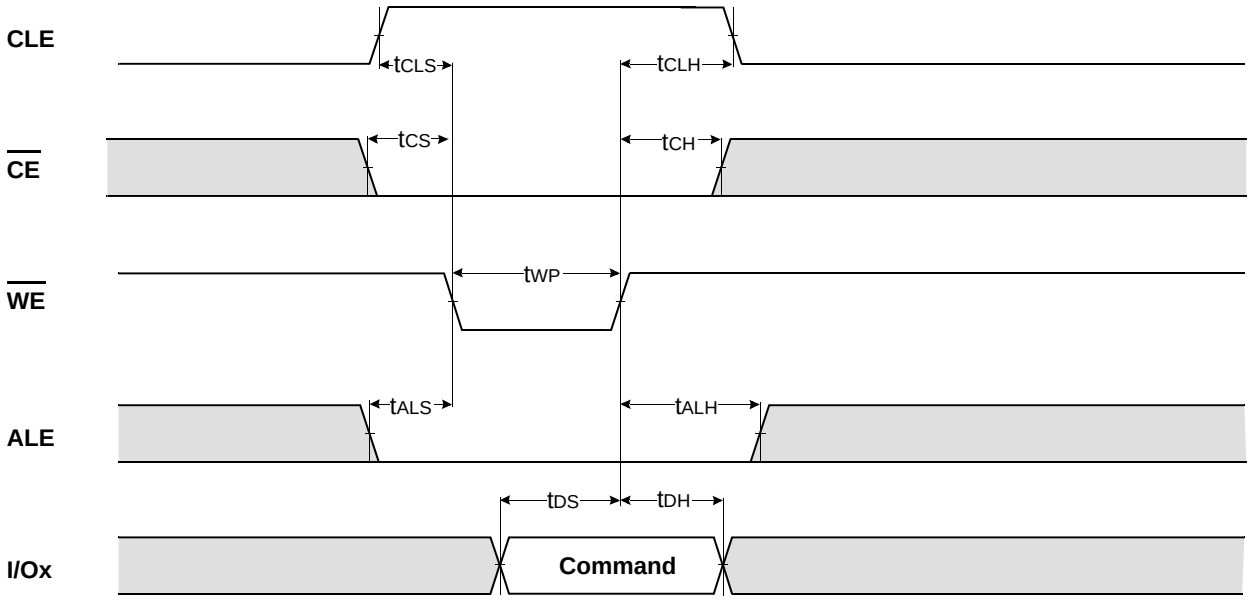
### Figure 4. Program Operation with $\overline{CE}$ don't-care.



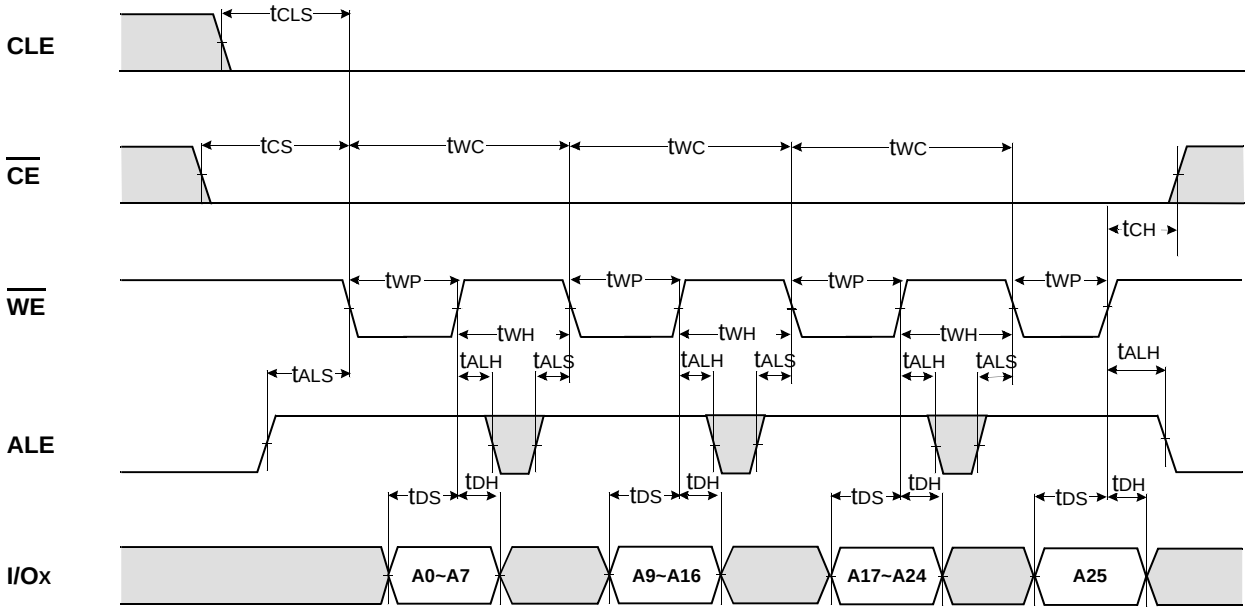

### Figure 5. Read Operation with $\overline{CE}$ don't-care.



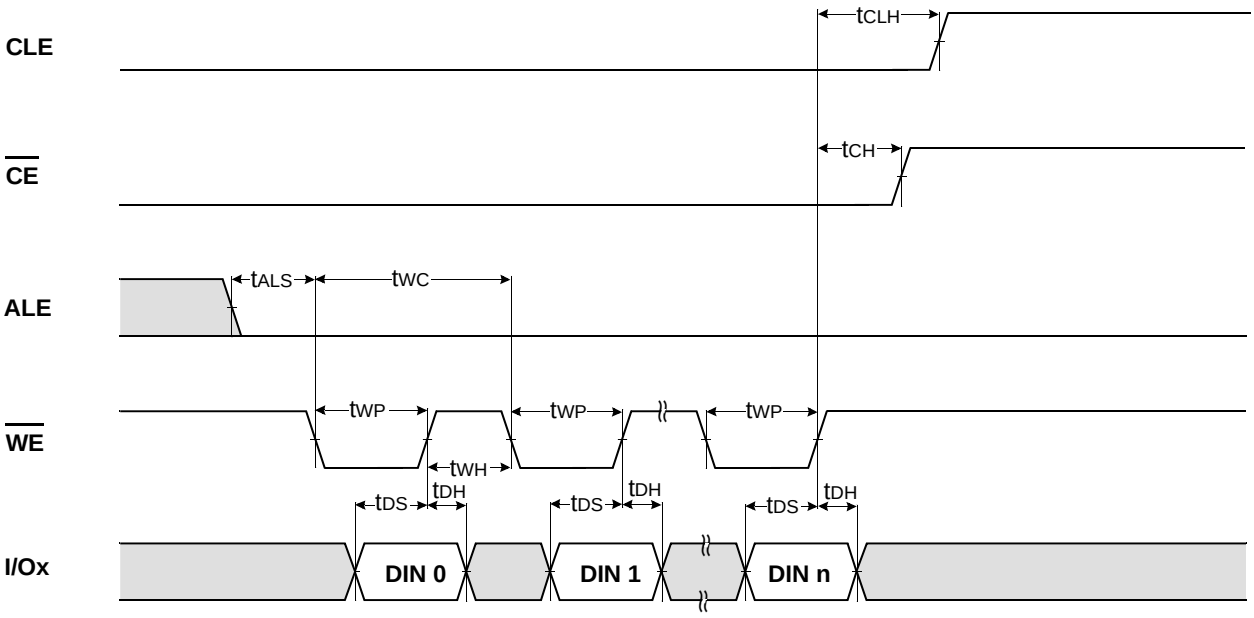
### Command Latch Cycle



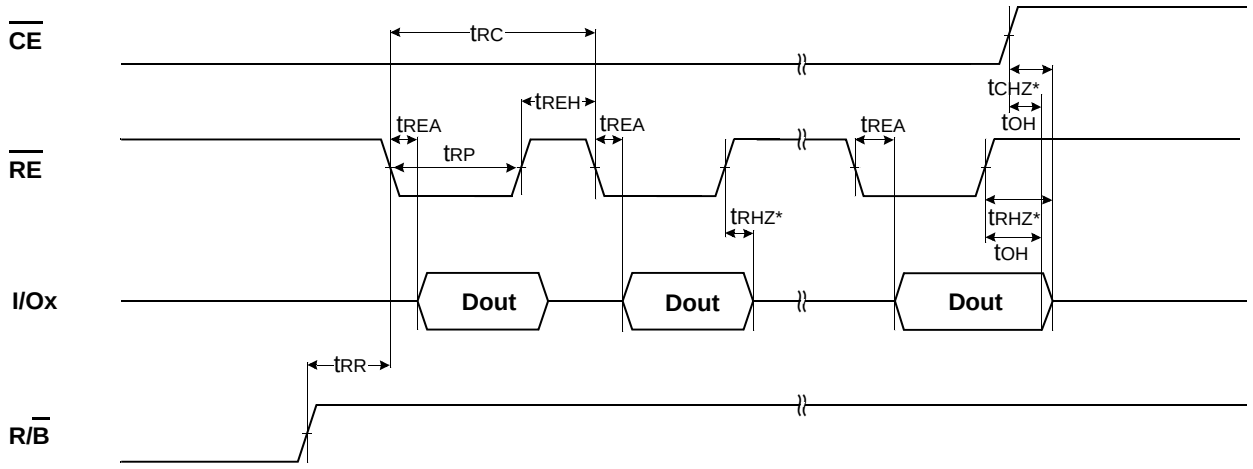

### Address Latch Cycle



## Input Data Latch Cycle




## Sequential Out Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

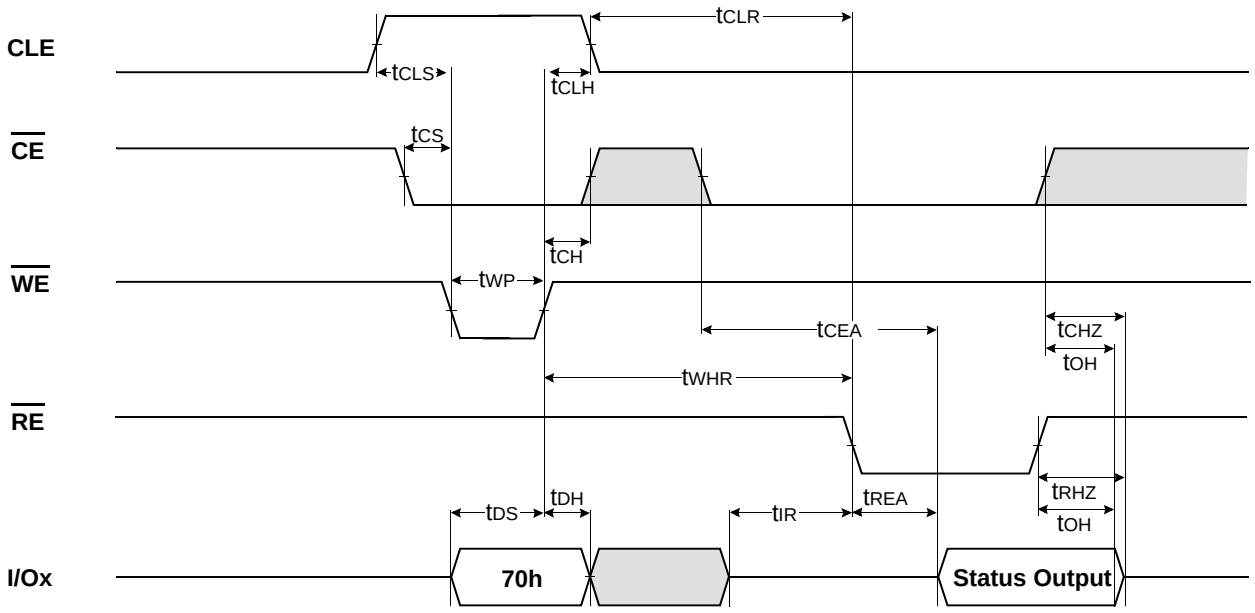



**NOTES :**

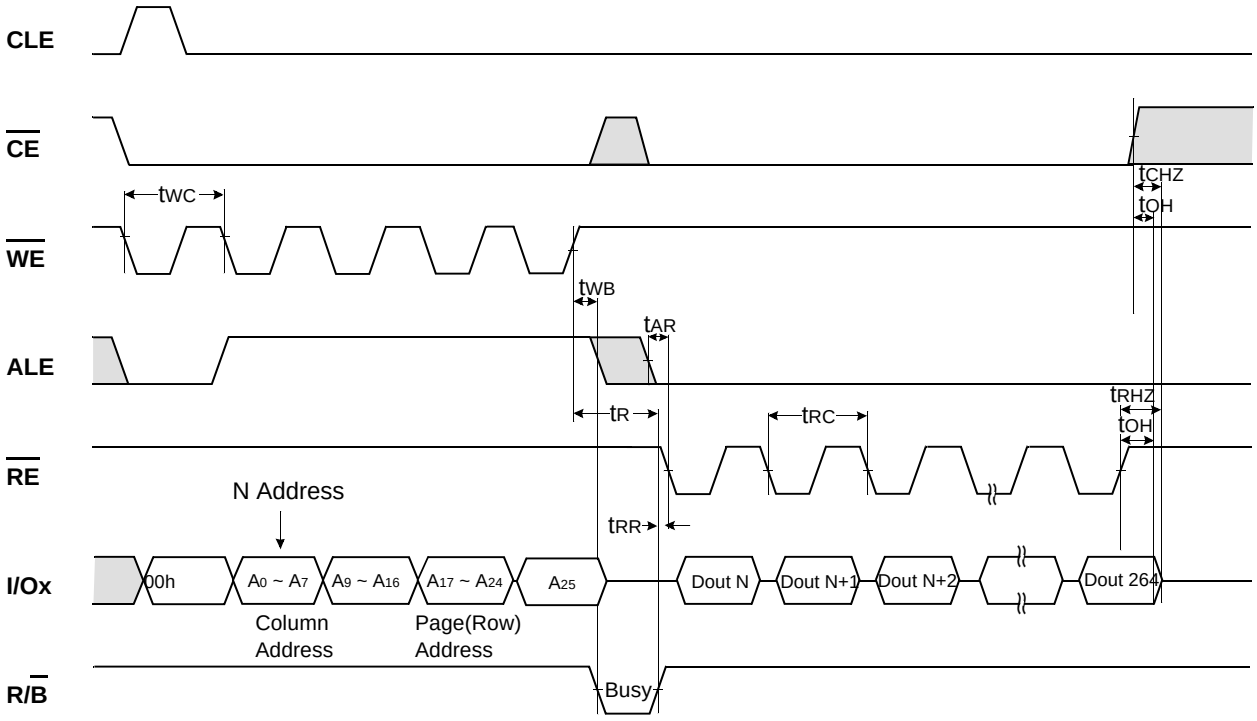
1.Transition is measured ±200mV from steady state voltage with load.

2.This parameter is sampled and not 100% tested.

### Status Read Cycle

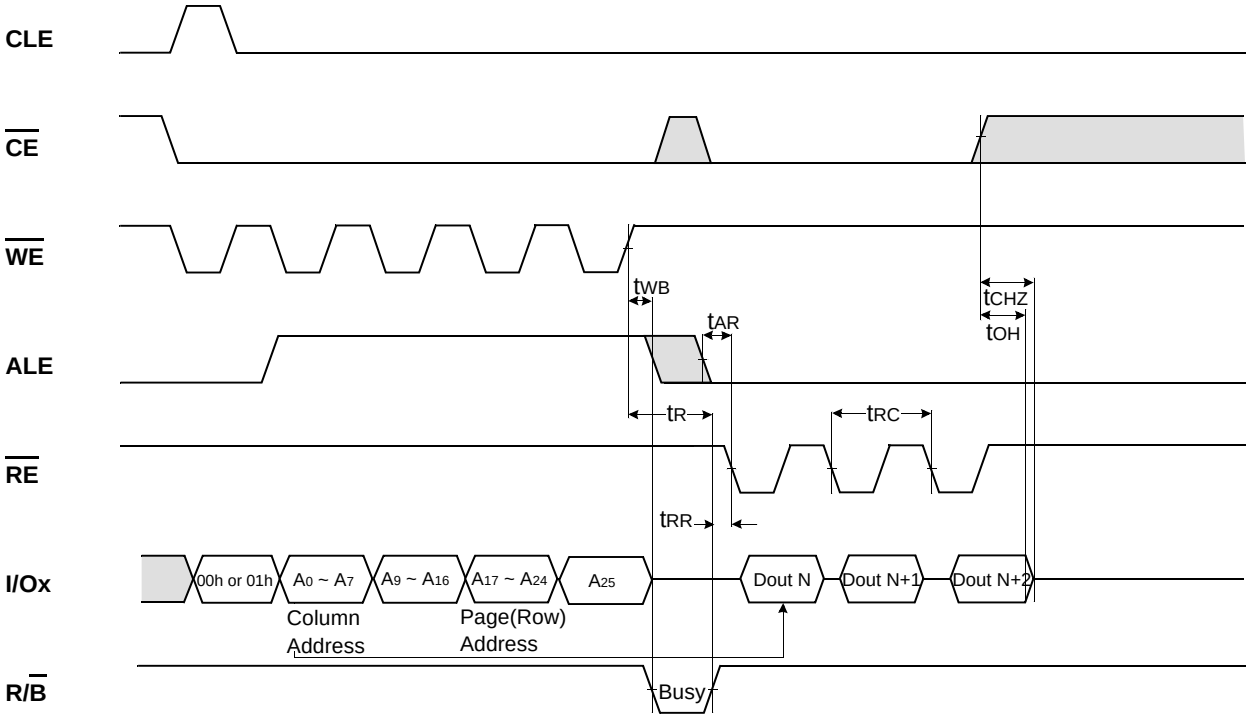



### READ1 OPERATION(READ ONE PAGE)

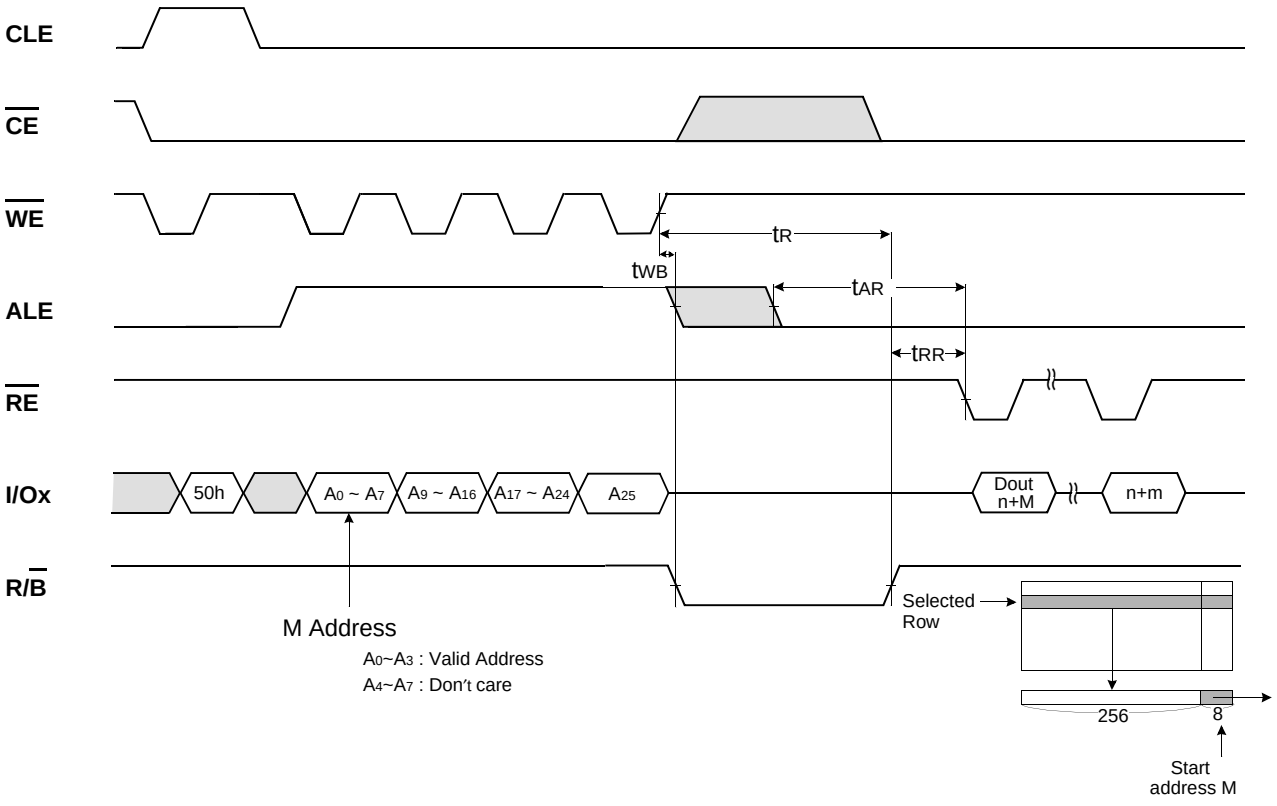



X16 device : m = 264 , Read CMD = 00h

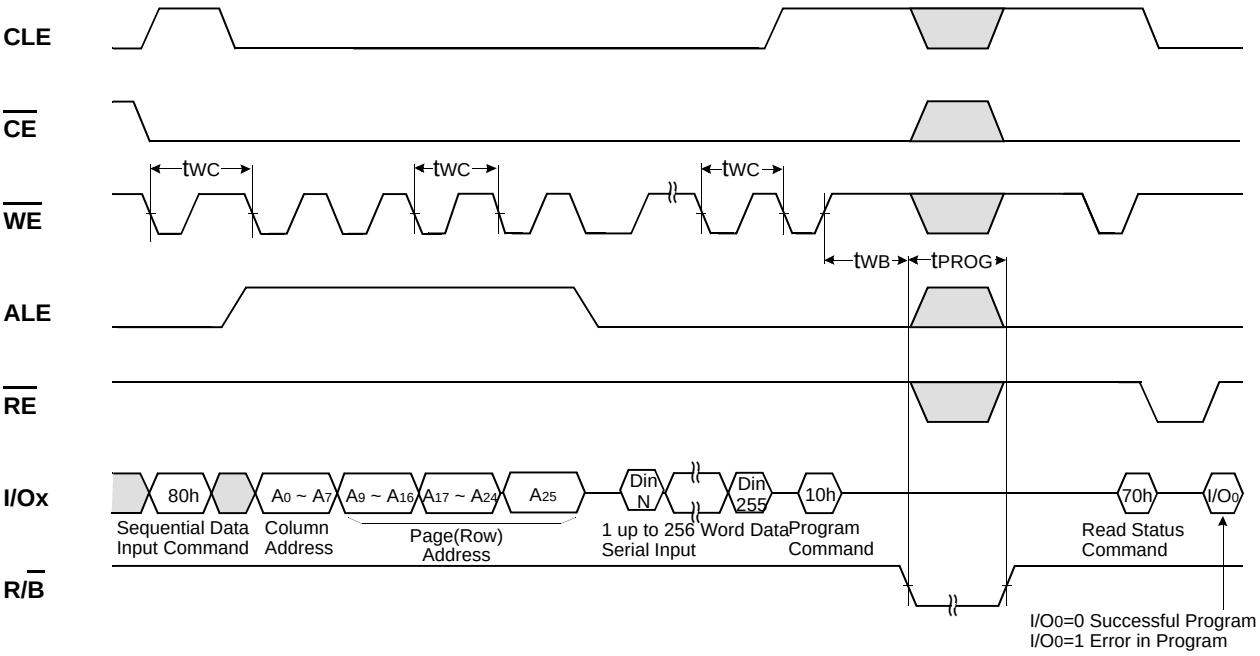
## READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)



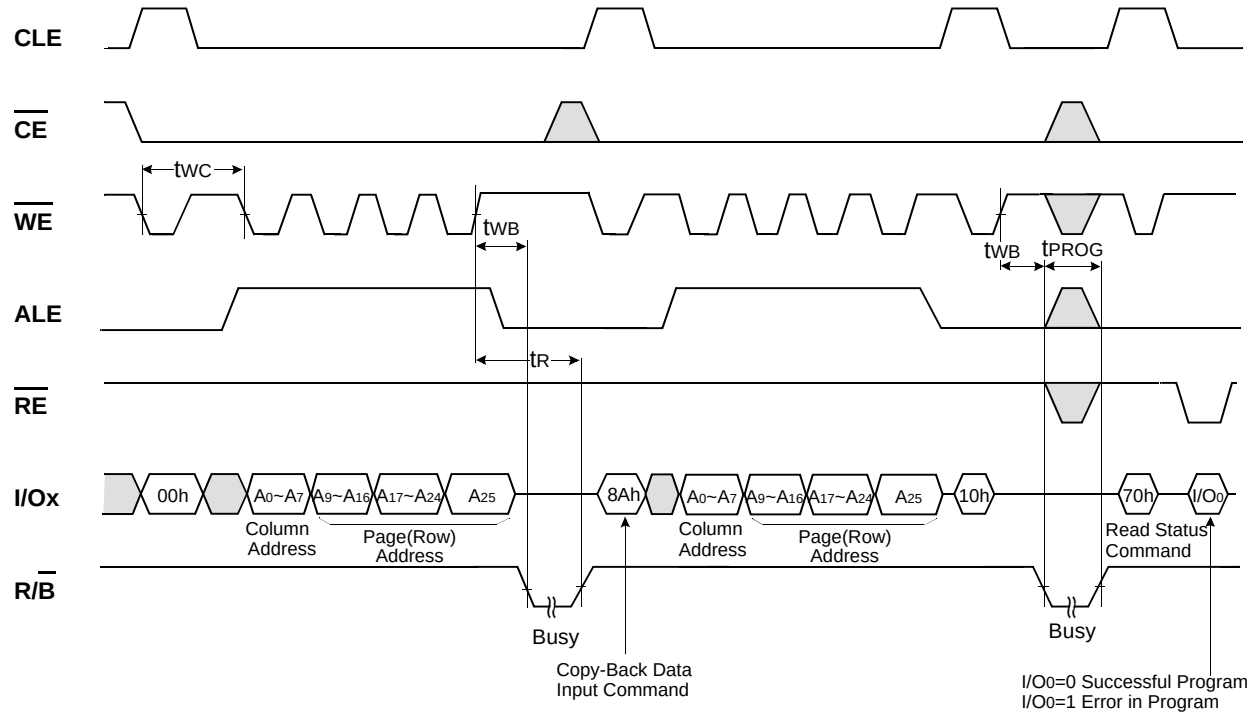

## READ2 OPERATION (READ ONE PAGE)



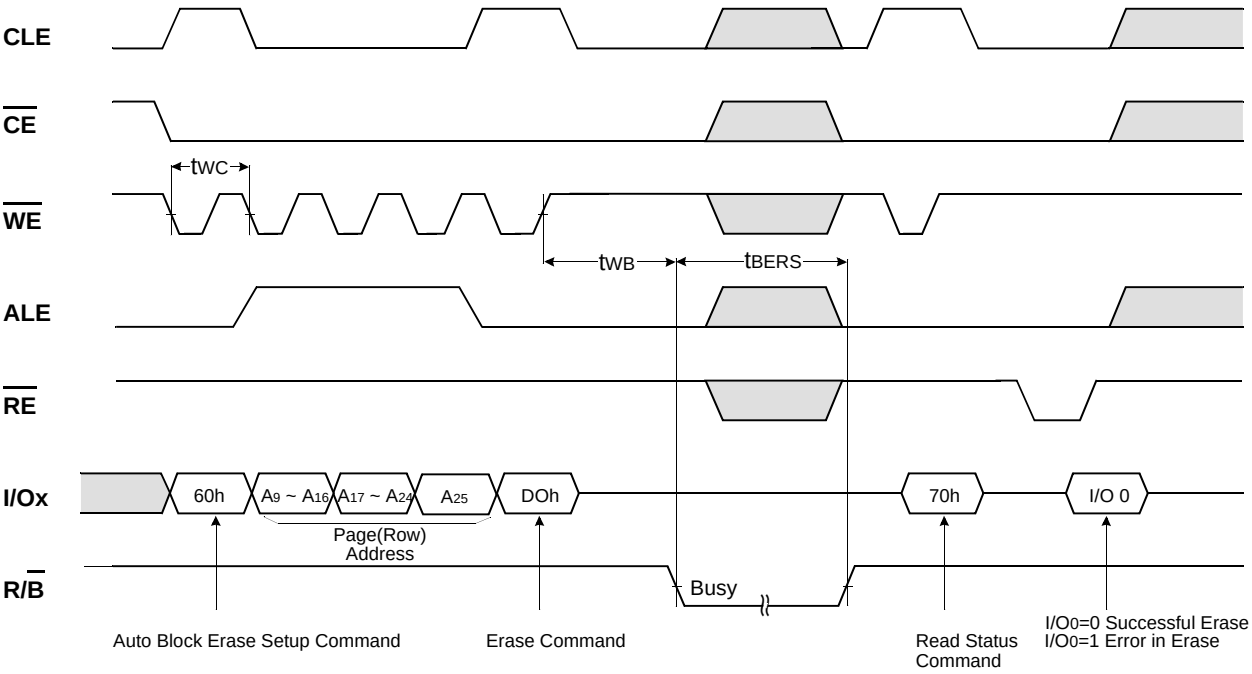
## PAGE PROGRAM OPERATION



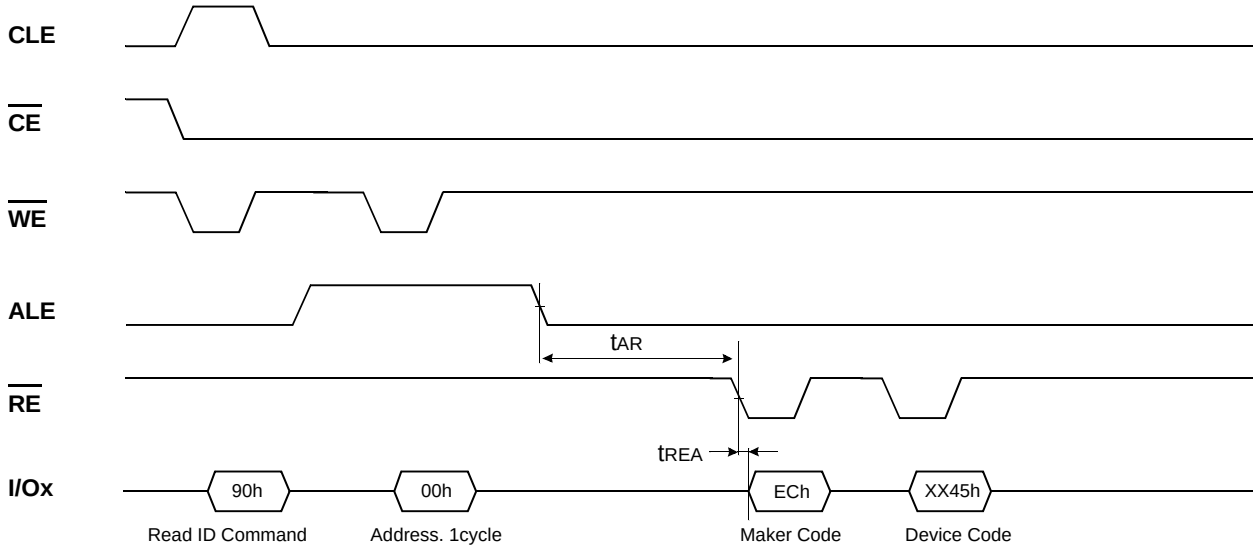

## COPY-BACK PROGRAM OPERATION



## BLOCK ERASE OPERATION (ERASE ONE BLOCK)




## MANUFACTURE & DEVICE ID READ OPERATION



## DEVICE OPERATION

### PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operations are available : random read, serial page read.

The random read mode is enabled when the page address is changed. The 264 words of data within the selected page are transferred to the data registers in less than 10μs($t_R$). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address[column 255 /263 depending on the state of GND input pin].

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 256~263 words may be selectively accessed by writing the Read2 command with GND input pin low. Addresses $A_0$~$A_2$ set the starting address of the spare area while addresses $A_3$~$A_7$ must be "L". The Read1 command is needed to move the pointer back to the main area. Figures 6, 7 show typical sequence and timings for each read operation.

**Figure 6. Read1 Operation**

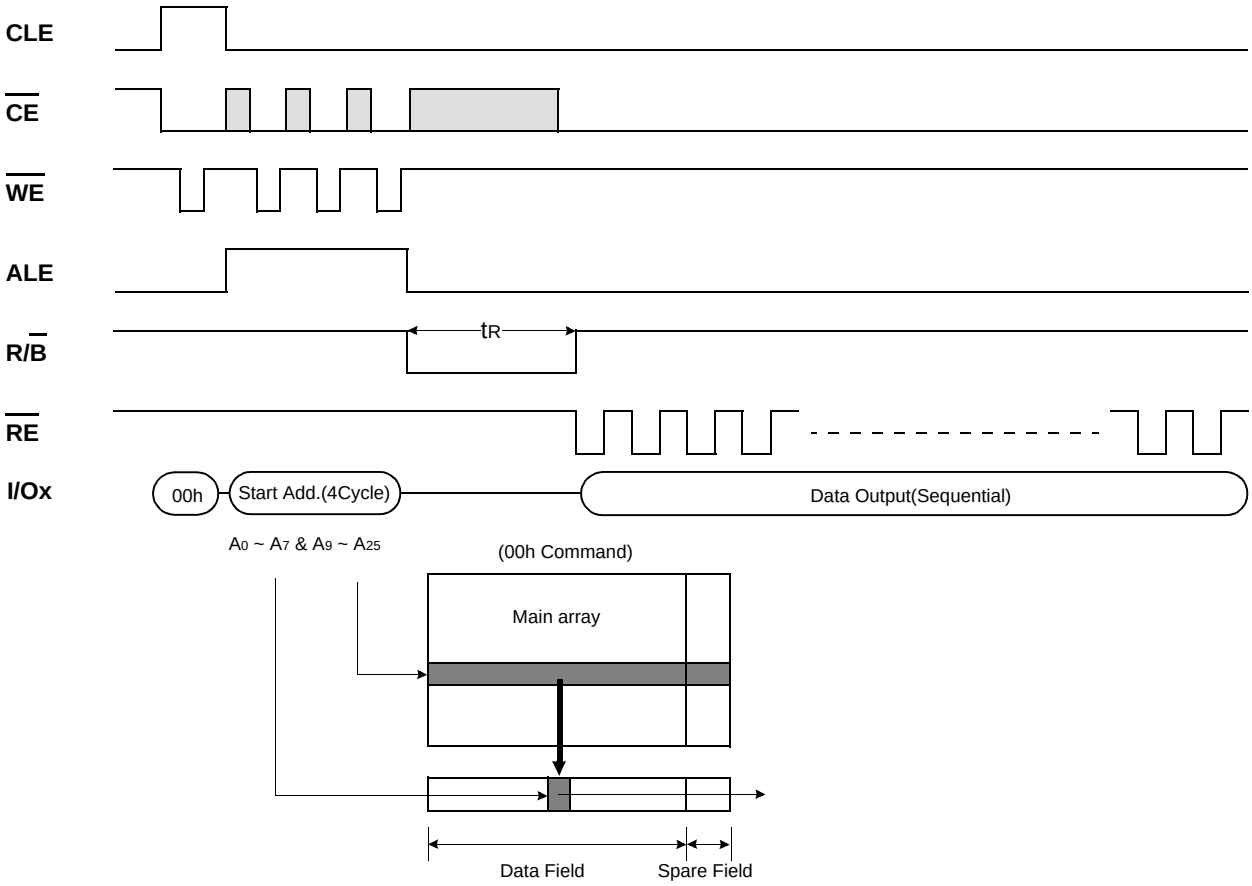
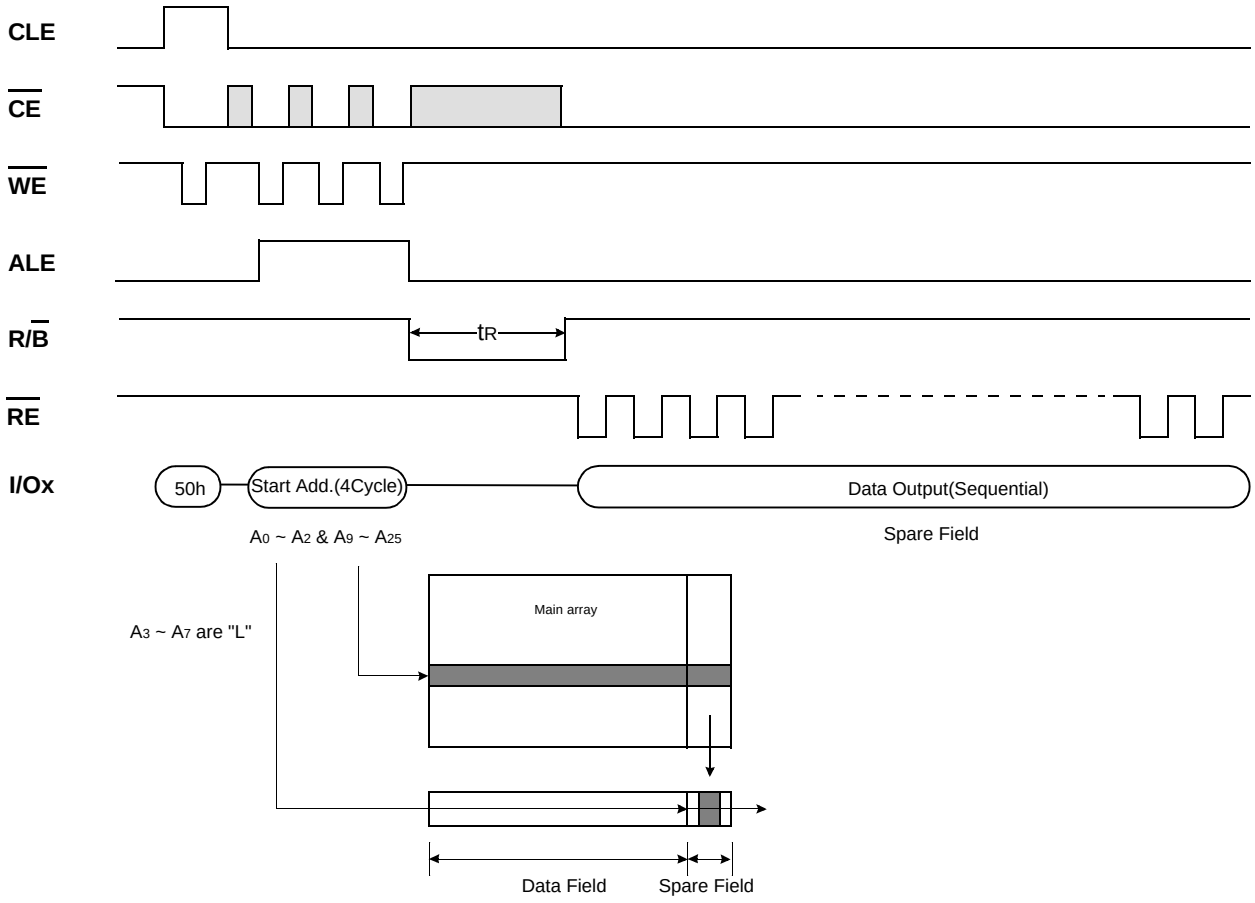


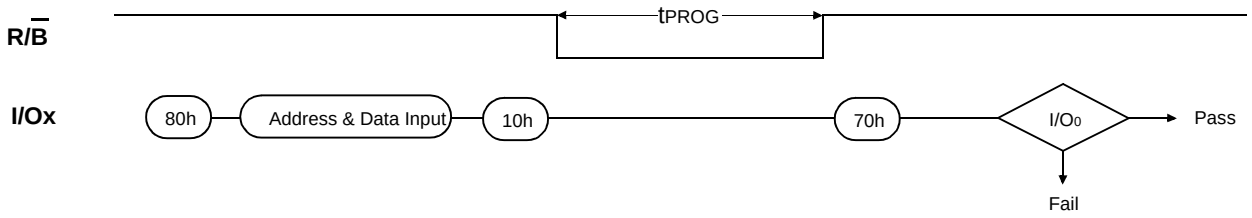
**Figure 7. Read2 Operation**



## PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a word or consecutive words up to 264, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 264 words of data may-be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The words other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

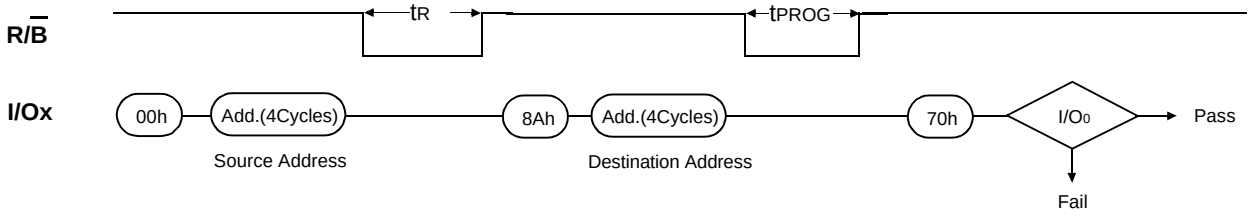
### Figure 8. Program Operation




## COPY-BACK PROGRAM

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the array to another page within the same array without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command with the address of the source page moves the whole 264words data into the internal buffer. As soon as the Flash returns to Ready state, copy-back programming command "8Ah" may be given with three address cycles of target page followed. The data stored in the internal buffer is then programmed directly into the memory cells of the destination page. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Since the memory array is internally partitioned into two different planes, copy-back program is allowed only within the same memory plane. Thus, A14 and A25, the plane address, of source and destination page address must be the same.

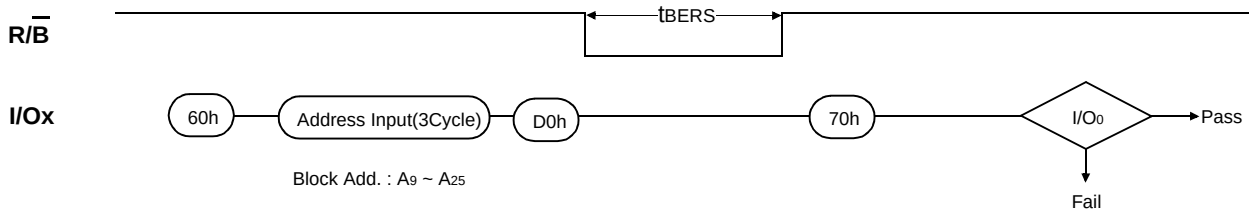
### Figure 9. Copy-Back Program Operation



## BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address $A_{14}$ to $A_{25}$ is valid while $A_9$ to $A_{13}$ is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 10 details the sequence.

### Figure 10. Block Erase Operation




## READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

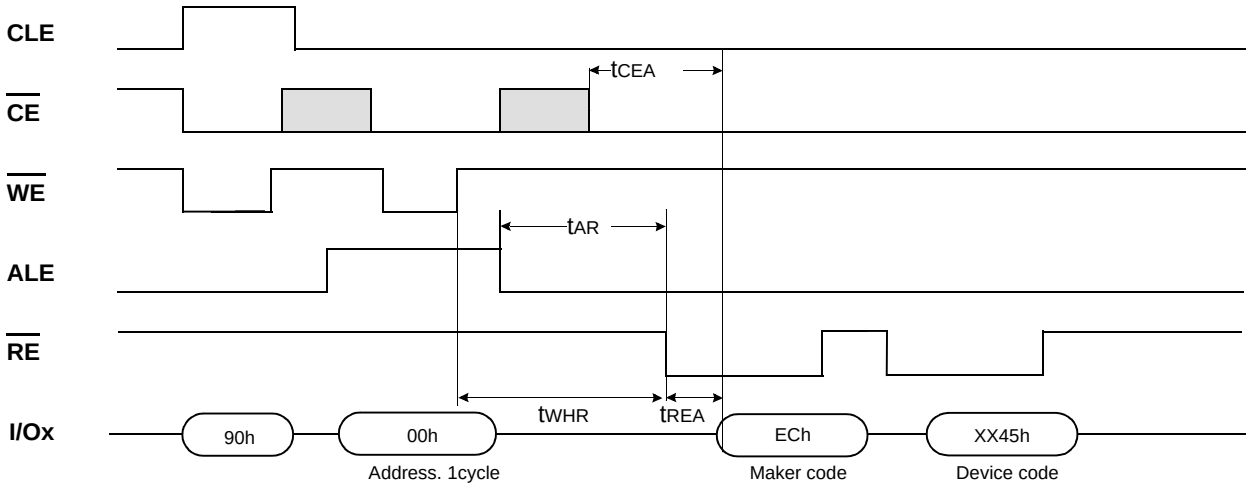
### Table 3. Read Status Register Definition

| I/O # | Status | Definition |
|---|---|---|
| I/O 0 | Program / Erase | "0" : Successful Program / Erase |
| | | "1" : Error in Program / Erase |
| I/O 1 | Reserved for Future Use | "0" |
| I/O 2 | | "0" |
| I/O 3 | | "0" |
| I/O 4 | | "0" |
| I/O 5 | | "0" |
| I/O 6 | Device Operation | "0" : Busy "1" : Ready |
| I/O 7 | Write Protect | "0" : Protected "1" : Not Protected |
| I/O 8~15 | Not use | Don't care |

## READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 11 shows the operation sequence.

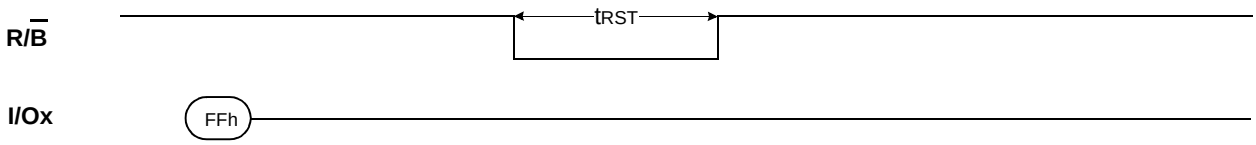
### Figure 11. Read ID Operation




## RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 4 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 12 below.

### Figure 12. RESET Operation

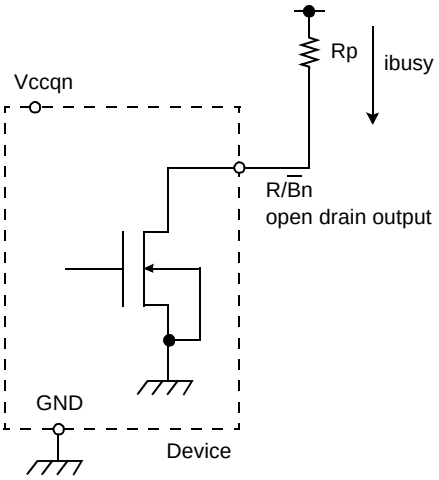


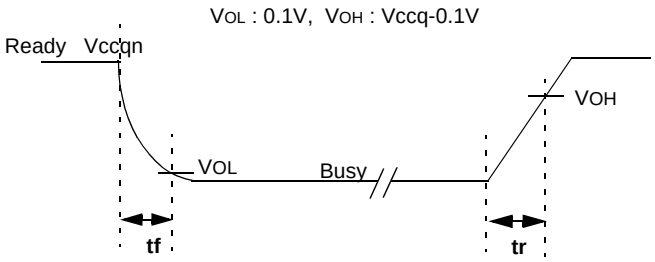

### Table4. Device Status

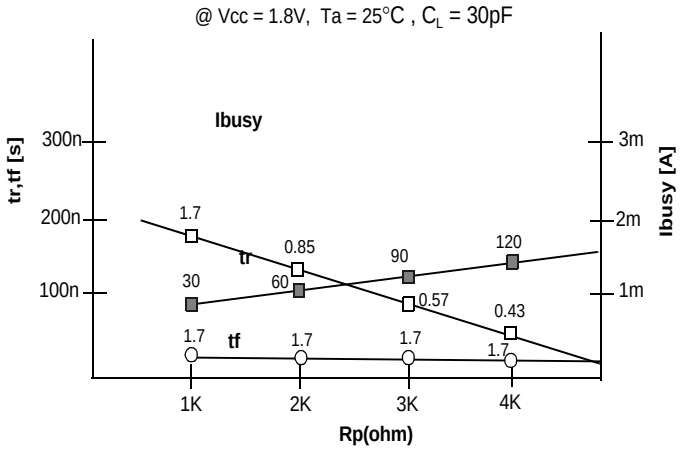
| | After Power-up | After Reset |
|---|---|---|
| Operation Mode | Read 1 | Waiting for next command |

## READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.




### Rp value guidance

$$Rp(min, 1.8V\ part) = \frac{Vccq(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.9V}{3mA + \Sigma I_L}$$

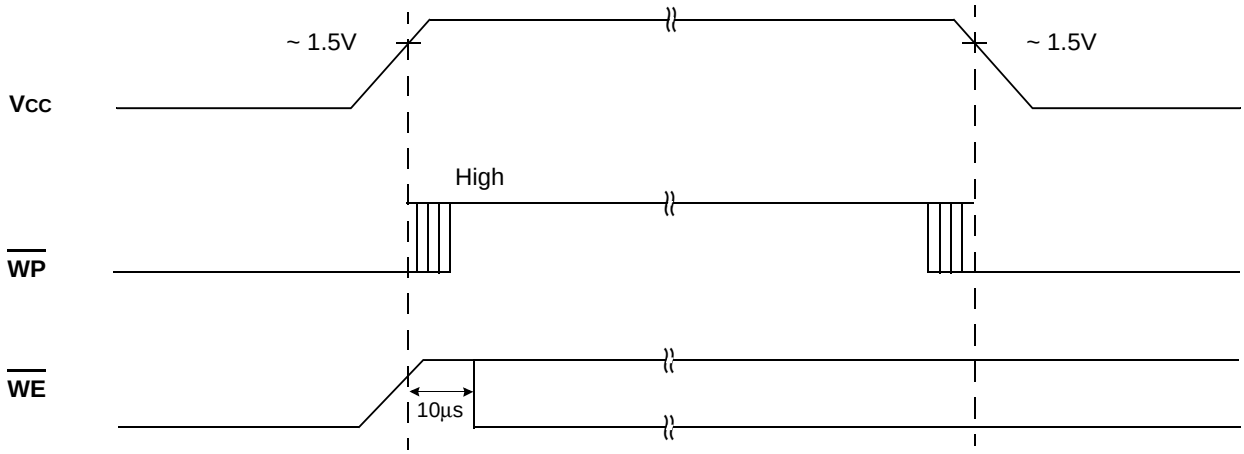
where $I_L$ is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

## Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at $V_{IL}$ during power-up and power-down and recovery time of minimum 10μs is required before internal circuit gets ready for any command sequences as shown in Figure 13. The two step command sequence for program/erase provides additional software protection.

### Figure 13. AC Waveforms for Power Transition

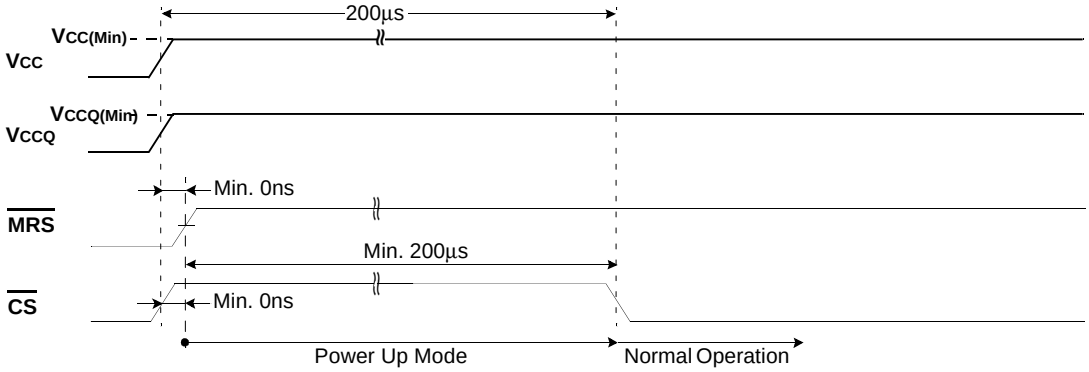


# 64Mb(4M x 16)
# Burst UtRAM B-Die

## POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minimum 200µs with $\overline{CS}$ and $\overline{MRS}$ high.

## TIMING WAVEFORM OF POWER UP




(POWER UP)

1. After Vcc reaches Vcc(Min.), wait 200µs with $\overline{CS}$ and $\overline{MRS}$ high. Then the device gets into the normal operation.

## FUNCTIONAL DESCRIPTION for ASYNCHRONOUS MODE(A15=0)

| $\overline{CS}$ | $\overline{MRS}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O0~7 | I/O8~15 | Mode | Power |
|---|---|---|---|---|---|---|---|---|---|
| H | H | X[1)] | X[1)] | X[1)] | X[1)] | High-Z | High-Z | Deselected | Standby |
| H | L | X[1)] | X[1)] | X[1)] | X[1)] | High-Z | High-Z | Deselected | DPD or PAR |
| L | H | H | H | X[1)] | X[1)] | High-Z | High-Z | Output Disabled | Active |
| L | H | X[1)] | X[1)] | H | H | High-Z | High-Z | Output Disabled | Active |
| L | H | L | H | L | H | Dout | High-Z | Lower Byte Read | Active |
| L | H | L | H | H | L | High-Z | Dout | Upper Byte Read | Active |
| L | H | L | H | L | L | Dout | Dout | Word Read | Active |
| L | H | H | L | L | H | Din | High-Z | Lower Byte Write | Active |
| L | H | H | L | H | L | High-Z | Din | Upper Byte Write | Active |
| L | H | H | L | L | L | Din | Din | Word Write | Active |
| L | L | H | L | X[1)] | X[1)] | High-Z | High-Z | Mode Register Set | Active |

1. X must be low or high state.
2. In asynchronous mode, Clock and $\overline{ADV}$ are ignored.

## FUNCTIONAL DESCRIPTION for SYNCHRONOUS MODE(A15=1)

| $\overline{CS}$ | $\overline{MRS}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O0~7 | I/O8~15 | CLK | $\overline{ADV}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | X[1)] | X[1)] | X[1)] | X[1)] | High-Z | High-Z | X[2)] | X[2)] | Deselected | Standby |
| H | L | X[1)] | X[1)] | X[1)] | X[1)] | High-Z | High-Z | X[2)] | X[2)] | Deselected | DPD or PAR |
| L | H | H | H | X[1)] | X[1)] | High-Z | High-Z | X[2)] | H | Output Disabled | Active |
| L | H | X[1)] | X[1)] | H | H | High-Z | High-Z | X[2)] | H | Output Disabled | Active |
| L | H | X[1)] | H | X[1)] | X[1)] | High-Z | High-Z | ⎍ | ⎍ | Read Add. Input Load | Active |
| L | H | L | H | L | H | Dout | High-Z | ⎍ | H | Lower Byte Read | Active |
| L | H | L | H | H | L | High-Z | Dout | ⎍ | H | Upper Byte Read | Active |
| L | H | L | H | L | L | Dout | Dout | ⎍ | H | Word Read | Active |
| L | H | H | L | L | H | Din | High-Z | X[2)] | L or ⎍ | Lower Byte Write | Active |
| L | H | H | L | H | L | High-Z | Din | X[2)] | L or ⎍ | Upper Byte Write | Active |
| L | H | H | L | L | L | Din | Din | X[2)] | L or ⎍ | Word Write | Active |
| L | L | H | L | X[1)] | X[1)] | High-Z | High-Z | X[2)] | L | Mode Register Set | Active |

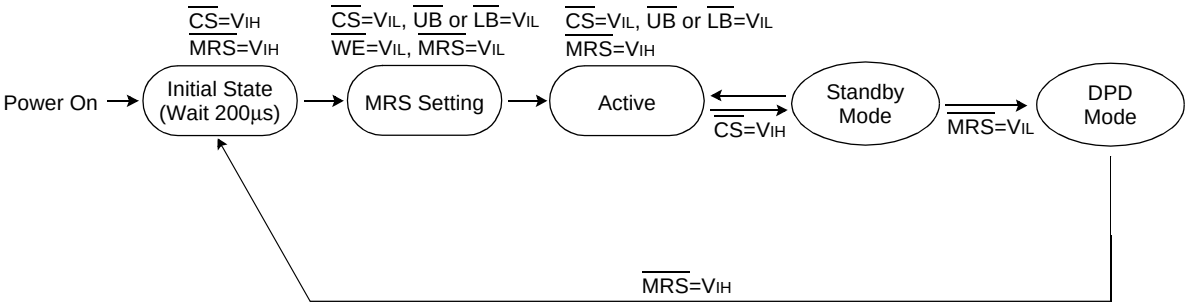
1. X must be low or high state.
2. X means "Don't care"(can be low, high or toggling).

## ABSOLUTE MAXIMUM RATINGS[1)]

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -0.2 to $V_{CC}$+0.3V | V |
| Power supply voltage relative to Vss | $V_{CC}$ | -0.2 to 3.6V | V |
| Output power supply voltage relative to Vss | $V_{CCQ}$ | -0.2 to 2.5V | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | $T_A$ | -25 to 85 | °C |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

## STANDBY MODE STATE MACHINES




NOTE : Default mode after power up is Asynchronous mode and DPD enable. But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up or after getting out of DPD mode.
If Synchronous operation is needed, set A15=1. For more detail, please refer to the Mode Register Set(See Page 35).
Once the device gets out of DPD mode, all the register settings are initialized into the default mode.

For entry to DPD mode, drive $\overline{MRS}$ pin into $V_{IL}$ for over 0.5us(suspend period) during standby mode after MRS setting has been completed(A4=0). To get out of the DPD mode, drive $\overline{MRS}$ pin into $V_{IH}$ with wake up sequence(See Page 50).

DPD mode can be selected through Mode Register Set(See Page 35).

## RECOMMENDED DC OPERATING CONDITIONS[1)]

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 2.7 | 2.9 | 3.1 | V |
| I/O power supply voltage | $V_{CCQ}$ | 1.7 | 1.85 | 2.0 | V |
| Ground | Vss | 0 | 0 | 0 | V |
| Input high voltage | $V_{IH}$ | 1.5 | - | $V_{DDQ}$+0.2[2)] | V |
| Input low voltage | $V_{IL}$ | -0.2[3)] | - | 0.4 | V |

1. $T_A$=-25 to 85°C, otherwise specified.
2. Overshoot: $V_{CC}$+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE[1)] (f=1MHz, $T_A$=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 8 | pF |
| Input/Output capacitance | $C_{IO}$ | $V_{IO}$=0V | - | 10 | pF |

1. Capacitance is sampled, not 100% tested.

## DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to $V_{CCQ}$ | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS}$=$V_{IH}$, $\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to $V_{CCQ}$ | -1 | - | 1 | µA |
| Average operating current | $I_{CC2}$ | Cycle time=Min, $I_{IO}$=0mA, 100% duty, $\overline{CS}$=$V_{IL}$, $\overline{MRS}$=$V_{IH}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$ | - | - | 45 | mA |
| Output low voltage | $V_{OL}$ | $I_{OL}$=0.1mA | - | - | 0.2 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-0.1mA | 1.4 | - | - | V |
| Standby Current(CMOS) | $I_{SB1}$ | $\overline{CS}$≥$V_{CCQ}$-0.2V, $\overline{MRS}$≥$V_{CCQ}$-0.2V, Other inputs=Vss to $V_{CCQ}$ | - | - | 180 | µA |
| Deep Power Down | $I_{SBD}$ | $\overline{MRS}$≤0.2V, $\overline{CS}$≥$V_{CCQ}$-0.2V, Other inputs=Vss to $V_{CCQ}$ | - | - | 25 | µA |

## DEVICE OPERATION

The device has several modes : Synchronous Burst Read mode, Asynchronous Write mode, Standby mode and Deep Power Down(DPD) mode.
Deep Power Down(DPD) mode is defined through Mode Register Set(MRS) option. Mode Register Set(MRS) option also defines Burst Length, Burst Type and First Access Latency Count at Synchronous Burst Read mode.
To set Mode Register, the system must drive CS, ADV, WE and MRS to $V_{IL}$ and drive OE to $V_{IH}$ during valid address. To get into the Standby mode, the system must drive CS to $V_{IH}$. To get into the Deep Power Down(DPD) mode, the system must drive CS to CMOS $V_{IH}$(VCC-0.2V) and MRS to CMOS $V_{IL}$(0.2V).

### Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of UtRAM. It programs Deep Power Down(DPD) mode, Burst Length, Burst Type, First Access Latency Count and various vendor specific options to make UtRAM useful for a variety of different applications. The default values of mode register are defined, therefore unless user specifies the specific modes, the device runs at default modes. If user wants to set modes other than default modes, user should write specific mode value on mode register after power up. The mode register is written by driving CS, ADV, WE and MRS to $V_{IL}$ and driving OE to $V_{IH}$ during valid address. The mode register is divided into various fields depending on the fields of functions. The Deep Power Down(DPD) field uses A4, Burst Length field uses A6~A7, Burst Type uses A8 and First Access Latency Count uses A9~A11. Refer to the Table below for detailed Mode Register Setting.

***Mode Register Setting according to field of function***

| Address | An~A16 | A15 | A14~A12 | A11~A9 | A8 | A7~A6 | A5 | A4 |
|---|---|---|---|---|---|---|---|---|
| **Function** | RFU | MS | RFU | Latency | BT | BL | RFU | DPD |

NOTE : RFU(Reserved for Future Use), BT(Burst Type), BL(Burst Length), DPD(Deep Power Down), MS(Mode Select)

| Mode Select | | First Access Latency Count | | | | Burst Type | | Burst Length | | |
|---|---|---|---|---|---|---|---|---|---|---|
| A15 | Async./Sync. | A11 | A10 | A9) | Latency | A8 | Type | A7 | A6 | Length |
| 0 | **Async. Mode** | 0 | 0 | 0 | Reserved | 0 | Linear | 0 | 0 | 4 |
| 1 | Sync. Mode | 0 | 0 | 1 | 3 | 1 | Interleave | 0 | 1 | 8 |
| | | 0 | 1 | 0 | 4 | | | 1 | 0 | 16 |
| | | 0 | 1 | 1 | 5 | | | 1 | 1 | Reserved |
| | | 1 | 0 | 0 | 6 | | | | | |
| | | 1 | 0 | 1 | Reserved | | | | | |
| | | 1 | 1 | 0 | Reserved | | | | | |
| | | 1 | 1 | 1 | Reserved | | | | | |

| Deep power Down | |
|---|---|
| A4 | DPD |
| 0 | **DPD Enable** |
| 1 | DPD Disable |

NOTE : Default mode(when user does not write any specific value to the mode register) is Async. mode and DPD enable.
Even though the device used to work in the sync. mode, once the device gets out of DPD mode, all the register settings are initialized into the default mode.But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up or after getting out of DPD mode.

## Asynchronous Read Operation

Asynchronous read operation starts when $\overline{CS}$, $\overline{OE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to $V_{IL}$ under the valid address.($\overline{MRS}$ and $\overline{WE}$ should be driven to $V_{IH}$ during asynchronous read operation)

## Asynchronous Write Operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are driven to $V_{IL}$ under the valid address.($\overline{MRS}$ and $\overline{OE}$ should be driven to $V_{IH}$ during write operation.)

## Asynchronous Write Operation in Synchronous Mode

A write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ & $\overline{LB}$ are driven to $V_{IL}$ under the valid address. Clock input does not have any affect to the write operation.(MRS and OE should be driven to $V_{IH}$ during write operation. ADV can be toggling for address latch or can be driven to $V_{IL}$)

## Synchronous Burst Read Operation

The device supports Linear Synchronous Burst Read mode and Interleave Synchronous Burst Read mode.
For the optimized Burst Mode to each system, the system should determine how many clock cycles are desirable for the initial word of each burst access(First Access Latency Count), how many words the device outputs at an access(Burst Length) and which type of burst operation(Burst Type : Linear or Interleave) is desired.(See Table "Mode Register Set")

### Clock(CLK)

The clock input is used as the reference for synchronous burst read operation of UtRAM. Synchronous burst read operation is synchronized to the rising edge of the clock. The clock transitions must swing between $V_{IL}$ and $V_{IH}$.

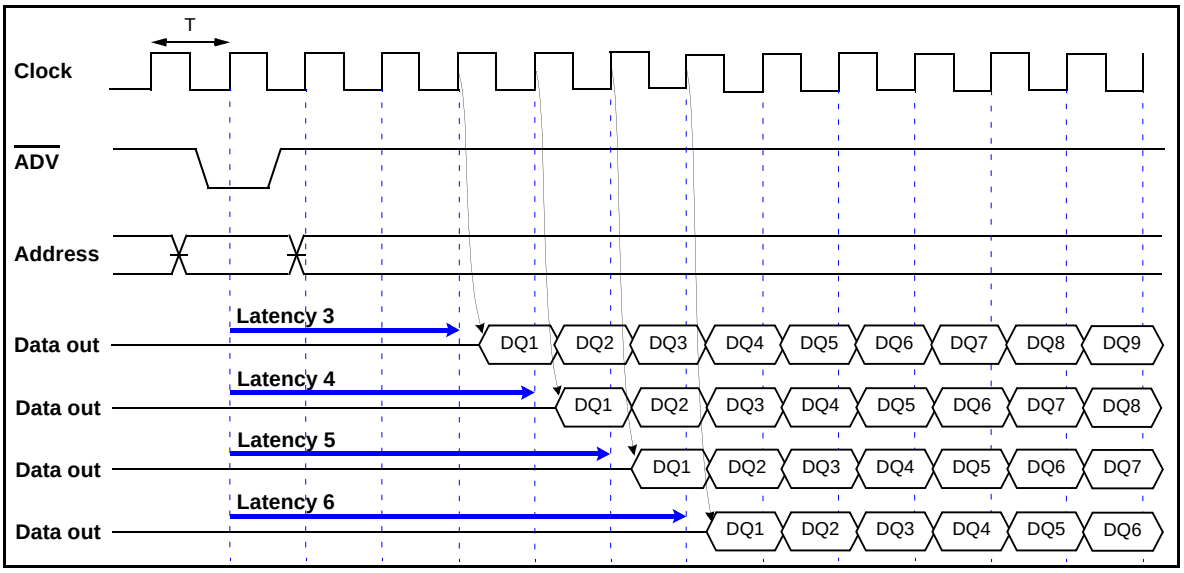
### First Access Latency Count

The First Access Latency Count configuration tells the device how many clocks must elapse from $\overline{ADV}$ de-assertion($V_{IH}$) before the first data word should be driven onto its data pins. This value depends on the input clock frequency.
The supported Latency Count is as follows.

***Latency Count support : 3, 4, 5, 6***

| Clock Frequency | Upto 54MHz | Upto 40MHz |
|---|---|---|
| Latency Count | **4**, 5, 6 | **3**, 4, 5, 6 |

***First Access Latency Configuration***




NOTE : Other First Access Latency Configuration settings are reserved.
Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse

### Burst Sequence

| Start Address | Burst Address Sequence | | | | | |
|---|---|---|---|---|---|---|
| | 4 word Burst | | 8 word Burst | | 16 word Burst | |
| | Linear | Interleave | Linear | Interleave | Linear | Interleave |
| **0** | 0-1-2-3 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4...14-15 | 0-1-2-3-4...14-15 |
| **1** | 1-2-3-0 | 1-0-3-2 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 | 1-2-3-4...14-15-0 | 1-0-3-2-5...15-14 |
| **2** | 2-3-0-1 | 2-3-0-1 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 | 2-3-4...14-15-0-1 | 2-3-0-1-6...12-13 |
| **3** | 3-0-1-2 | 3-2-1-0 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 | 3-4-5...15-0-1-2 | 3-2-1-0-7...13-12 |
| **4** | | | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 | 4-5-6...15-0-1-2-3 | 4-5-6-7-0...10-11 |
| **5** | | | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 | 5-6...15-0-1-2-3-4 | 5-4-7-6-1...11-10 |
| **6** | | | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 | 6-7...15-0-1-2-3-4-5 | 6-7-4-5-2...8-9 |
| **7** | | | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 | 7-8...15-0-1...5-6 | 7-6-5-4-3...9-8 |
| **~** | | | | | ~ | ~ |
| **14** | | | | | 14-15-0-1...12-13 | 14-15-12-13-10...0-1 |
| **15** | | | | | 15-0-1...12-13-14 | 15-14-13-12-11...1-0 |

### Burst Stop

Burst stop is used when the system wants to stop burst operation on special purpose. If driving $\overline{CS}$ to $V_{IH}$ during burst read operation, then burst operation will be stopped. During burst read operation, the new burst operation by ADV can not be issued. The new burst operation can be issued only after the previous burst operation is finished.

## AC OPERATING CONDITIONS

### TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to $V_{CCQ}$-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x $V_{CCQ}$
Output load: $C_L$=50pF

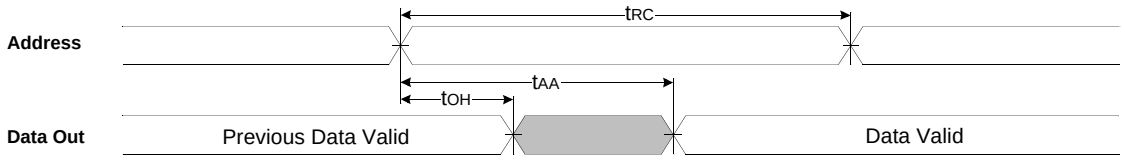
## ASYNCHRONOUS AC CHARACTERISTICS ($V_{CC}$=2.7~3.1V, $V_{CCQ}$=1.7~2.0V, $T_A$=-25 to 85°C)

| Parameter List | | Symbol | Speed | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Async. Read | Read Cycle Time | $t_{RC}$ | 85 | - | ns |
| | Address Access Time | $t_{AA}$ | - | 85 | ns |
| | Chip Select to Output | $t_{CO}$ | - | 85 | ns |
| | Output Enable to Valid Output | $t_{OE}$ | - | 40 | ns |
| | $\overline{UB}$, $\overline{LB}$ Access Time | $t_{BA}$ | - | 40 | ns |
| | Chip Select to Low-Z Output | $t_{LZ}$ | 10 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output | $t_{BLZ}$ | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | ns |
| | Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 25 | ns |
| | $\overline{UB}$, $\overline{LB}$ Disable to High-Z Output | $t_{BHZ}$ | 0 | 25 | ns |
| | Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 25 | ns |
| | Output Hold | $t_{OH}$ | 10 | - | ns |
| Async. Write | Write Cycle Time | $t_{WC}$ | 85 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 70 | - | ns |
| | Address Set-up Time to Beginning of Write | $t_{AS}$ | 0 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 70 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Write | $t_{BW}$ | 70 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 60[1)] | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | ns |
| | Data to Write Time Overlap | $t_{DW}$ | 35 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | ns |
| MRS | $\overline{MRS}$ Enable to Register Write Start | $t_{MW}$ | 0 | 500 | ns |
| | Register Write Recovery Time | $t_{RWR}$ | 5 | - | ns |
| | End of Write to $\overline{MRS}$ Disable | $t_{WU}$ | 0 | - | ns |

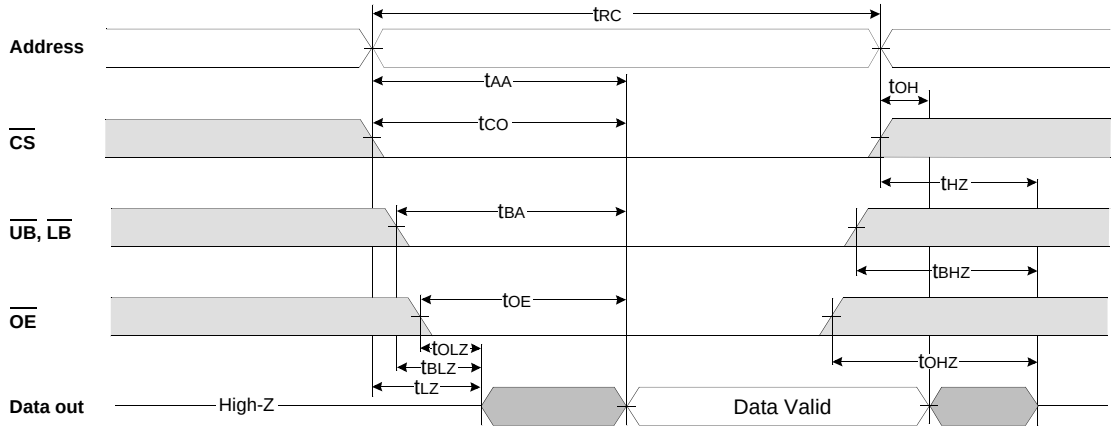
1. $t_{WP}$(min)=85ns for continuous write operation over 50 times.

## ASYNCHRONOUS READ TIMING WAVEFORM

### TIMING WAVEFORM OF ASYNCHRONOUS READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=$V_{IL}$, $\overline{MRS}$=$\overline{WE}$=$V_{IH}$, $\overline{UB}$ or $\overline{LB}$=$V_{IL}$)




### TIMING WAVEFORM OF ASYNCHRONOUS READ CYCLE(2)($\overline{MRS}$=$\overline{WE}$=$V_{IH}$)

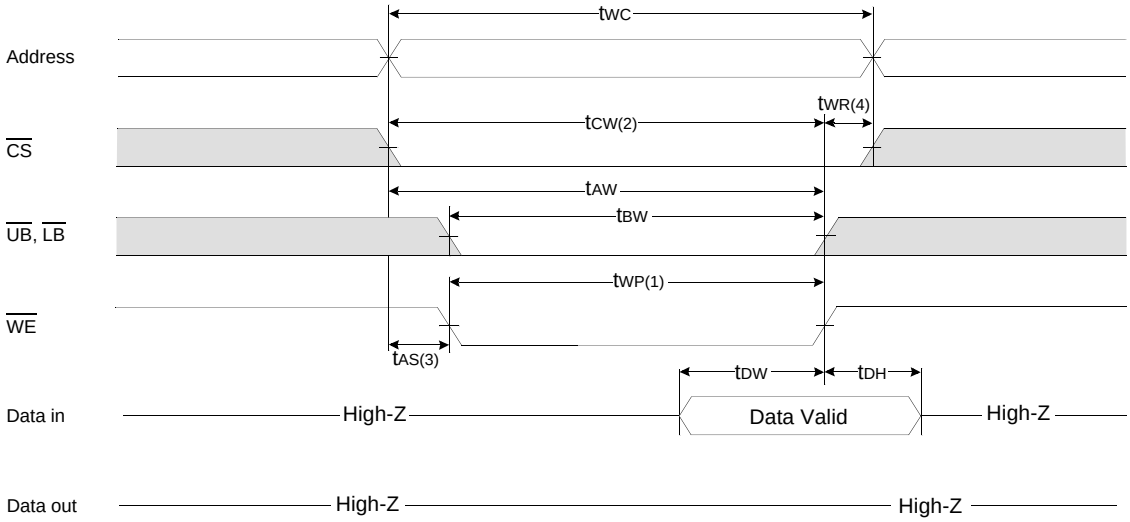



(ASYNCHRONOUS READ CYCLE)

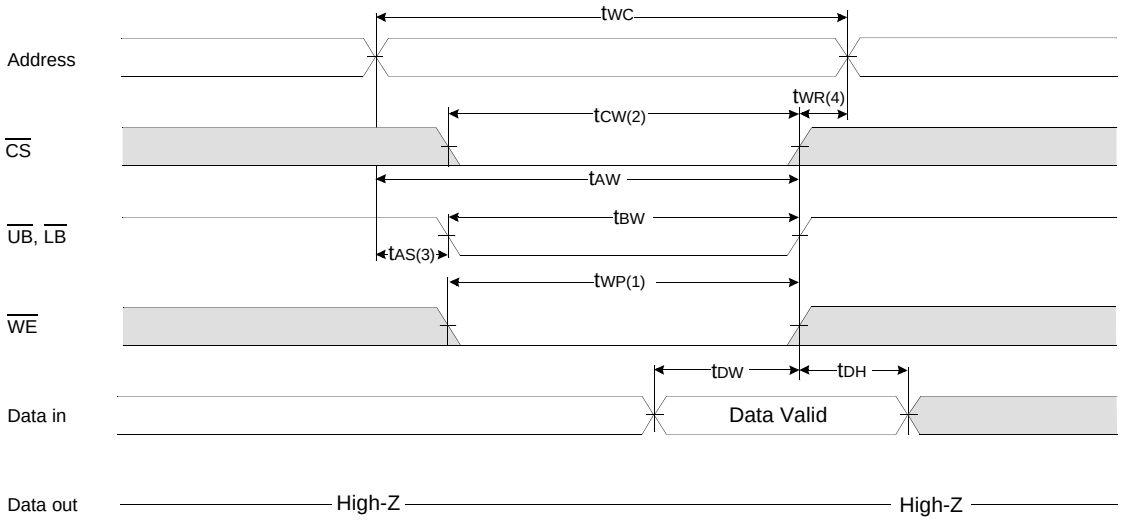
1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.
3. $t_{OE}$(max) is met only when $\overline{OE}$ becomes enabled after $t_{AA}$(max).
4. If invalid address signals shorter than min. $t_{RC}$ are continuously repeated for over 4us, the device needs a normal read timing($t_{RC}$) or needs to sustain standby state for min. $t_{RC}$ at least once in every 4us.
5. In asynchronous mode, Clock and ADV are ignored.

## ASYNCHRONOUS WRITE TIMING WAVEFORM

### TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{WE}$ Controlled)




### TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{UB}$ & $\overline{LB}$ Controlled)




(WRITE CYCLE)

1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS}$ going low to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. In asynchronous mode, Clock and $\overline{ADV}$ are ignored.

## AC OPERATING CONDITIONS

### TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to $V_{CCQ}$-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x $V_{CCQ}$
Output load: $C_L$=50pF

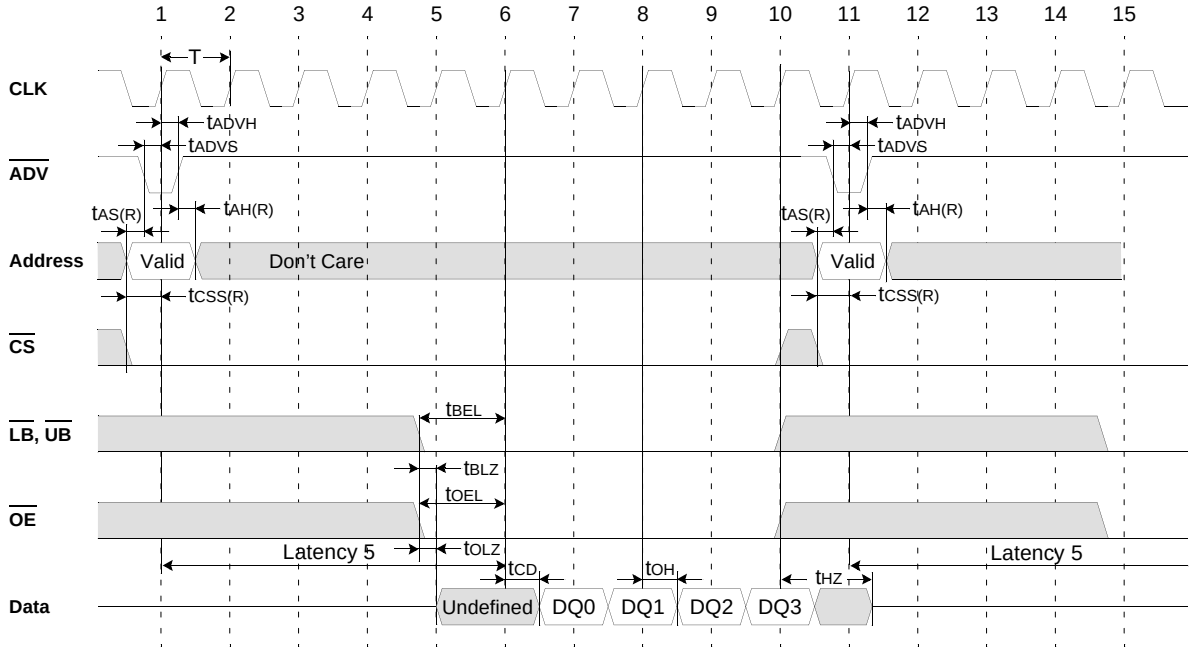
### SYNCHRONOUS AC CHARACTERISTICS ($V_{CC}$=2.7~3.1V, $V_{CCQ}$=1.7~2.0V, $T_A$=-25 to 85°C, Maximum Main Clock Frequency=54MHz)

| Parameter List | | Symbol | Speed | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Sync. Burst Read | Clock Cycle Time | T | 18.5 | 200 | ns |
| | Address Set-up Time to $\overline{ADV}$ Falling | $t_{AS(R)}$ | 0 | - | ns |
| | Address Hold Time from $\overline{ADV}$ Rising | $t_{AH(R)}$ | 7 | - | ns |
| | $\overline{ADV}$ Setup Time | $t_{ADVS}$ | 7 | - | ns |
| | $\overline{ADV}$ Hold Time | $t_{ADVH}$ | 7 | - | ns |
| | $\overline{CS}$ Setup Time to Clock Rising | $t_{CSS(R)}$ | 7 | - | ns |
| | $\overline{CS}$ Low Hold Time from Clock | $t_{CSLH}$ | 10 | - | ns |
| | $\overline{CS}$ High Pulse Width | $t_{CSHP}$ | 5 | - | ns |
| | $\overline{ADV}$ High Pulse Width | $t_{ADHP}$ | 5 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Latency | $t_{BEL}$ | 1 | - | Clock |
| | Output Enable to End of Latency | $t_{OEL}$ | 1 | - | Clock |
| | $\overline{UB}$, $\overline{LB}$ Valid to Low-Z Output | $t_{BLZ}$ | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | ns |
| | Latency Clock Rising Edge to Data Output | $t_{CD}$ | - | 12 | ns |
| | Output Hold | $t_{OH}$ | 3 | - | ns |
| | Output High-Z | $t_{HZ}$ | - | 10 | ns |
| Async. Write | Write Cycle Time | $t_{WC}$[2] | 85 | - | ns |
| | Address Set-up Time to $\overline{ADV}$ Falling | $t_{AS(W)}$ | 0 | - | ns |
| | Address Hold Time from $\overline{ADV}$ Rising | $t_{AH(W)}$ | 7 | - | ns |
| | $\overline{CS}$ Setup Time to $\overline{ADV}$ Rising | $t_{CSS(W)}$ | 10 | - | ns |
| | Address Set-up Time to Beginning of Write | $t_{AS}$ | 0 | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | ns |
| | Burst Read End Clock to Next ADV Falling | $t_{BEWA}$ | 3 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 70 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 70 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Write | $t_{BW}$ | 70 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 60[1] | - | ns |
| | $\overline{WE}$ High Pulse Width | $t_{WHP}$ | 5 ns | Latency-1 clock | - |
| | Data to Write Time Overlap | $t_{DW}$ | 35 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | ns |
| MRS | $\overline{MRS}$ Enable to Register Write Start | $t_{MW}$ | 0 | 500 | ns |
| | Register Write Recovery Time | $t_{RWR}$ | 5 | - | ns |
| | End of Write to $\overline{MRS}$ Disable | $t_{WU}$ | 0 | - | ns |

1. $t_{WP}$(min)=85ns for continuous write operation over 50 times.
2. In ADDRESS LATCH TYPE WRITE TIMING, $t_{WC}$ is same as $t_{AW}$.

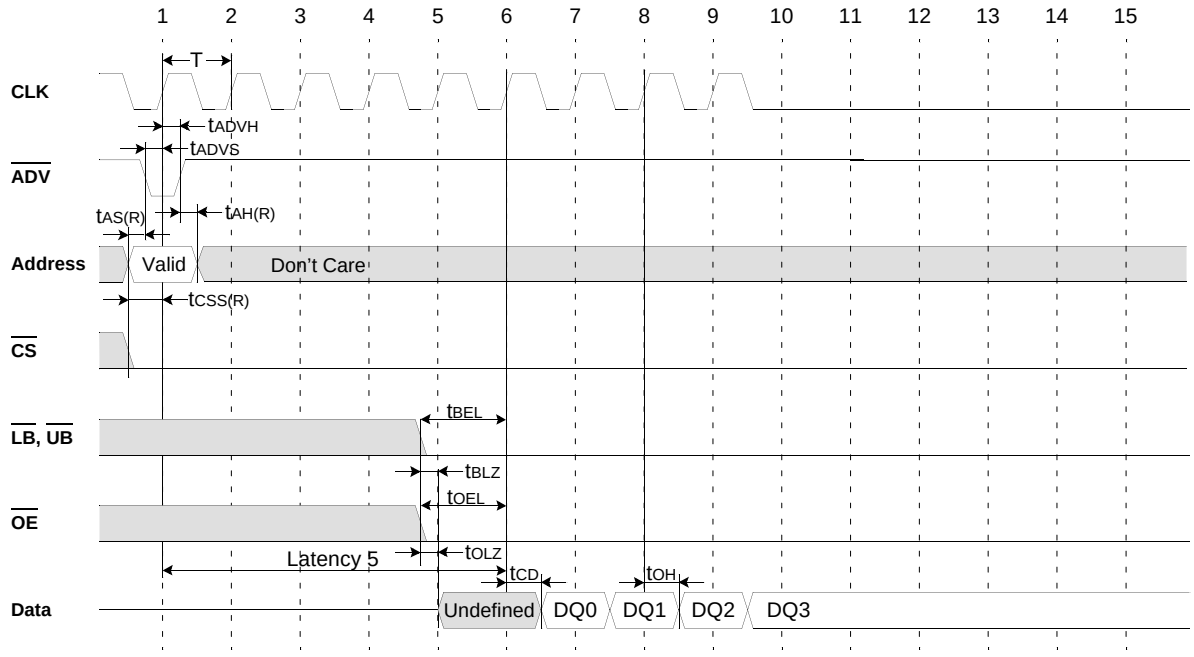
## SYNCHRONOUS BURST READ TIMING WAVEFORM

### TIMING WAVEFORM OF BURST READ CYCLE(1) [Latency=5, Burst Length=4] ($\overline{WE}$=$V_{IH}$, $\overline{MRS}$=$V_{IH}$)




(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The new burst operation can be issued only after the previous burst operation is finished.

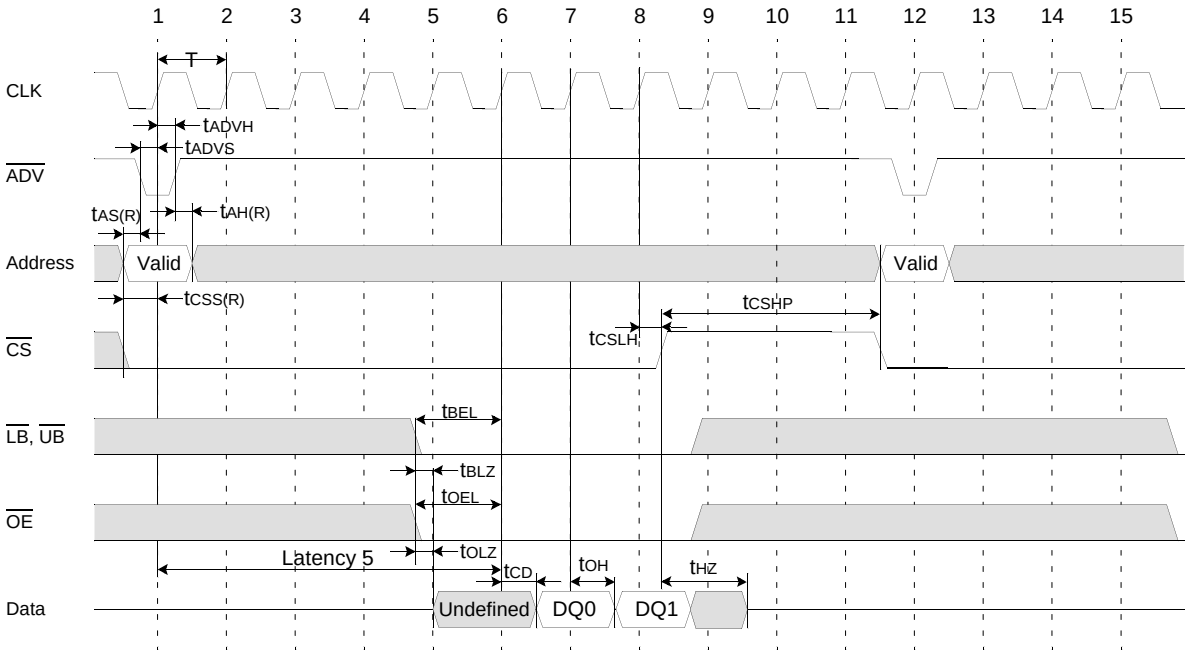
### TIMING WAVEFORM OF BURST READ CYCLE(2) [Latency=5, Burst Length=4] ($\overline{WE}$=$V_{IH}$, $\overline{MRS}$=$V_{IH}$)




(SYNCHRONOUS BURST READ CYCLE)
1.Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.

## BURST STOP TIMING WAVEFORM

**TIMING WAVEFORM OF BURST STOP by $\overline{CS}$ [Latency=5, Burst Length=4]** ($\overline{WE}$=$V_{IH}$, $\overline{MRS}$=$V_{IH}$)

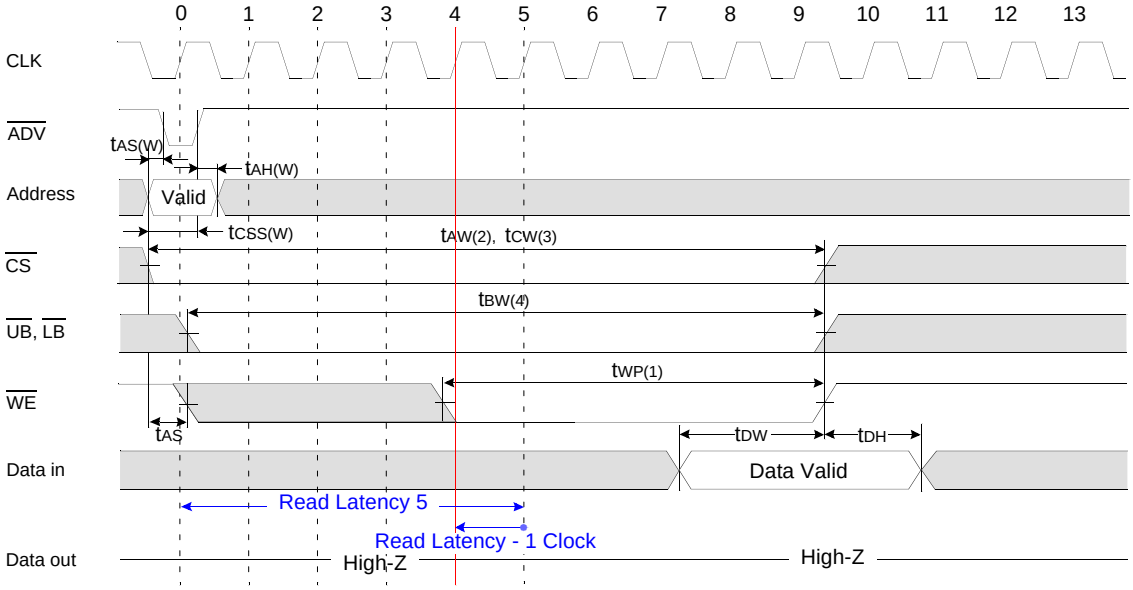



(SYNCHRONOUS BURST STOP)

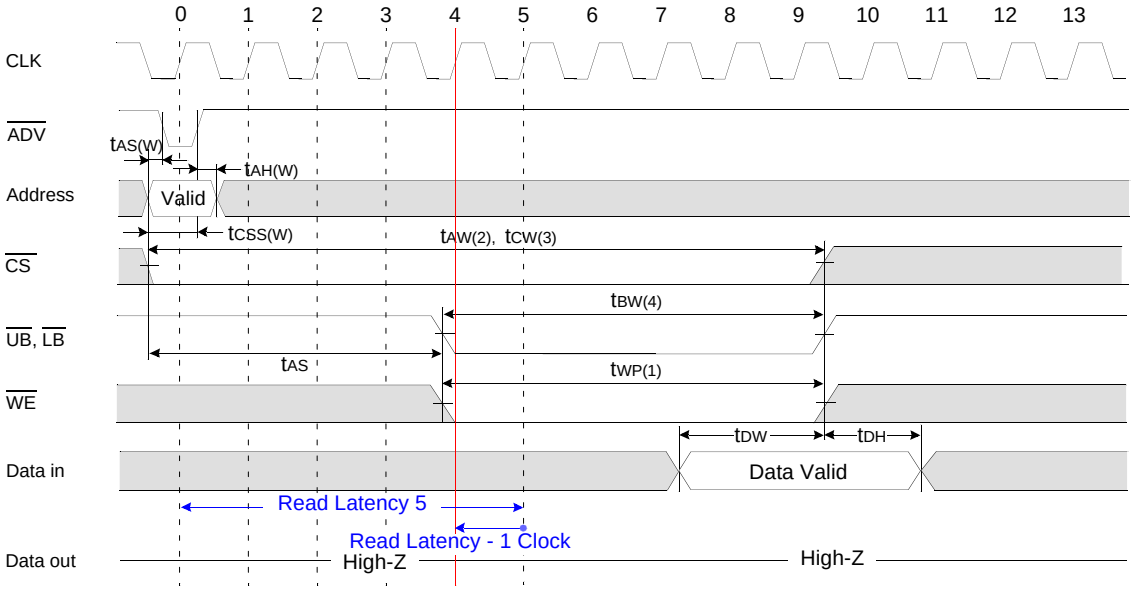
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.

## ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

### TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type) ($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{WE}$ Controlled)




### TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type) ($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{UB}$ & $\overline{LB}$ Controlled)

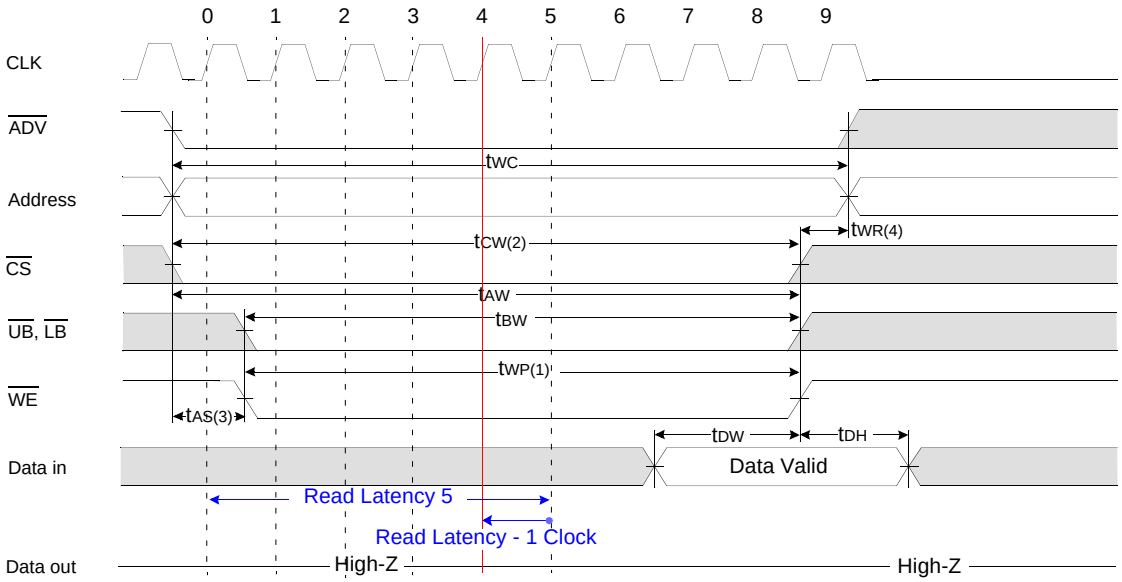



(ADDRESS LATCH TYPE WRITE CYCLE)

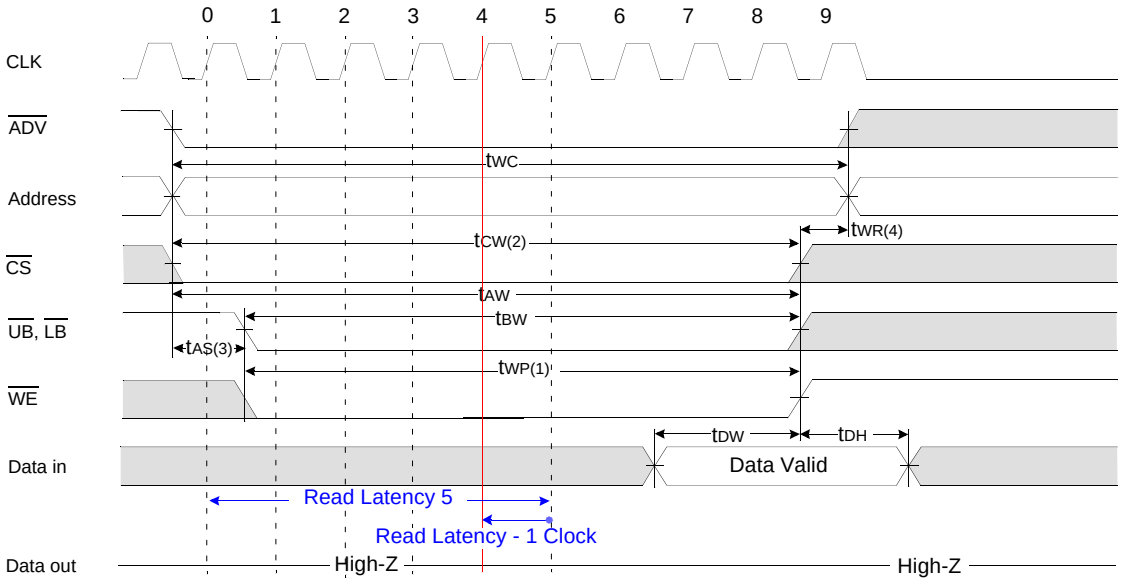
1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting UB or LB for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{AW}$ is measured from the address valid to the end of write. In this address latch type write timing, $t_{WC}$ is same as $t_{AW}$.
3. $t_{CW}$ is measured from the $\overline{CS}$ going low to the end of write.
4. $t_{BW}$ is measured from the $\overline{UB}$ and $\overline{LB}$ going low to the end of write.
5. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

## ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

### TIMING WAVEFORM OF WRITE CYCLE(Low $\overline{ADV}$ Type) ($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{WE}$ Controlled)




### TIMING WAVEFORM OF WRITE CYCLE(Low $\overline{ADV}$ Type) ($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{UB}$ & $\overline{LB}$ Controlled)

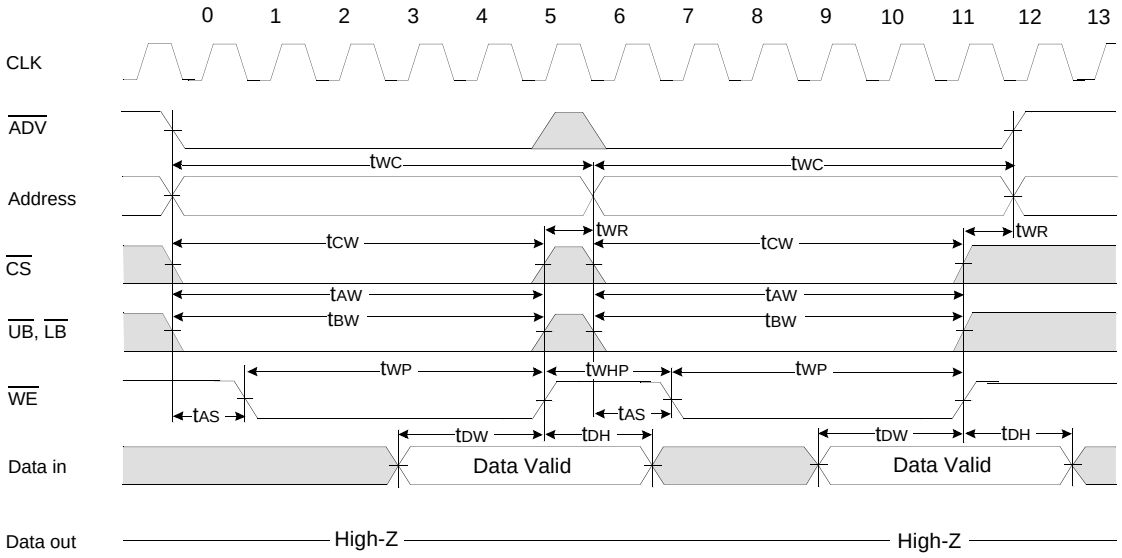



(LOW $\overline{ADV}$ TYPE WRITE CYCLE)

1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS}$ going low to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

## ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

### TIMING WAVEFORM OF CONTINUOUS WRITE CYCLE(Low $\overline{ADV}$ Type) ($\overline{MRS}$=$V_{IH}$, $\overline{OE}$=$V_{IH}$, $\overline{WE}$ Controlled)

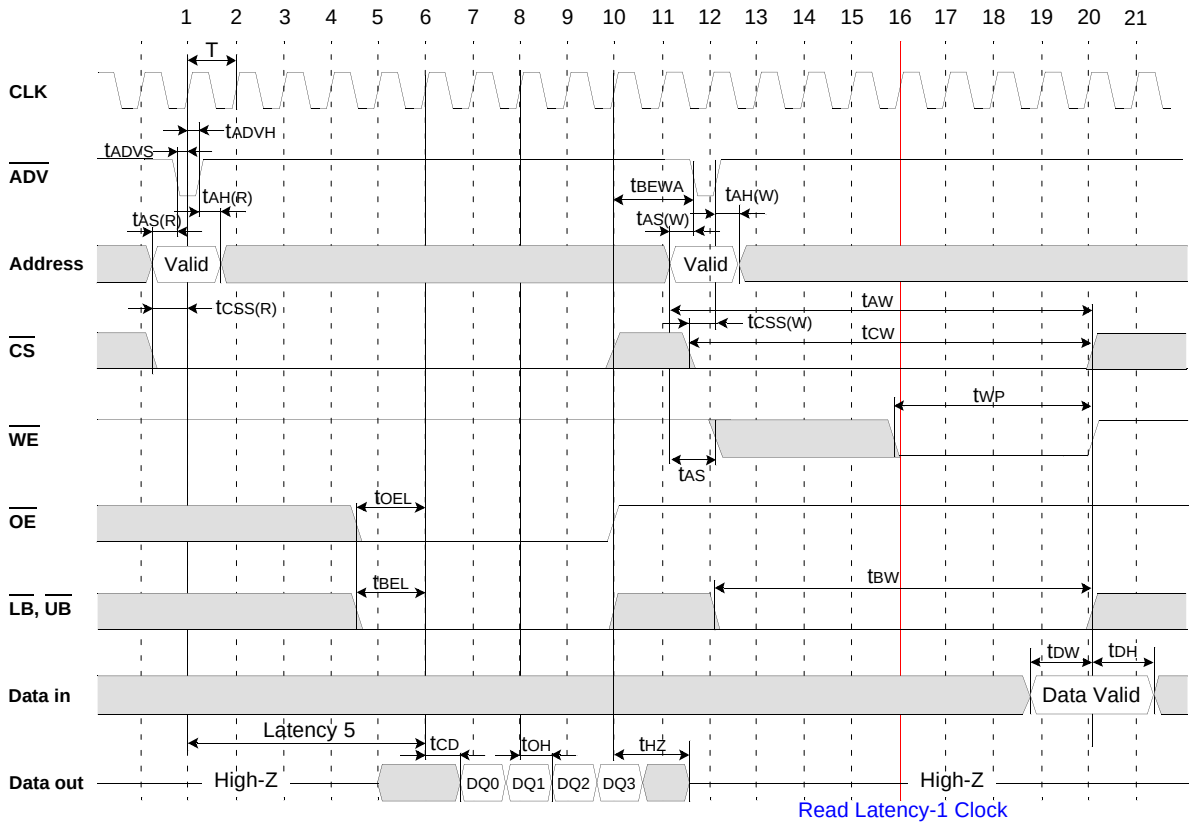



(LOW $\overline{ADV}$ TYPE CONTINUOUS WRITE CYCLE)

1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS}$ going low to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. Clock input does not have any affect to the continuous write operation if $t_{WHP}$ is shorter than (Read Latency - 1) clock duration.
6. $t_{WP}$(min)=85ns for continuous write operation over 50 times.

## SYNCH. BURST READ to ASYNCH. WRITE(Address Latch Type) TIMING WAVEFORM

**[Latency=5, Burst Length=4]** ($\overline{MRS}$=$V_{IH}$)

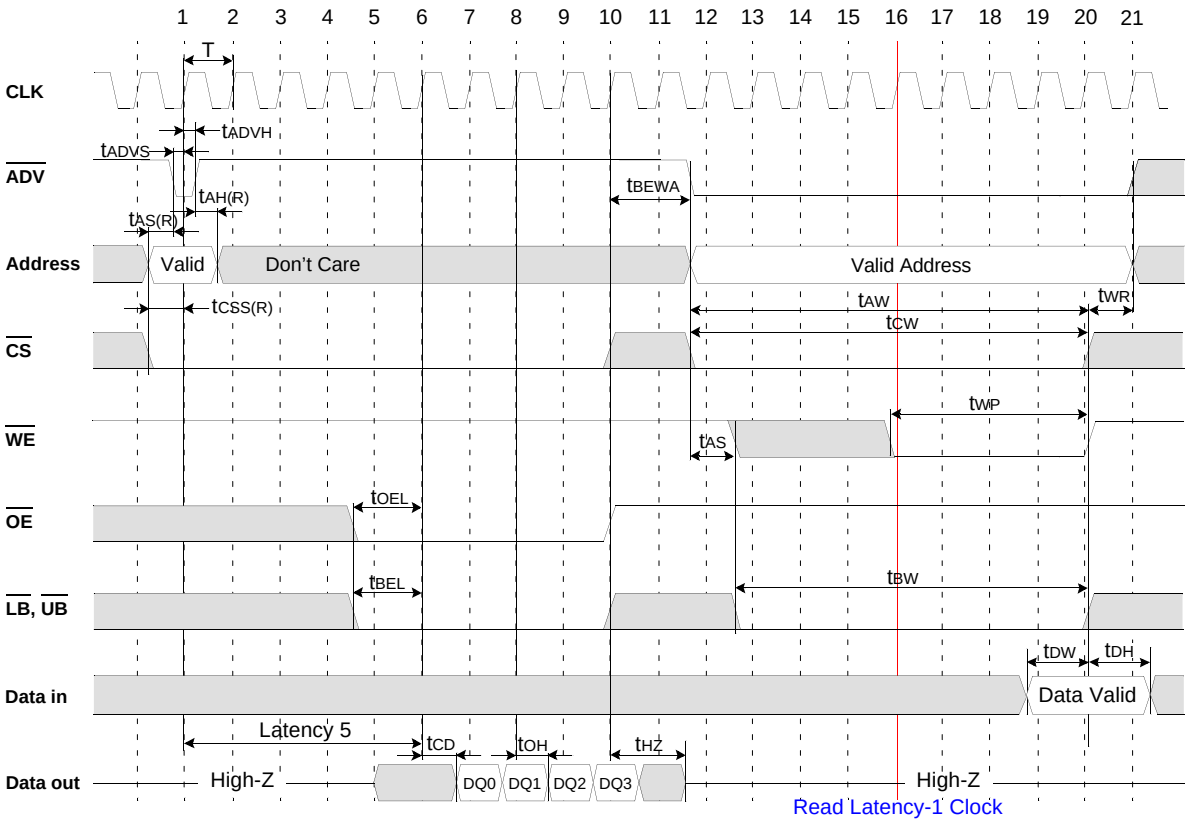



(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

## SYNCH. BURST READ to ASYNCH. WRITE(Low $\overline{ADV}$ Type) TIMING WAVEFORM

**[Latency=5, Burst Length=4]** ($\overline{MRS}$=$V_{IH}$)

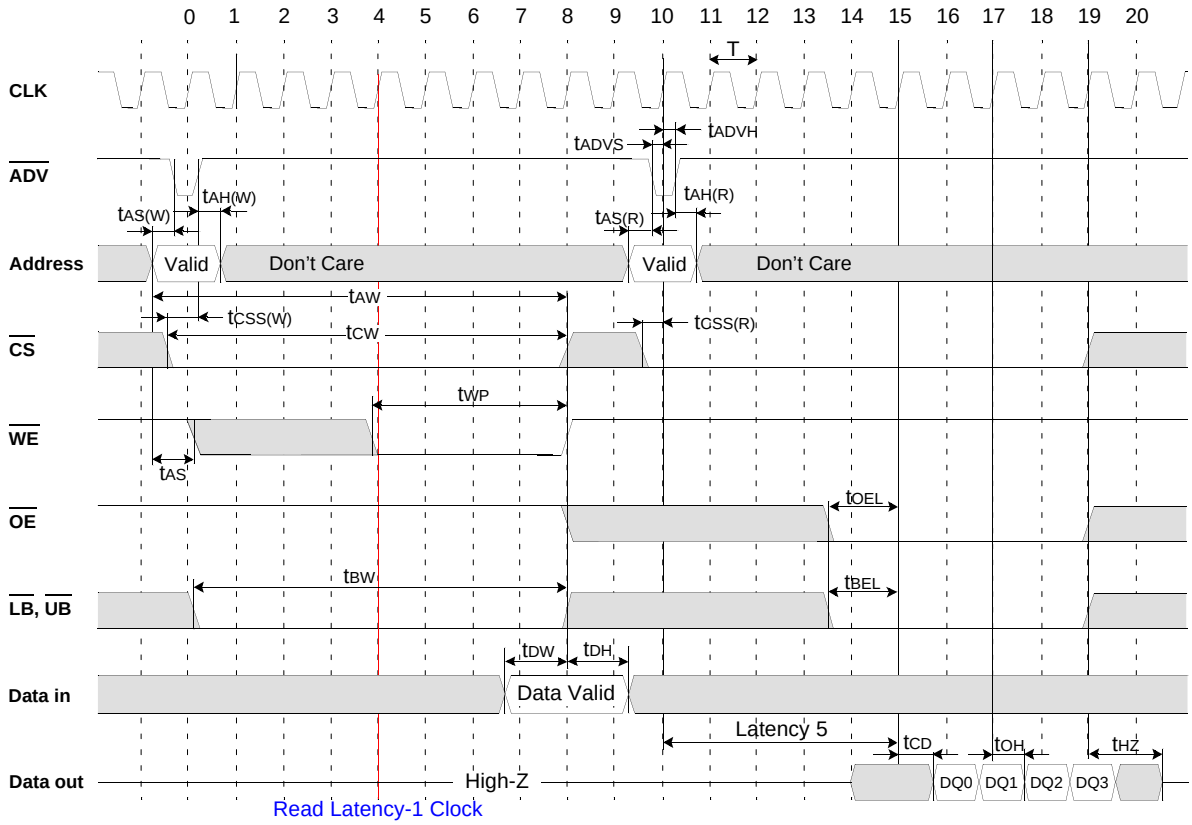



(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

(LOW $\overline{ADV}$ TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

## ASYNCH. WRITE(Address Latch Type) to SYNCH. BURST READ TIMING WAVEFORM

**[Latency=5, Burst Length=4]**($\overline{MRS}$=$V_{IH}$)

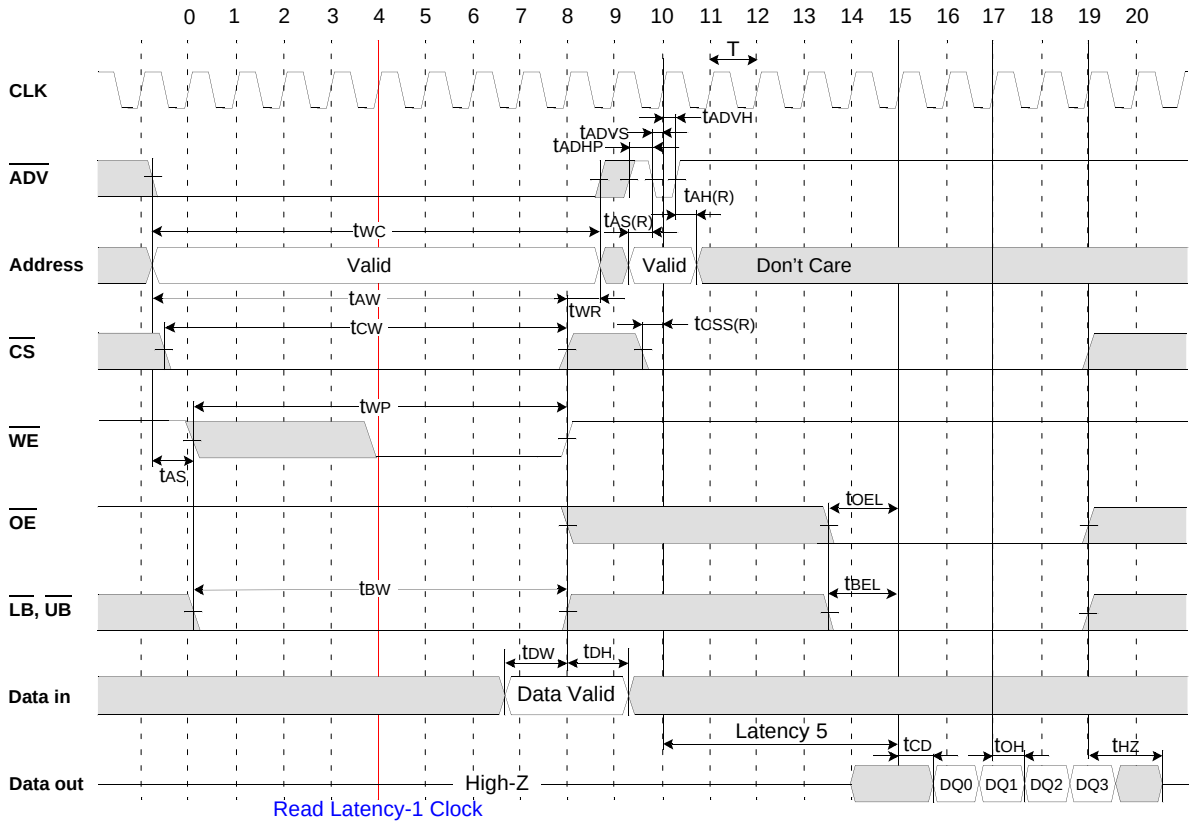



(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

## ASYNCH. WRITE(Low $\overline{ADV}$ Type) to SYNCH. BURST READ TIMING WAVEFORM

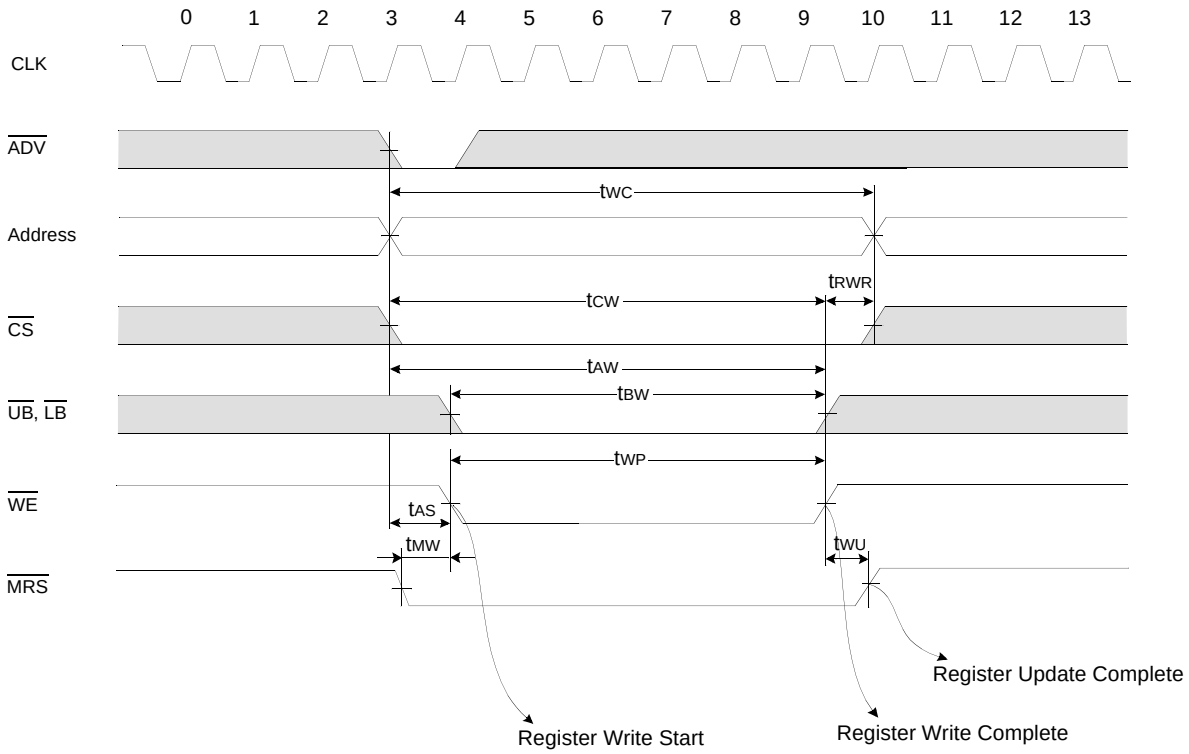
**[Latency=5, Burst Length=4]** ($\overline{MRS}$=$V_{IH}$)




(SYNCHRONOUS BURST READ CYCLE)
1. Only one rising edge of the clock is allowed during $\overline{ADV}$ low pulse.
2. The next operation can be issued only after the previous burst operation is finished.

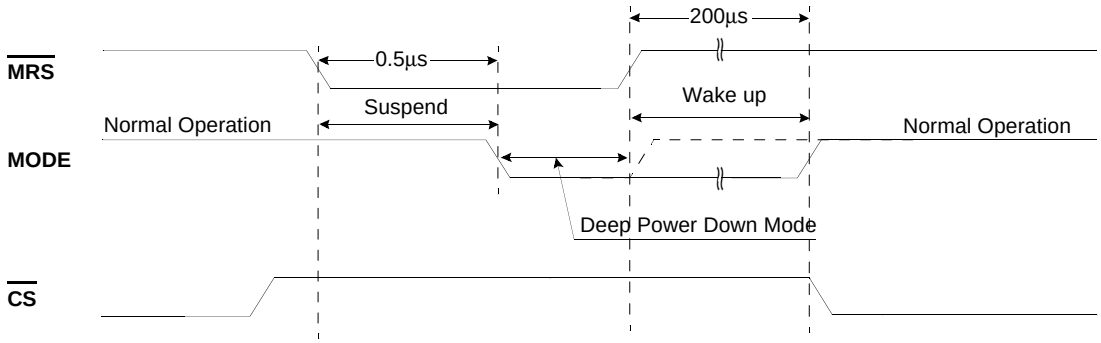
(LOW $\overline{ADV}$ TYPE ASYNCHRONOUS WRITE CYCLE - $\overline{WE}$ controlled)
1. Clock input does not have any affect to the write operation if $\overline{WE}$ is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to $\overline{WE}$ low going for proper write operation.

## TIMING WAVEFORM OF MRS MODE SETTING ($\overline{OE}$=$V_{IH}$)




(MRS SETTING TIMING)
1. Clock input does not have any affect to the register write operation.

## TIMING WAVEFORM OF DEEP POWER DOWN MODE ENTRY AND EXIT




(DEEP POWER DOWN MODE)

1. When $\overline{MRS}$ pin is driven to low under the standby state, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. In this case, the stanby state is achieved by toggling $\overline{CS}$ pin high.
3. To return to normal operation, the device needs Wake Up period.
4. Wake Up sequence is just the same as Power Up sequence.

## PACKAGE DIMENSION

### 111-Ball Fine pitch Ball Grid Array Package (measured in millimeters)