Document Title

Multi-Chip Package MEMORY
256M Bit (16Mx16) Nand Flash Memory / 8M Bit (512Kx16) Full CMOS SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft.	April 18, 2003	Preliminary
0.1	Revised - Added comment on $\overline{BYTE}$s and SA pin function in SRAM FUNCTIONAL DESCRIPTION. - Deleted output load condition of "C_L=100pF+1TTL" in SRAM AC TEST CONDITION.	April 30, 2003	Preliminary
0.5	Revised <NAND Flash> - Changed t_{CLH}(min) from 10ns to 8ns in AC Timing Characteristics. - Changed t_{CH}(min) from 10ns to 8ns in AC Timing Characteristics. - Changed t_{ALH}(min) from 10ns to 8ns in AC Timing Characteristics. - Changed t_{DH}(min) from 10ns to 8ns in AC Timing Characteristics. - Changed t_{RHZ}(max) from 30ns to 26ns in AC Characteristics. - Added Page Program Operation Timing. <SRAM> - Changed t_{OHZ}(max) from 20ns to 11ns in AC Characteristics. - Changed t_{CW}(min) from 45ns to 40ns in AC Characteristics. - Changed t_{DH}(min) from 0ns to -1ns in AC Characteristics.	July 7, 2003	Preliminary

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

Multi-Chip Package MEMORY
256M Bit (16Mx16) Nand Flash Memory / 8M Bit (512Kx16) Full CMOS SRAM

FEATURES

<Common>
- Power Supply Voltage : 2.7V to 2.9V
- Operating Temperature : -25°C ~ 85°C
- Package : 69 - ball FBGA Type - 8 x 11mm, 0.8 mm pitch

<NAND Flash>
- Voltage Supply : 2.4~2.9V
- Organization
  - Memory Cell Array : (16M + 512K)bit x16bit
  - Data Register : (256 + 8)bit x16bit
- Automatic Program and Erase
  - Page Program : (256 + 8)Word
  - Block Erase : (8K + 256)Word
- Page Read Operation
  - Page Size : (256 + 8)Word
  - Random Access : 10µs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back
- Unique ID for Copyright Protection

<SRAM>
- Organization: 512K x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs

GENERAL DESCRIPTION

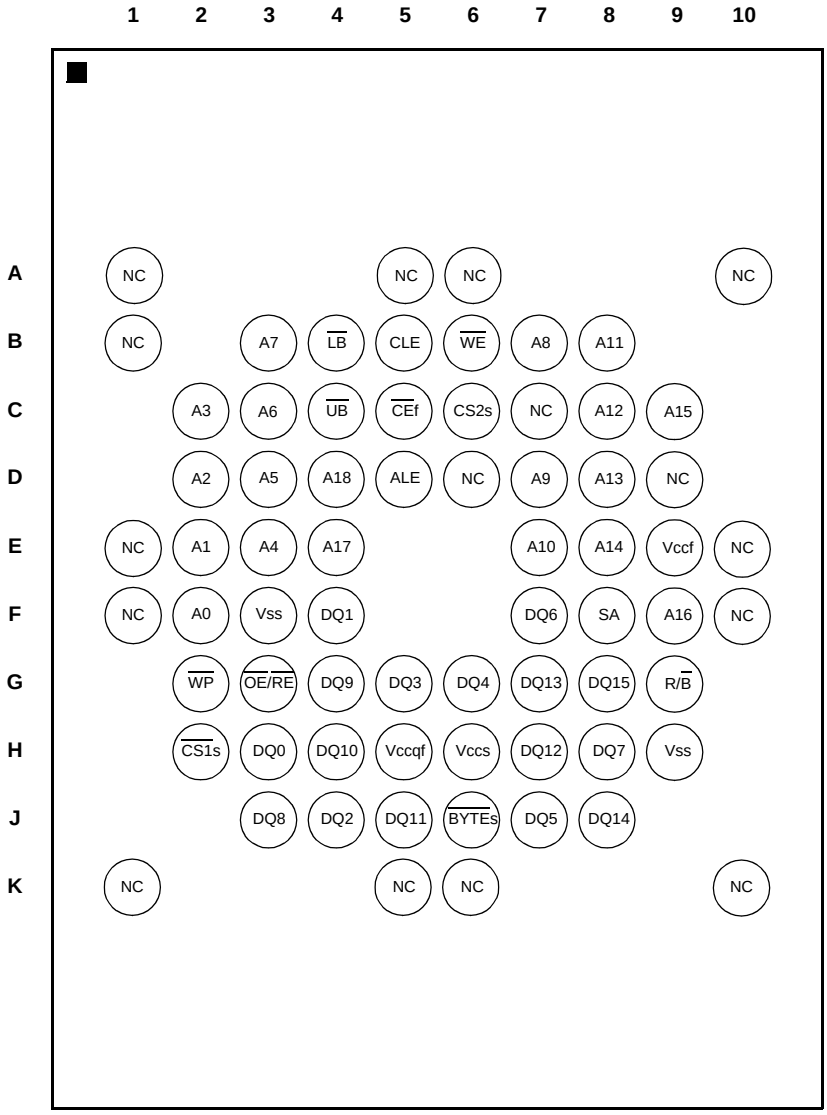
The K5P5781FCM featuring single 2.8V power supply is a Multi Chip Package Memory which combines 256Mbit Nand Flash and 8Mbit full CMOS SRAM.

The 256Mbit Flash memory is organized as 16M x16 bit and the 8Mbit SRAM is organized as 512K x16 bit. In 256Mbit NAND Flash a program operation can be performed in typical 200µs on a 264-word page and an erase operation can be performed in typical 2ms on a 8K-word block. Data in the page can be read out at 50ns cycle time per word. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the FLASH′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The 8Mbit SRAM is fabricated by SAMSUNG′s advanced full CMOS process technology. The device supports low data retention voltage for battery back-up operation with low data retention current.

The K5P5781FCM is suitable for use in data memory of mobil communication system to reduce not only mount area but also power consumption. This device is available in 69-ball FBGA Type.

PIN CONFIGURATION



69-FBGA: Top View (Ball Down)

PIN DESCRIPTION

Ball Name	Description	Ball Name	Description
A_0 to A_{18}	Address Input Balls (SRAM)	ALE	Address Latch Enable (Flash Memory)
DQ_0 to DQ_{15}	Data Input/Output Balls (Common)	$\overline{BYTEs}$[1)]	$\overline{BYTE}$ Control (SRAM)
Vccf	Power Supply (Flash Memory)	SA[1)]	Address Inputs (SRAM)
Vccs	Power Supply (SRAM)	$\overline{CE}$f	Chip Enable (Flash Memory)
Vccqf	Output Buffer Power (Flash Memory) This input should be biased to Vccf.	$\overline{CS}$1s	Chip Select (SRAM Low Active)
		CS2s	Chip Select (SRAM High Active)
Vss	Ground (Common)	$\overline{WE}$	Write Enable (Common)
$\overline{LB}$	Lower Byte Enable (SRAM)	$\overline{OE}$/$\overline{RE}$	Output Enable (Common)
$\overline{UB}$	Upper Byte Enable (SRAM)	R/$\overline{B}$	Ready/Busy Output (Flash Memory)
$\overline{WP}$	Write Protection (Flash Memory)	NC	No Connection
CLE	Command Latch Enable (Flash Memory)		

Note :
1. Please refer to SRAM FUNCTIONAL DESCRIPTION in page 31.

ORDERING INFORMATION

K 5 P 57 81 F C M - F 0 55

Samsung MCP(2 Chip) Memory

Device Type
NAND Flash + fCMOS SRAM

NAND Flash Density , Org.
57 : 256Mbit, x16

SRAM Density , Org.
81 : 8Mbit, x16

Operating Voltage
F : 2.8V

SRAM Speed
55: 55ns

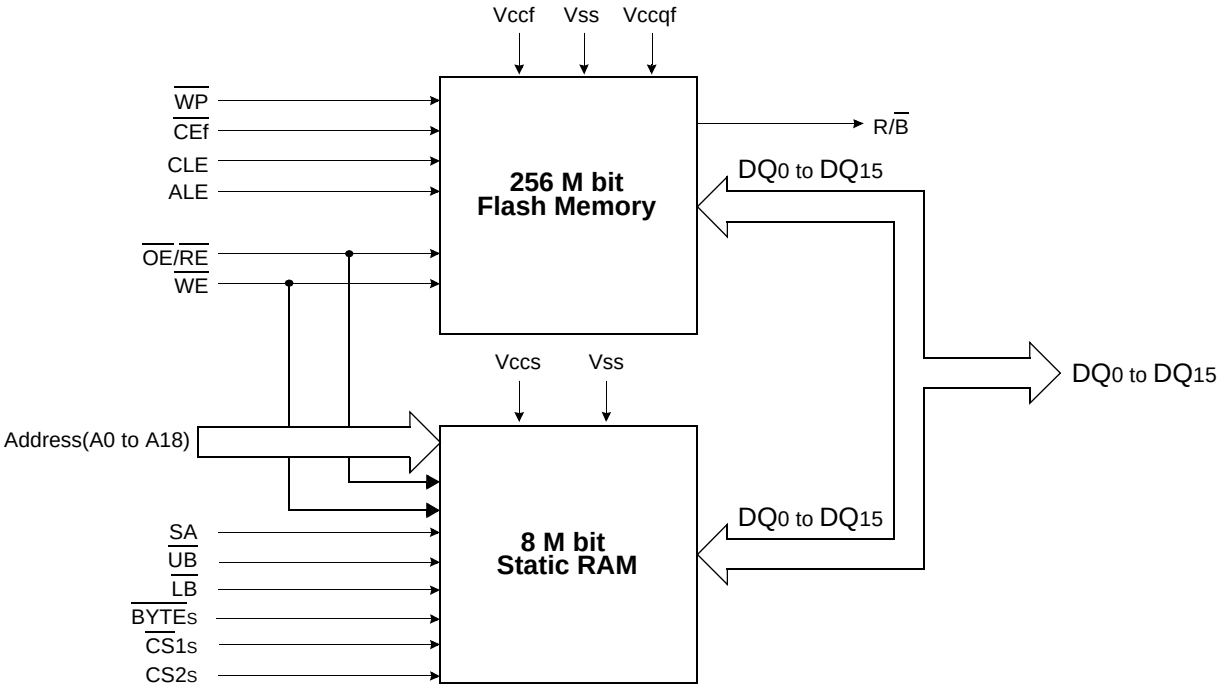
NAND Flash Speed
0 : NONE

Package
F : FBGA

Version
M : 1st Generation

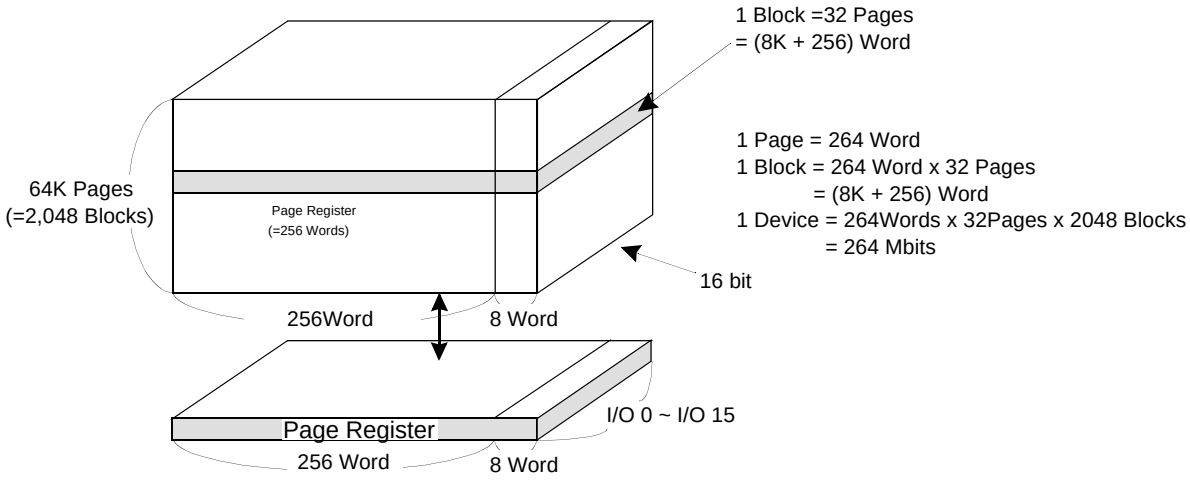
Flash Boot Block Mode
C : Uniform Block

Figure 1. FUNCTIONAL BLOCK DIAGRAM



256M Bit(16Mx16)
NAND Flash Memory

Figure 2. NAND Flash ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O8 to 15
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	L*
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	L*
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	L*

Column Address
Row Address (Page Address)

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

PRODUCT INTRODUCTION

The device is a 264Mbit(276,824,064 bit) memory organized as 65,536 rows(pages) by 264 columns. Spare eight columns are located from column address of 256~263. A 264-word data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of two NAND structures. A NAND structure consists of 16 cells. Total 16896 NAND cells reside in a block. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2048 separately erasable 8K-Word blocks. It indicates that the bit by bit erase operation is prohibited on the device.

The device has addresses multiplexed into lower 8 I/Os. Device allows sixteen bit wide data transport into and out of page registers. This scheme dramatically reduces pin counts while providing high performance and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset command, Read command, Status Read command, etc require just one cycle bus. Some other commands like Page Program and Copy-back Program and Block Erase, require two cycles: one cycle for setup and the other cycle for execution. The 16M-word physical space requires 24 addresses, thereby requiring three cycles for word-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the device.

The device includes one block sized OTP(One Time Programmable), which can be used to increase system security or to provide identification capabilities. Detailed information can be obtained by contact with Samsung.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	00h	8Ah	
Lock	2Ah		
Unlock	23h	24h	
Lock-tight	2Ch		
Read Block Lock Status	7Ah		
Block Erase	60h	D0h	
Read Status	70h	-	O

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN/OUT}$	-0.6 to + 4.6	V
	V_{CC}	-0.6 to + 4.6	
	V_{CCQ}	-0.6 to + 4.6	
Temperature Under Bias	T_{BIAS}	-40 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Short Circuit Current	Ios	5	mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC},+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.4	2.65	2.9	V
Supply Voltage	V_{CCQ}	2.4	2.65	2.9	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I_{CC1}	tRC=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	20	mA
	Program	I_{CC2}	-	-	10	25	
	Erase	I_{CC3}	-	-	10	25	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	
Input High Voltage		V_{IH}	I/O pins	V_{CCQ}-0.4	-	V_{CCQ}+0.3	V
			Except I/O pins	V_{CC}-0.4	-	V_{CC}+0.3	
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.5	
Output High Voltage Level		V_{OH}	I_{OH}=-100µA	V_{CCQ}-0.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=100µA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.1V	3	4	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	2013	-	2048	Blocks

NOTE :
1. The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.
3. Minimum 1004 valid blocks are guaranteed for each contiguous 128Mb memory space.

AC TEST CONDITION

(TA=-40 to 85°C, Vcc=2.4V~2.9V)

Parameter	NAND Flash
Input Pulse Levels	0V to VccQ
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VccQ/2
Output Load (VccQ:2.65V +/-10%)	1 TTL GATE and CL=30pF

CAPACITANCE(T_A=25°C, V_{CC}=2.65V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⌐↑	H	X	Read Mode	Command Input
L	H	L	⌐↑	H	X		Address Input(3clock)
H	L	L	⌐↑	H	H	Write Mode	Command Input
L	H	L	⌐↑	H	H		Address Input(3clock)
L	L	L	⌐↑	H	H	Data Input	
L	L	L	H	↓⌐	X	Data Output	
L	L	L	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Dummy Busy Time for the Lock or Lock-tight Block		t_{LBSY}	-	5	10	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	8	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	.-	ns
$\overline{CE}$ Hold Time	t_{CH}	8	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25 (1)	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	8	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	8	-	ns
Write Cycle Time	t_{WC}	45	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NOTE :
1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	25	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{CE}$ Access Time	t_{CEA}	-	45	ns
$\overline{RE}$ Access Time	t_{REA}	-	30	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	26	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR1}	60	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low in Block Lcok Mode	t_{WHR2}	100	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

NOTE :
1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. The time to Ready depends on the value of the pull-up resistor tied R/B pin.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st word in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFFFh data at the column address of 256 and 261. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original invalid block information is prohibited.

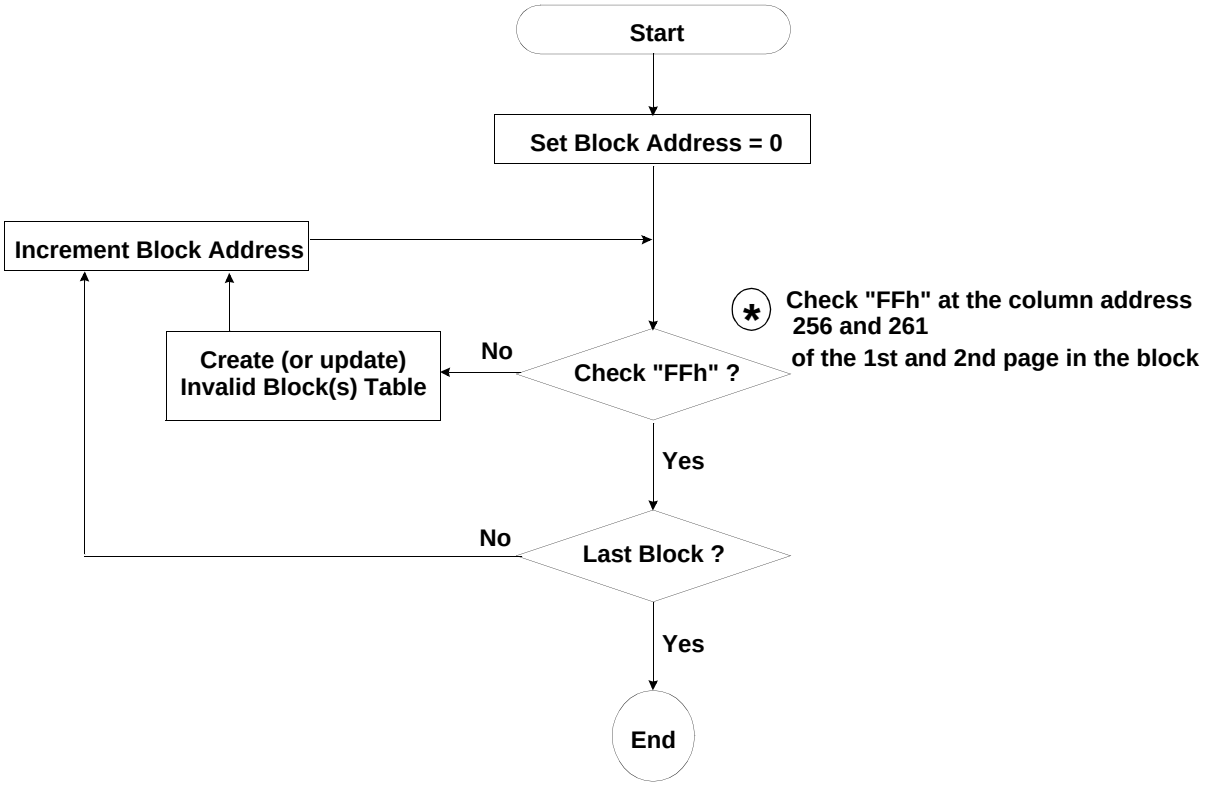


Figure 3. Flow chart to create invalid block table.

NAND Flash Technical Notes *(Continued)*

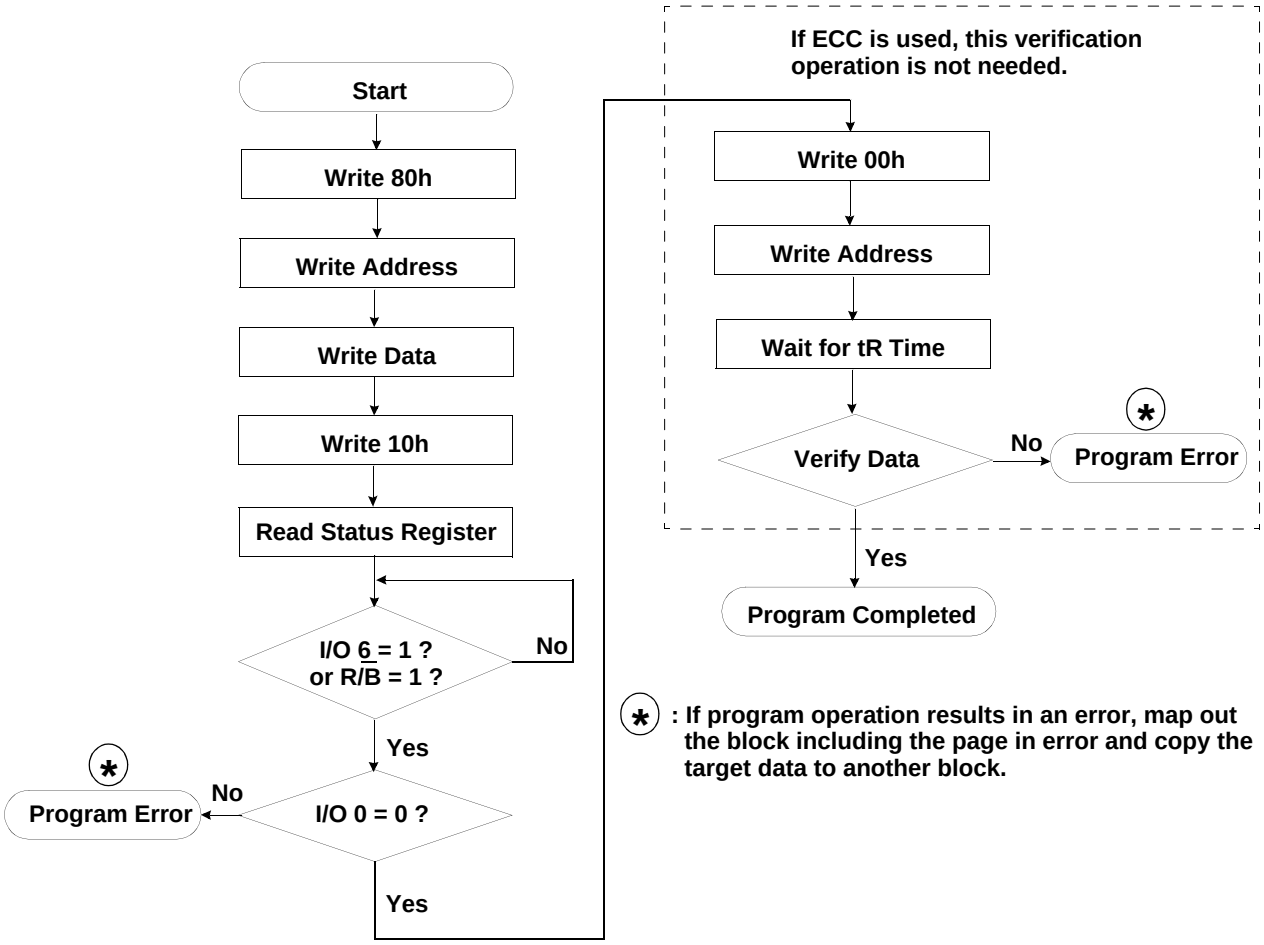
Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

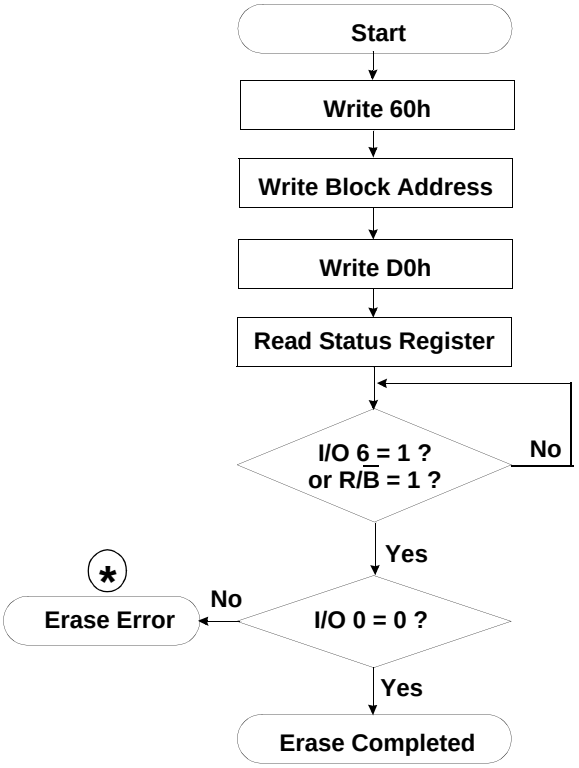
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

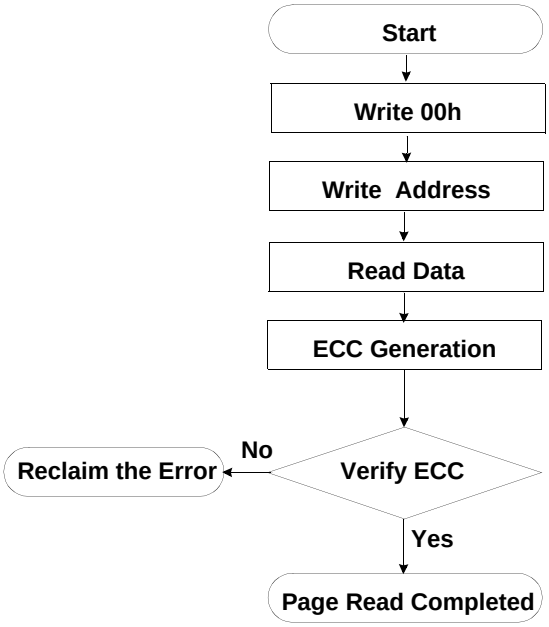


NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

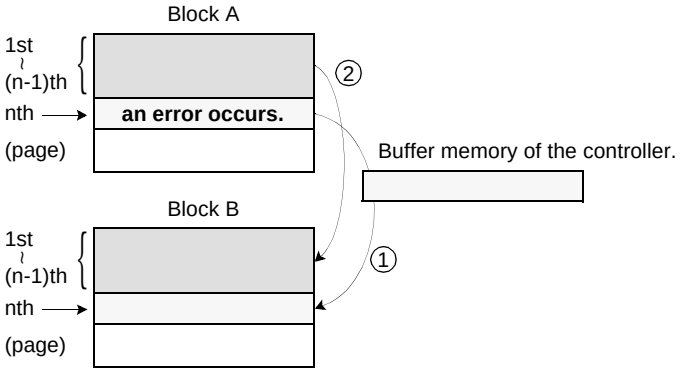


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
* Step4
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Pointer Operation

Samsung NAND Flash has two address pointer commands as a substitute for the most significant column address. '00h' command sets the pointer to 'A' area(0~255word), and '50h' command sets the pointer to 'B' area(256~263word). With these commands, the starting column address can be set to any of a whole page(0~263word). '00h' or '50h' is sustained until another address pointer command is inputted. To program data starting from 'A' or 'B' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary.

Table 3. Destination of the pointer

Command	Pointer position	Area
00h 50h	0 ~ 255 word 256 ~ 263 word	main array(A) spare array(B)

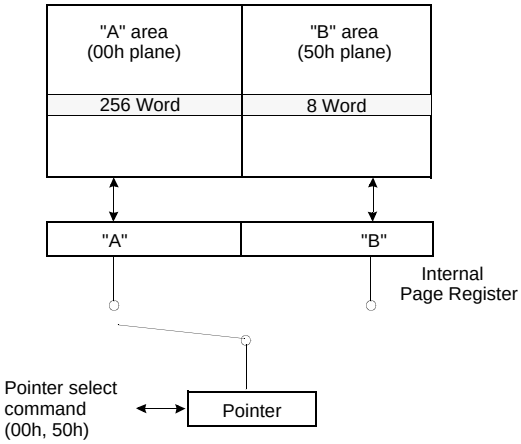
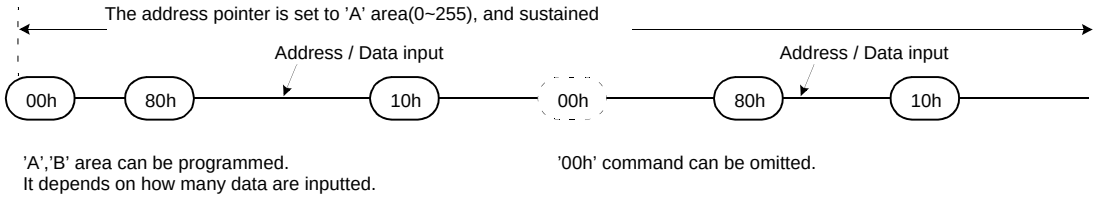
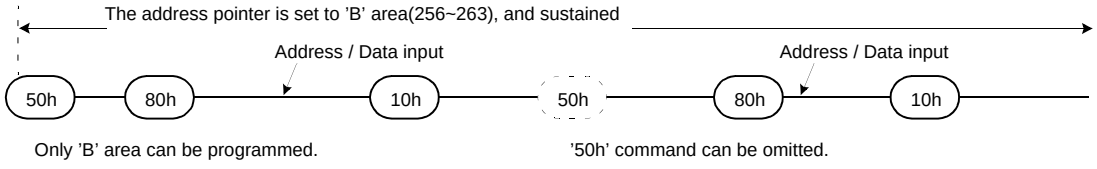


Figure 5. Block Diagram of Pointer Operation

(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte/264word page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 6. Program Operation with $\overline{CE}$ don't-care.

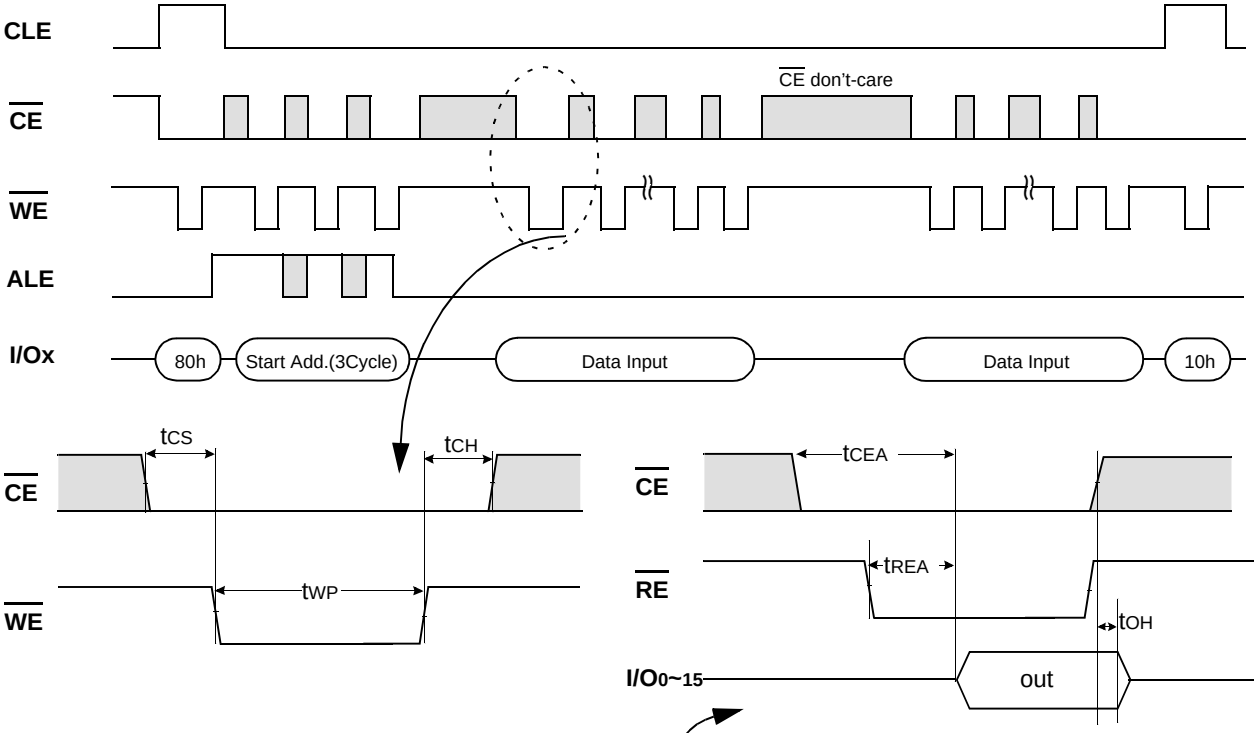
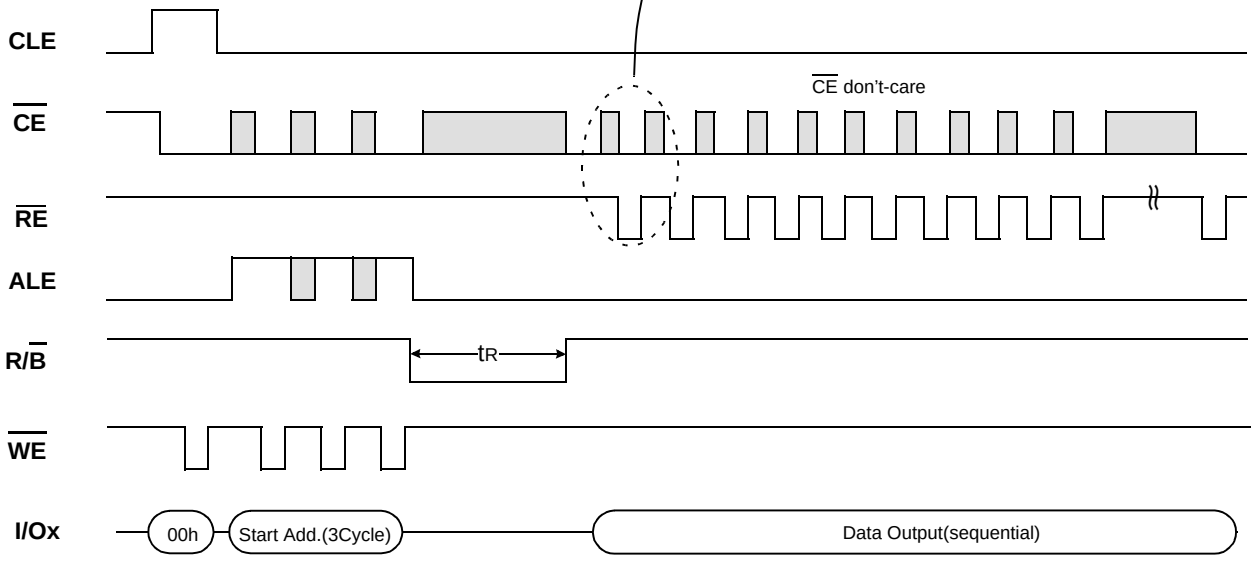


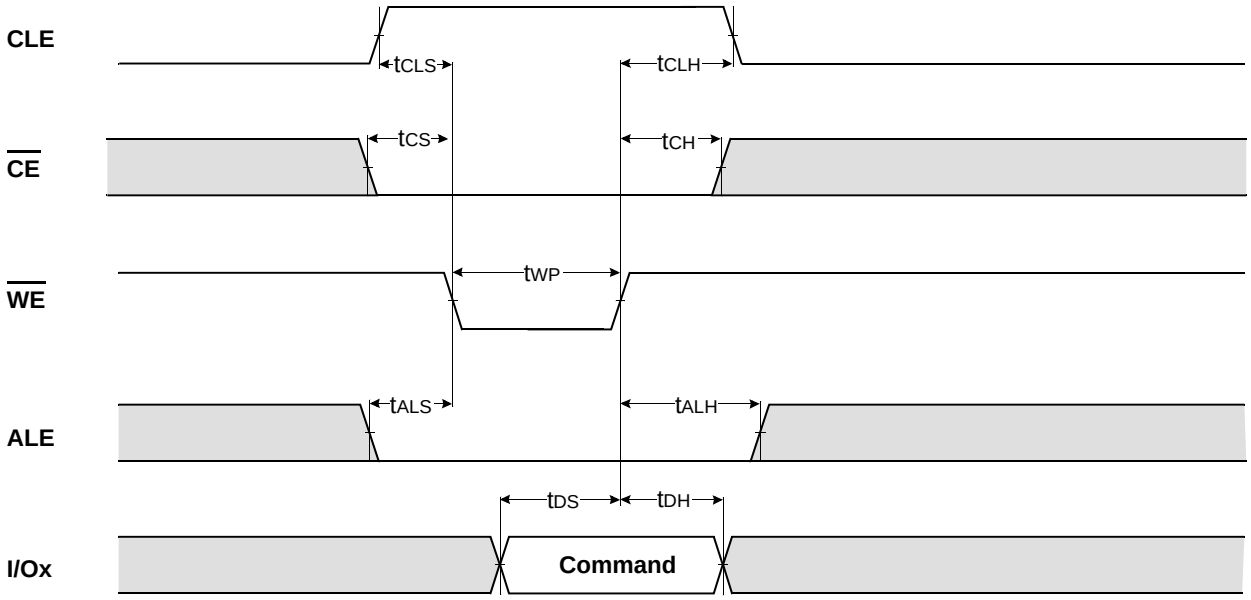
Figure 7. Read Operation with $\overline{CE}$ don't-care.



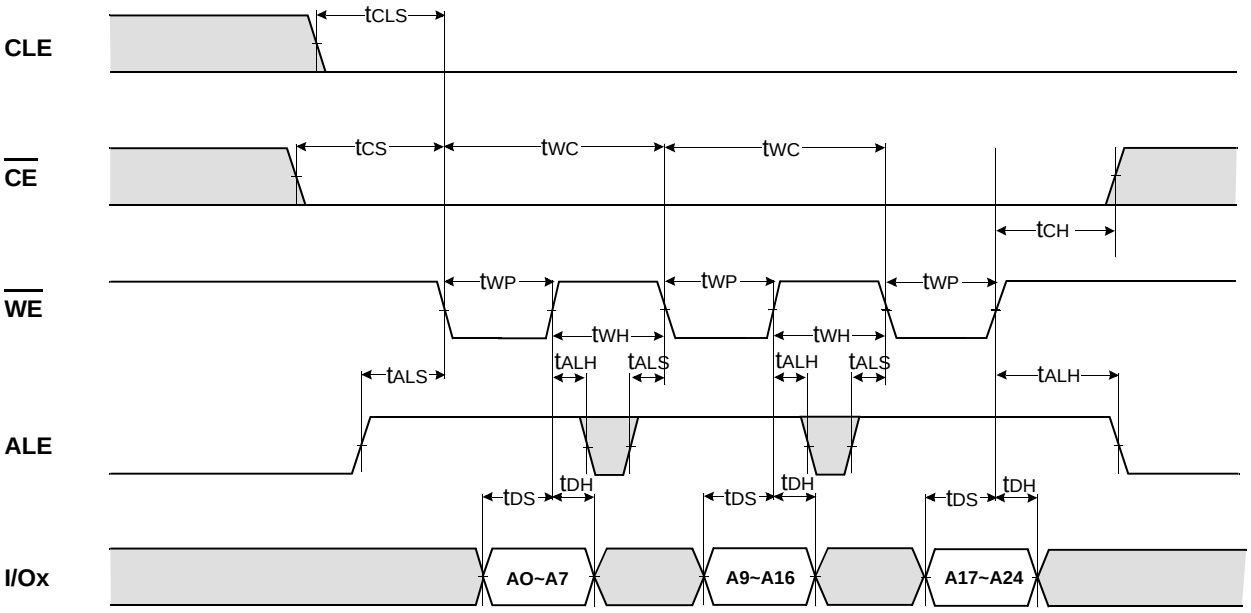
Device	I/O	DATA
	I/Ox	Data In/Out
NAND Flash	I/O 0 ~ I/O 15[1)]	~264word

NOTE: 1. I/O8~15 must be set to "0" during command or address input.
2. I/O8~15 are used only for data bus.

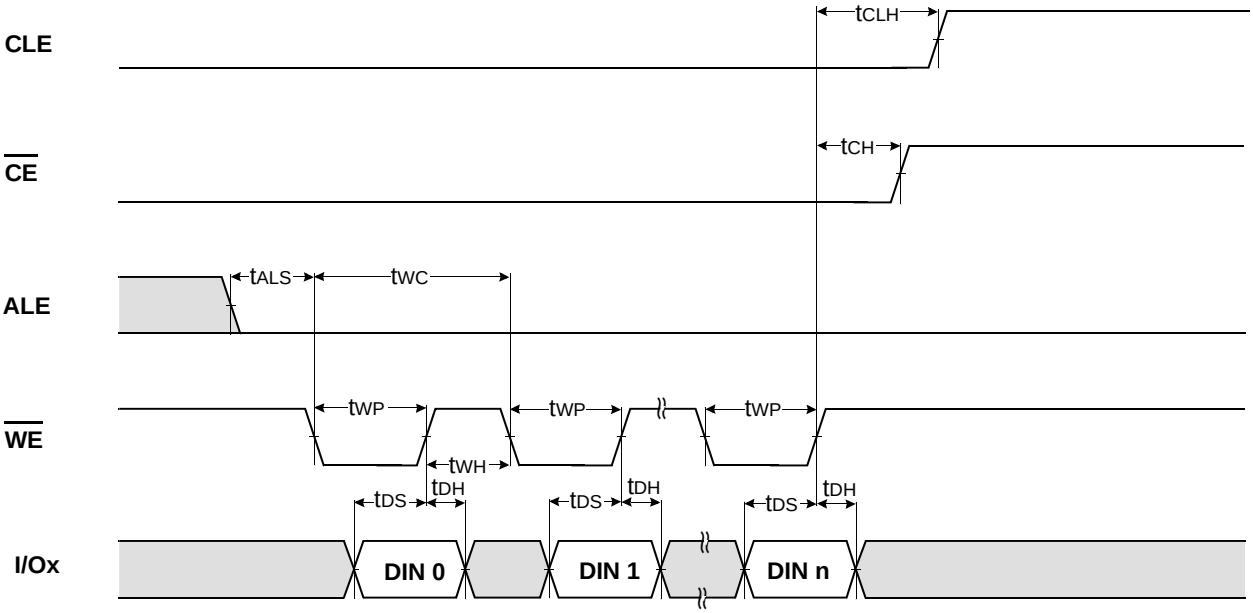
* Command Latch Cycle



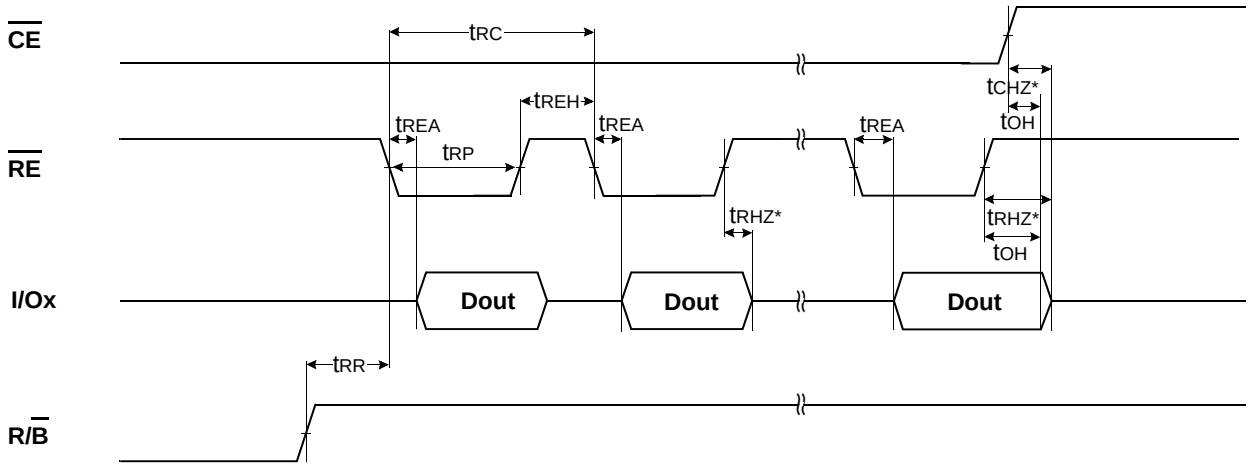
* Address Latch Cycle



*** Input Data Latch Cycle**

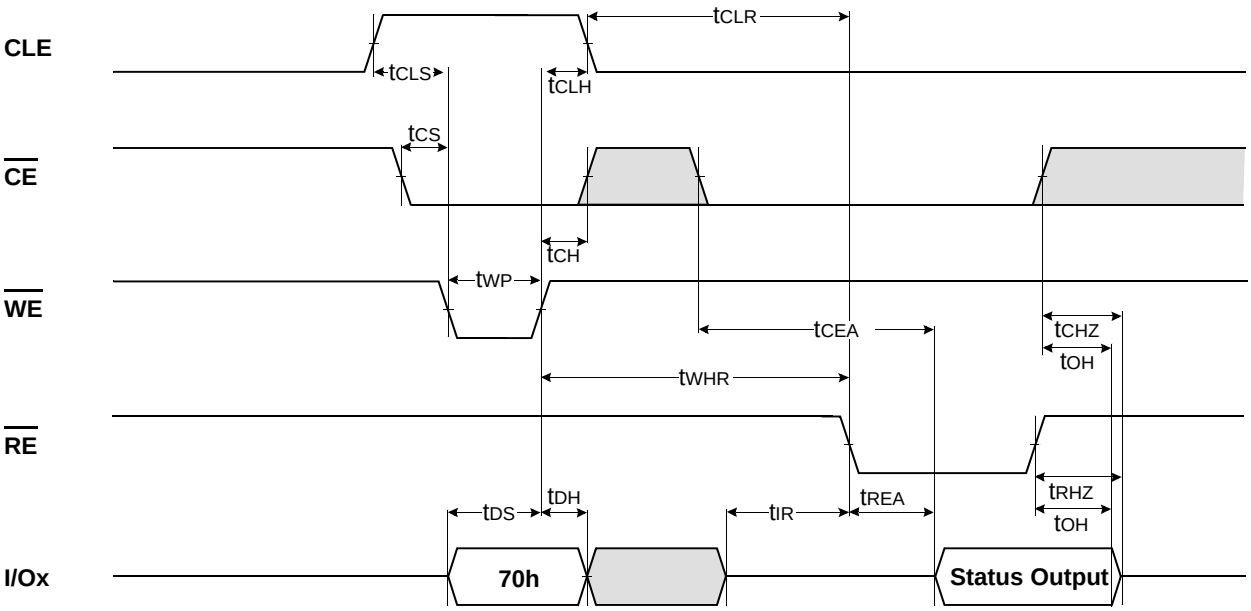


*** Sequential Out Cycle after Read**(CLE=L, $\overline{WE}$=H, ALE=L)

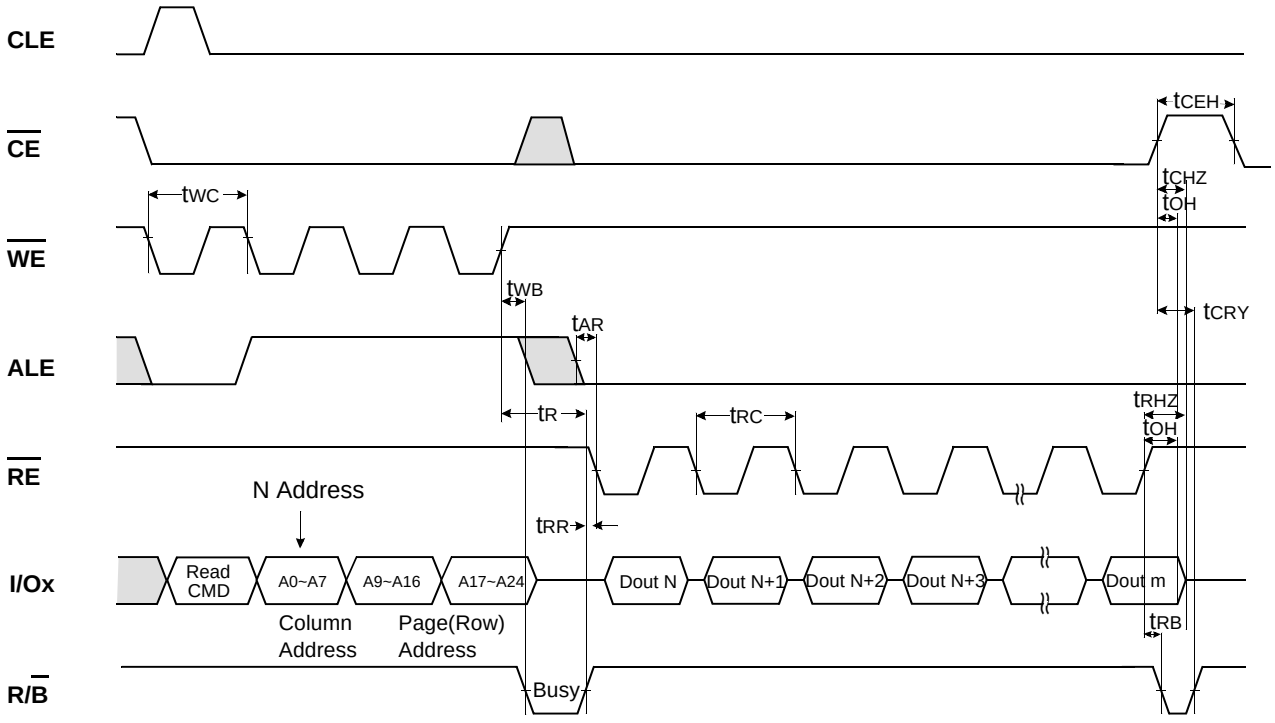


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

*** Status Read Cycle**

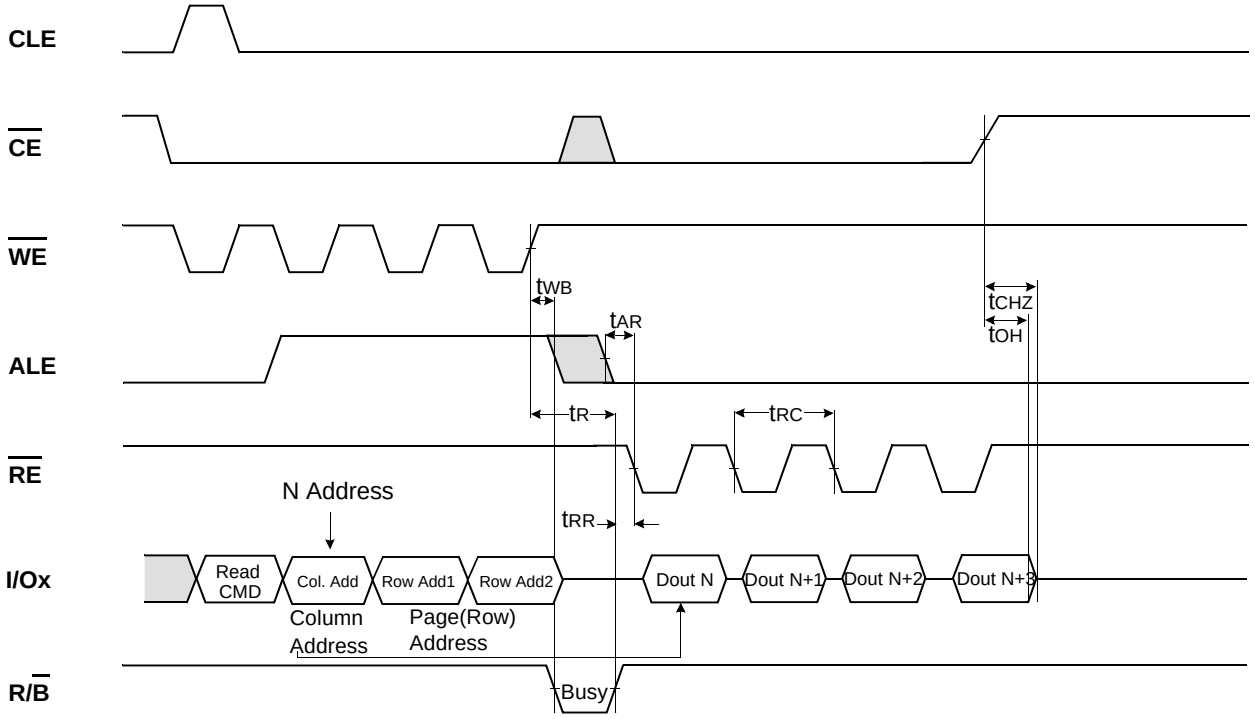


READ1 OPERATION(READ ONE PAGE)

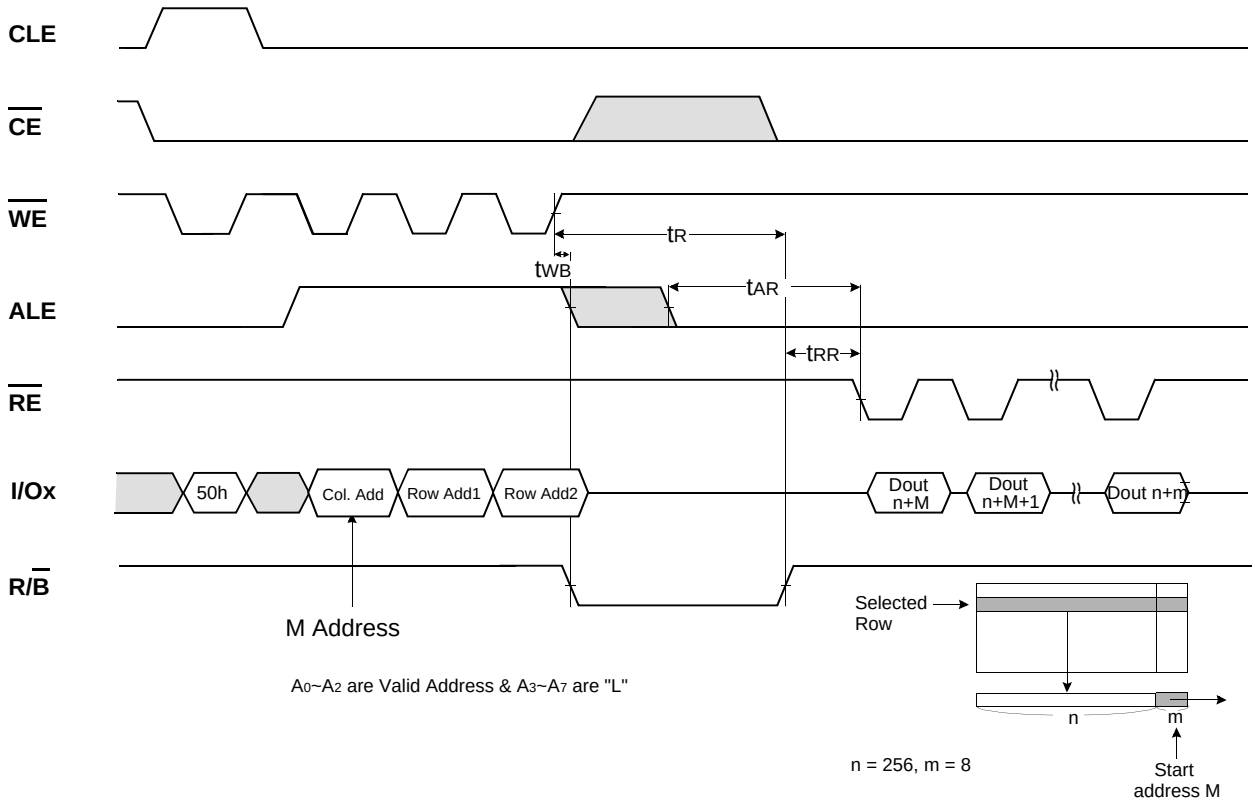


m = 264 , Read CMD = 00h

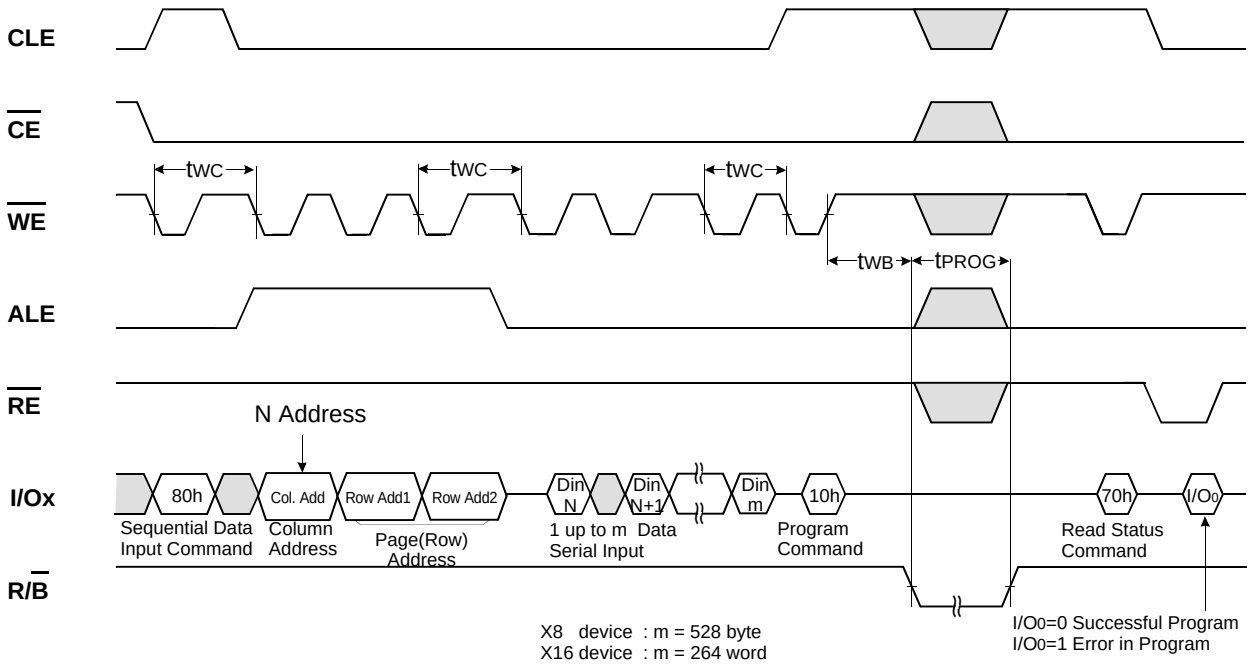
READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)



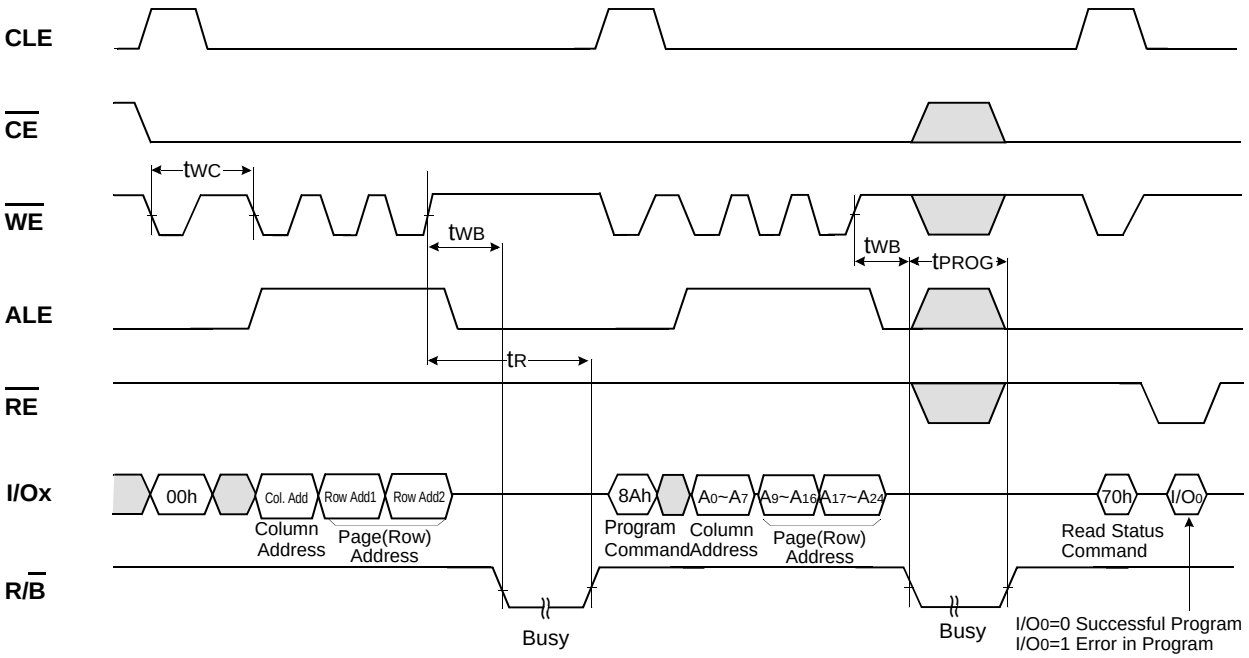
READ2 OPERATION (READ ONE PAGE)



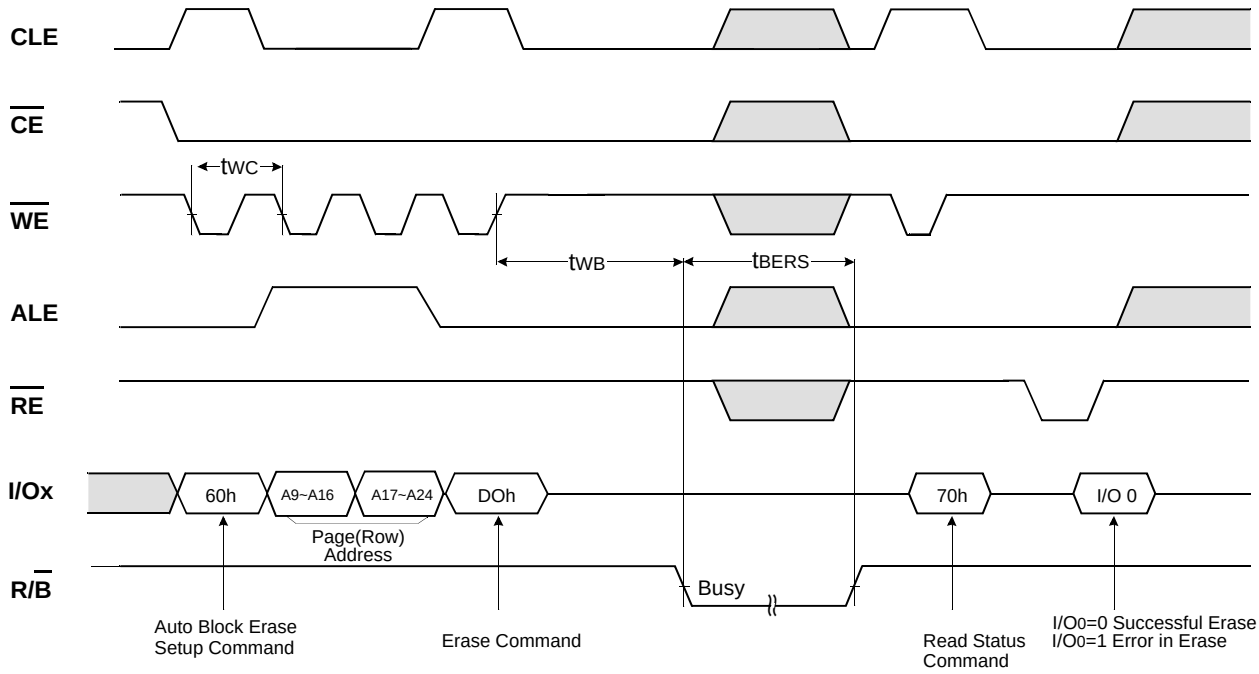
PAGE PROGRAM OPERATION



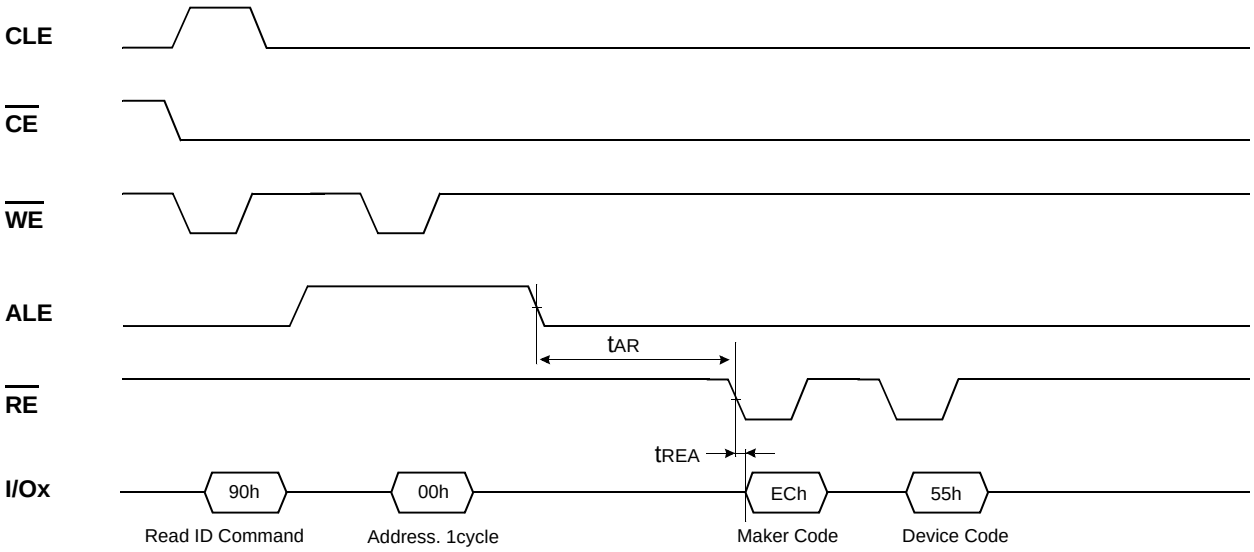
COPY-BACK PROGRAM OPERATION



BLOCK ERASE OPERATION (ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION



DEVICE OPERATION

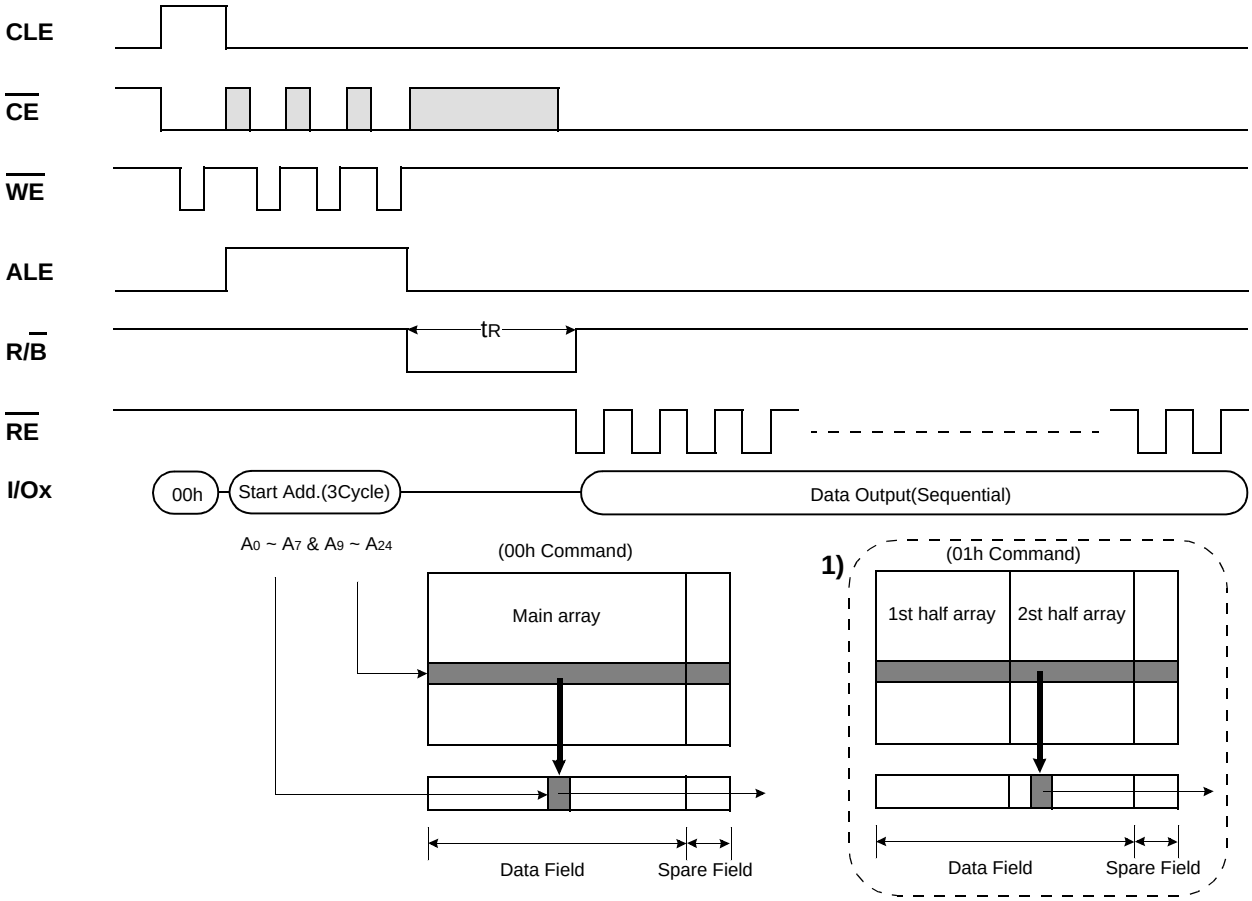
PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operations are available : random read, serial page read.

The random read mode is enabled when the page address is changed. The 264 words of data within the selected page are transferred to the data registers in less than 10μs(t_R). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data starting from the selected column address up to the last column address[column 255 /263 depending on the state of GND input pin].

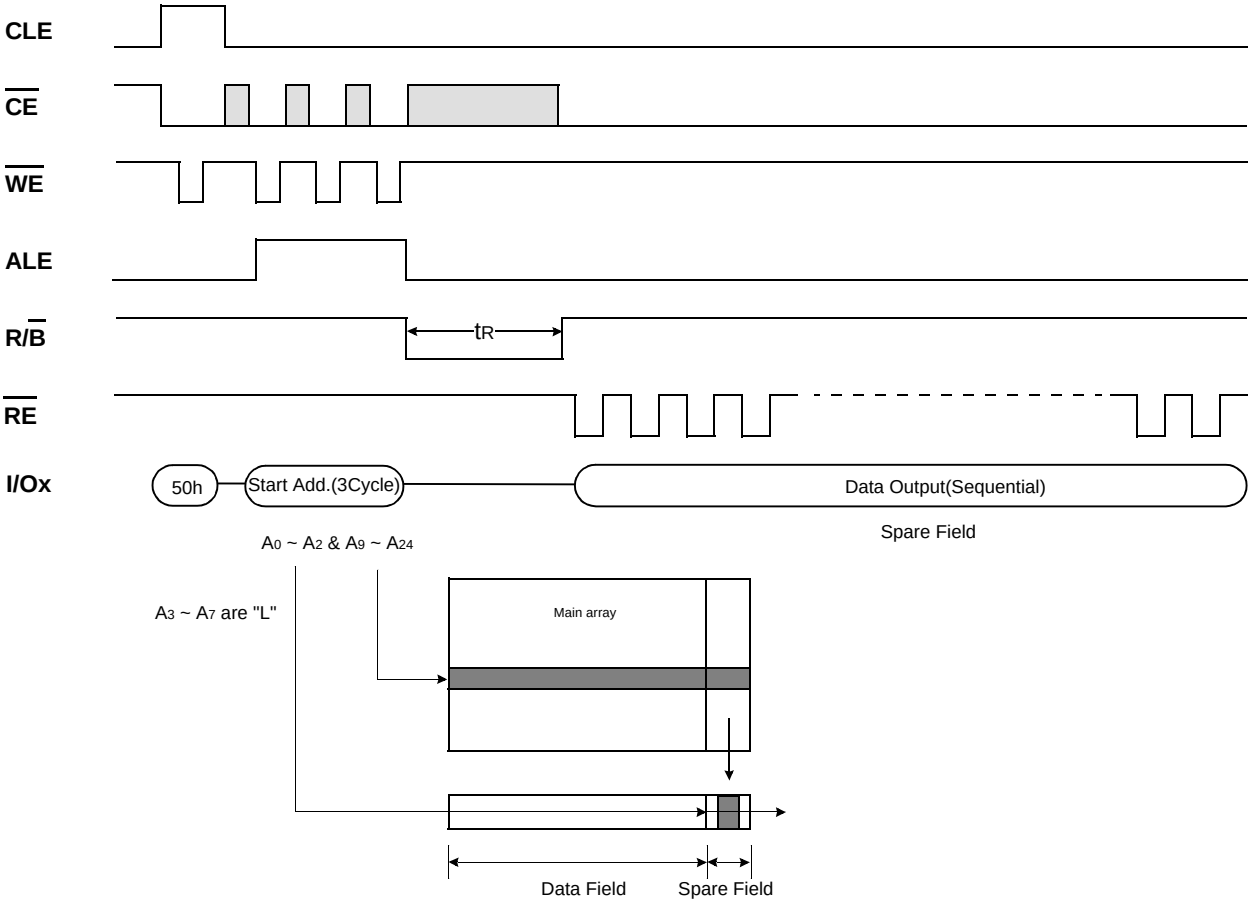
The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 256~263 words may be selectively accessed by writing the Read2 command with GND input pin low. Addresses A_0~A_2 set the starting address of the spare area while addresses A_3~A_7 must be "L". The Read1 command is needed to move the pointer back to the main area. Figures 8,9 show typical sequence and timings for each read operation.

Figure 8. Read1 Operation



NOTE: 1) After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

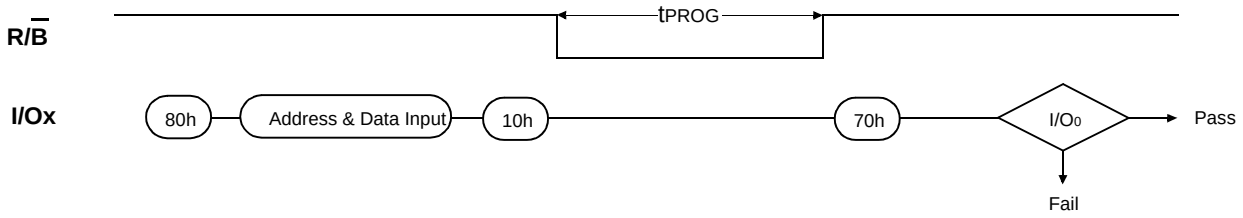
Figure 9. Read2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte/word or consecutive bytes/words up to 264, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 264 words of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The words other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 10). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

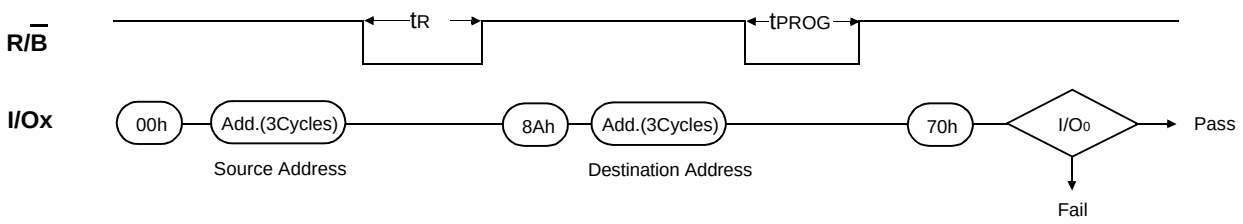
Figure 10. Program Operation



COPY-BACK PROGRAM

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the array to another page within the same array without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command with the address of the source page moves the whole 264words data into the internal buffer. As soon as the Flash returns to Ready state, copy-back programming command "8Ah" may be given with three address cycles of target page followed. The data stored in the internal buffer is then programmed directly into the memory cells of the destination page. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Since the memory array is internally partitioned into two different planes, copy-back program is allowed only within the same memory plane. Thus, A14, the plane address, of source and destination page address must be the same.

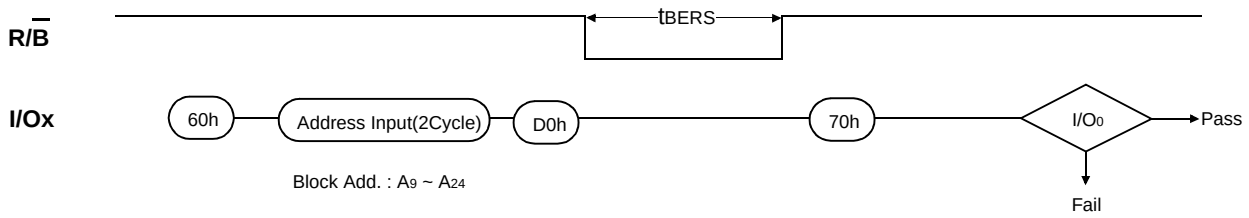
Figure 11. Copy-Back Program Operation



BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{14} to A_{24} is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 12 details the sequence.

Figure 12. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

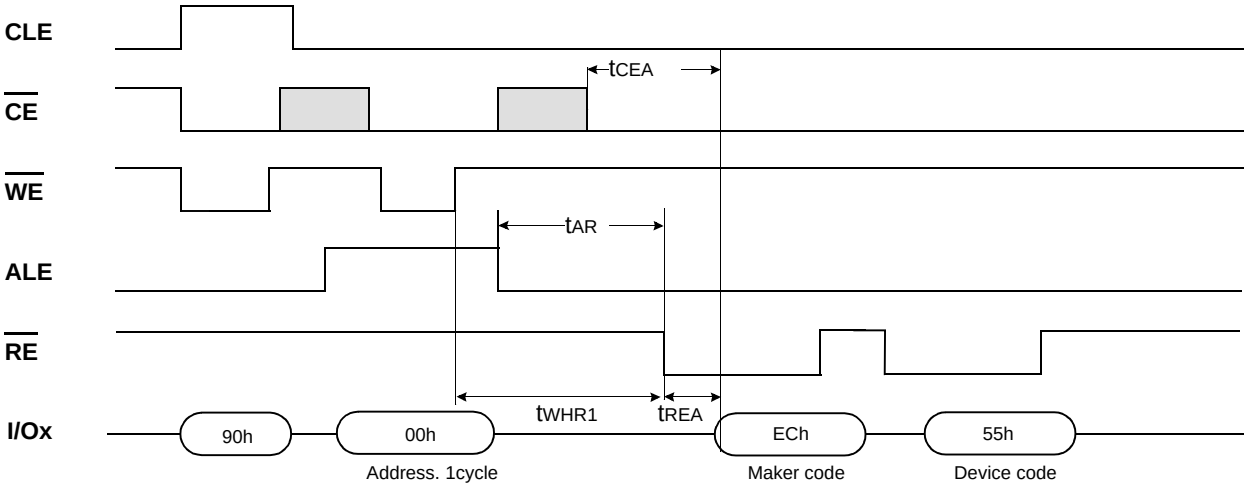
Table4. Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected
I/O 8~15	Not use	Don't care

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 13 shows the operation sequence.

Figure 13. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 5 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 14 below.

Figure 14. RESET Operation

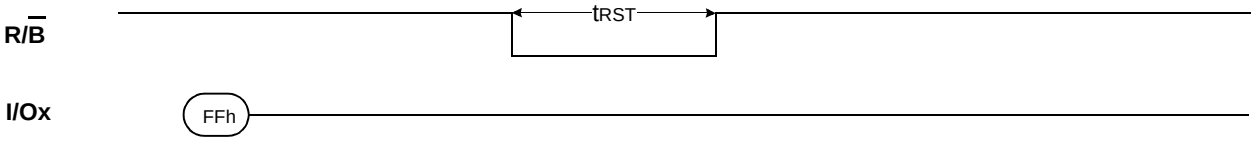


Table5. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied.

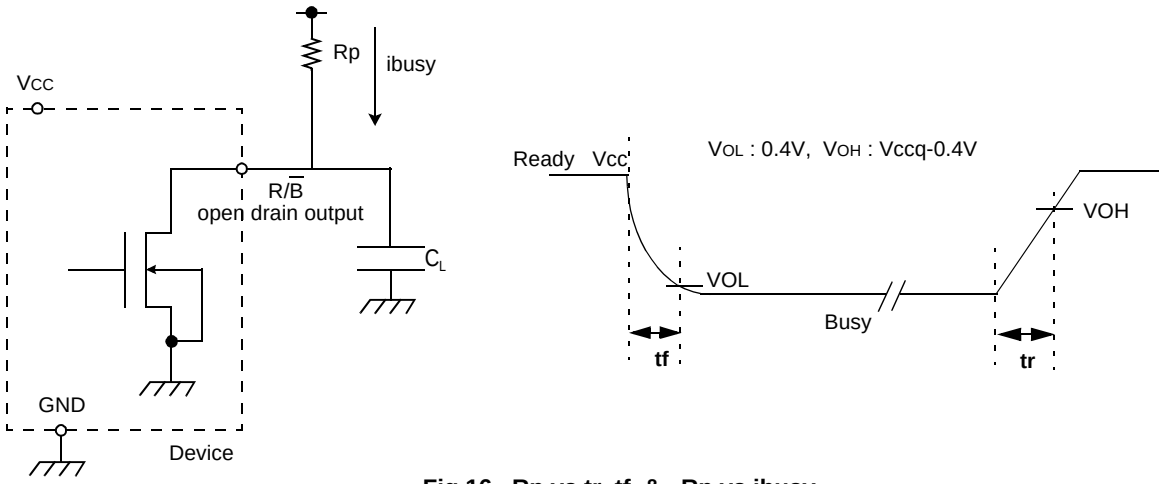
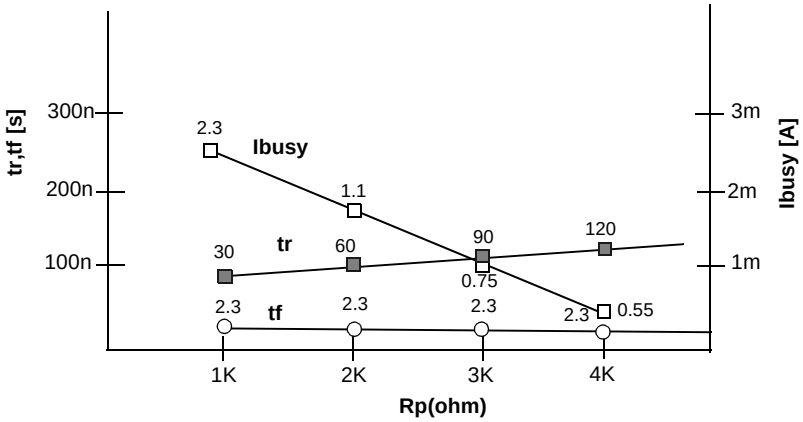


Fig 16 Rp vs tr ,tf & Rp vs ibusy

@ Vcc = 2.65V, Ta = 25°C , C_L = 30pF



Rp value guidance

$$Rp(min, 2.65V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{2.5V}{3mA + \Sigma I_L}$$

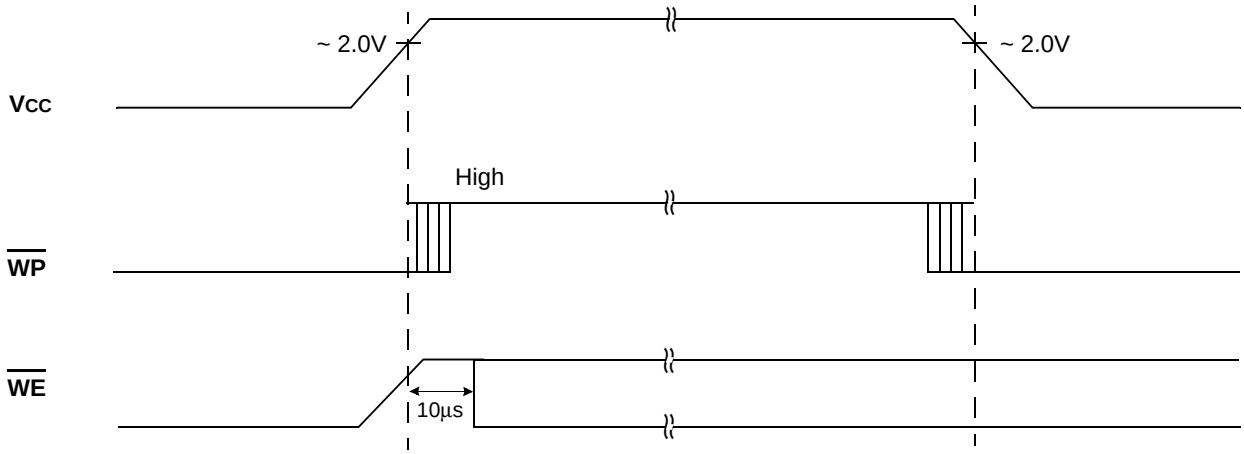
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.8V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 10μs is required before internal circuit gets ready for any command sequences as shown in Figure 17. The two step command sequence for program/erase provides additional software protection.

Figure 17. AC Waveforms for Power Transition



8M Bit(512Kx16) SRAM

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	SA	$\overline{LB}$	$\overline{UB}$	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	2)	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	2)	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	X[1]	X[1]	X[1]	X[1]	2)	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	High[3]	2)	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	High[3]	2)	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	High[3]	2)	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	High[3]	2)	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	High[3]	2)	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	High[3]	2)	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	High[3]	2)	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	High[3]	2)	L	L	Din	Din	Word Write	Active

Note: 1) X = V_{IL} or V_{IH}
2) V_{IL} or V_{IH} or Floating
3) High = CMOS level input high(same as Vcc)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions over 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.3[3)]	-	0.6	V

Note:
1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTIC

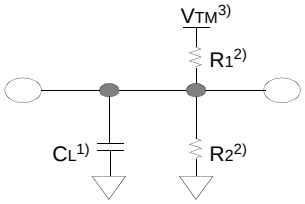
Item	Symbol	Test Conditions		Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH}, V_{IO}=Vss to Vcc		-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100%duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS_2≥Vcc-0.2V, $\overline{BYTE}$=High[2)], V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	2	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL}, $\overline{BYTE}$=High[2)], V_{IN}=V_{IL} or V_{IH}	55ns	-	-	28	mA
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current(CMOS)	I_{SB1}	Other input =0~Vcc, $\overline{BYTE}$=High[2)] 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V(CS_1 controlled) or 2) 0V≤CS_2≤0.2V(CS_2 controlled)		-	0.5	15	µA

1. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.
2. High = CMOS level input high(same as Vcc)

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(see right): C_L=30pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM} =2.8V

AC CHARACTERISTICS (Vcc=2.7~3.3V, Industrial product: T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins		Units
			55ns		
			Min	Max	
Read	Read Cycle Time	tRC	55	-	ns
	Address Access Time	tAA	-	55	ns
	Chip Select to Output	tCO	-	55	ns
	Output Enable to Valid Output	tOE	-	25	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	55	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	20	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	20	ns
	Output Disable to High-Z Output	tOHZ	0	11	ns
	Output Hold from Address Change	tOH	10	-	ns
Write	Write Cycle Time	tWC	55	-	ns
	Chip Select to End of Write	tCW	40	-	ns
	Address Set-up Time	tAS	0	-	ns
	Address Valid to End of Write	tAW	45	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	45	-	ns
	Write Pulse Width	tWP	40	-	ns
	Write Recovery Time	tWR	0	-	ns
	Write to Output High-Z	tWHZ	0	20	ns
	Data to Write Time Overlap	tDW	25	-	ns
	Data Hold from Write Time	tDH	-1	-	ns
	End Write to Output Low-Z	tOW	5	-	ns

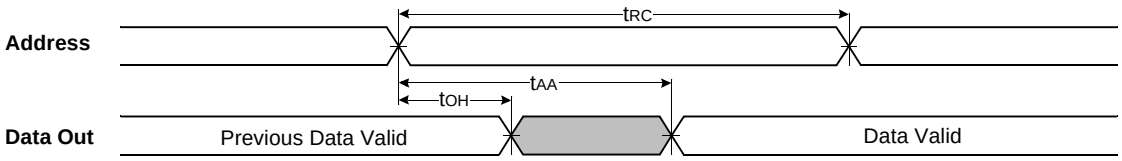
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ2)	Max	Unit
Vcc for data retention	VDR	$\overline{CS_1}$≥Vcc-0.2V1)	1.5	-	3.3	V
Data retention current	IDR	Vcc=1.5V, $\overline{CS_1}$≥Vcc-0.2V1)	-	0.5	6	µA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

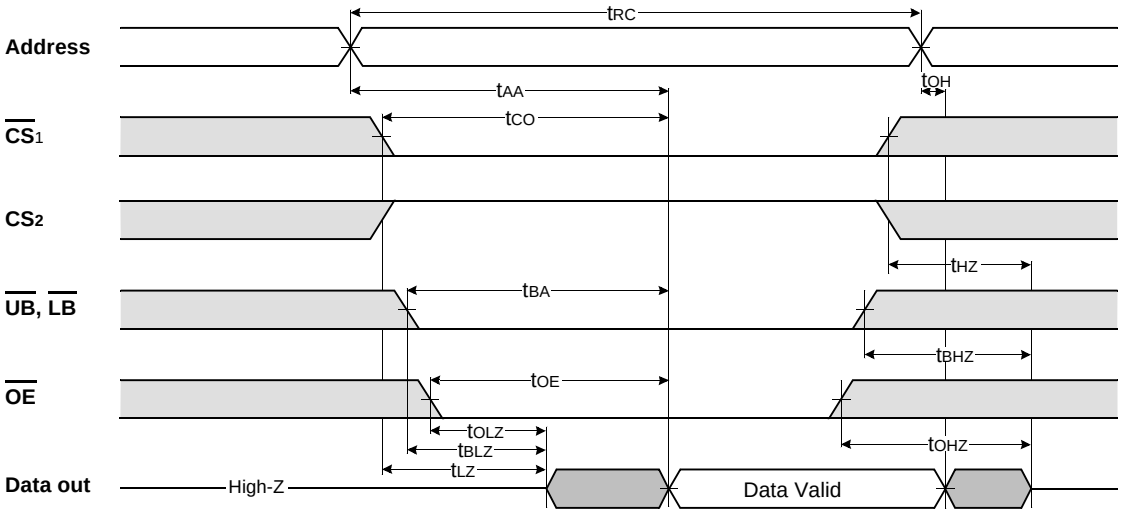
1. $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or 0≤CS_2≤0.2V(CS_2 controlled), $\overline{BYTE}$=High(CMOS level input high)
2. Typical values are measured at T_A=25°C and not 100% tested.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL}, $\overline{BYTE}$=High(CMOS level input high))



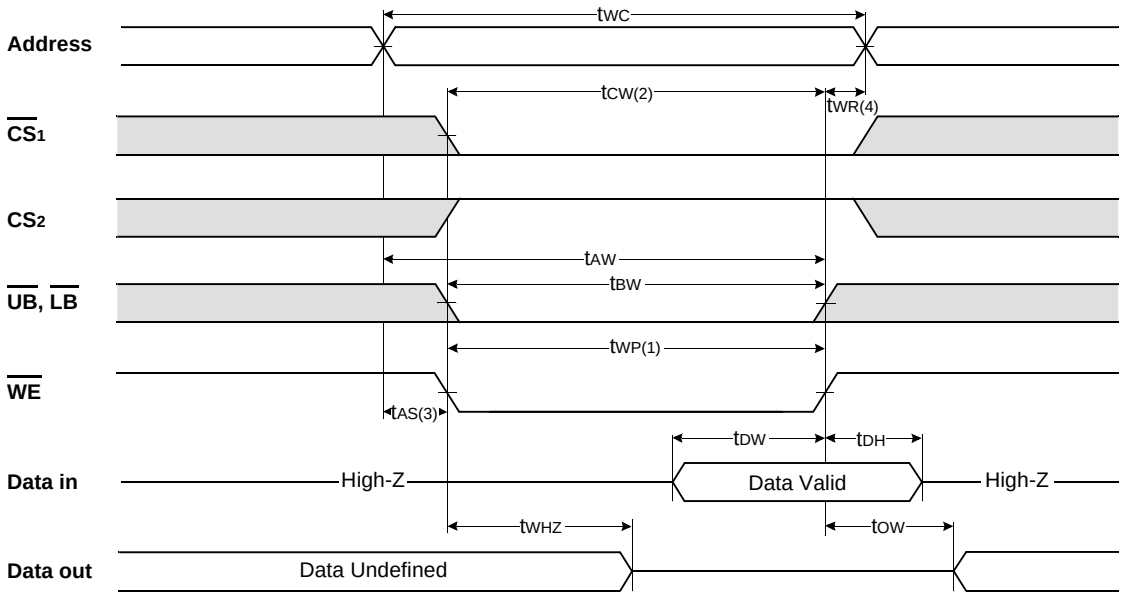
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH}, $\overline{BYTE}$=High(CMOS level input high))



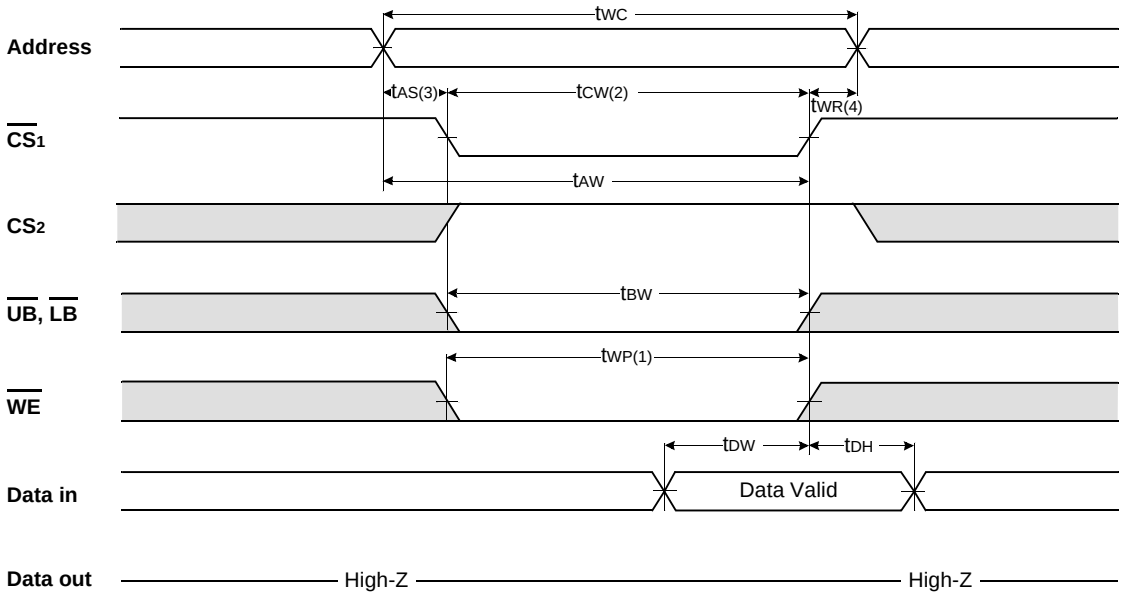
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

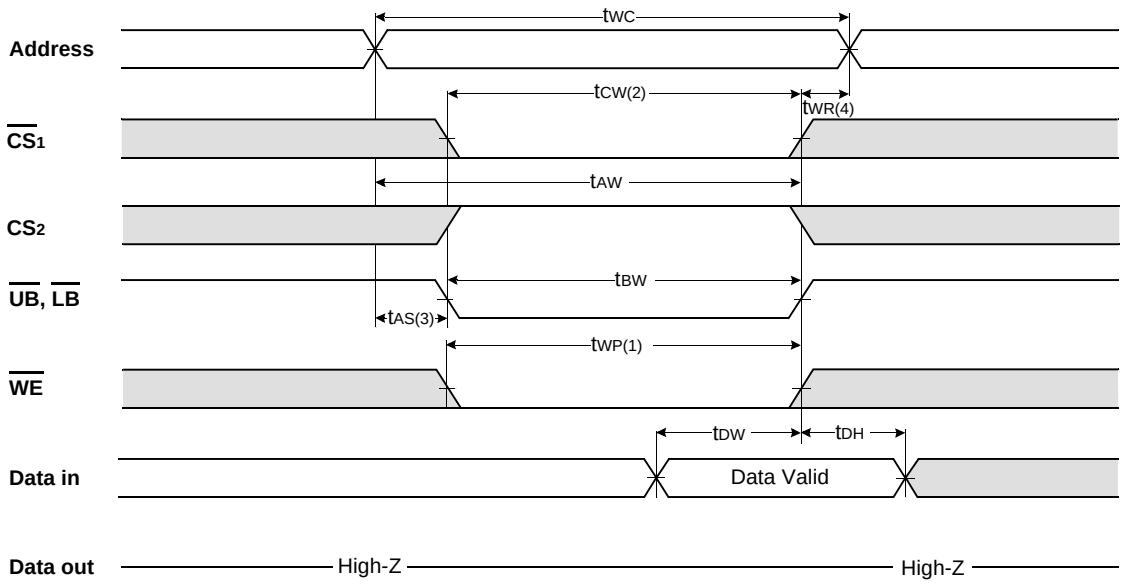
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled, $\overline{BYTE}$=High(CMOS level input high))



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled, $\overline{BYTE}$=High(CMOS level input high))



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{BYTE}$=High(CMOS level input high))

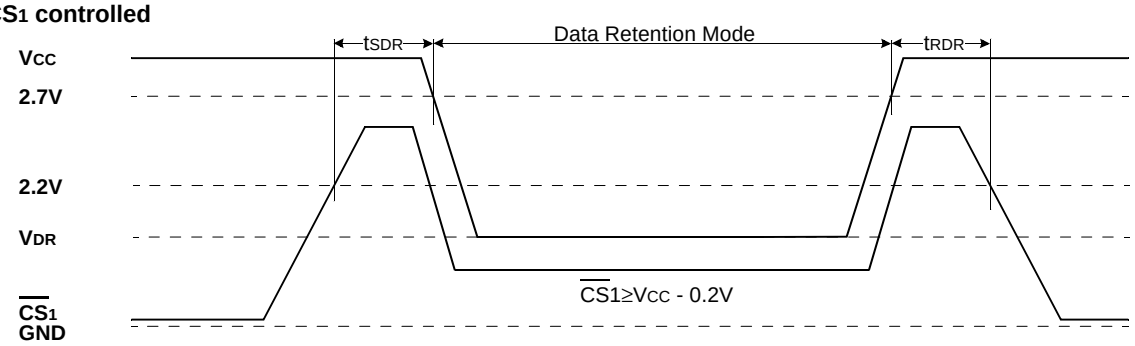


NOTES (WRITE CYCLE)

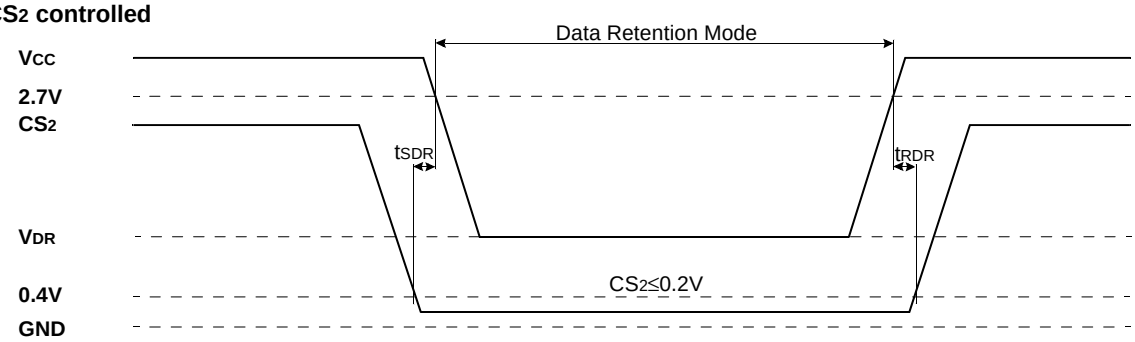
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting UB or LB for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS_2 controlled



PACKAGE DIMENSION

69-Ball FINE PITCH BGA Package (measured in millimeters)