Document Title

Multi-Chip Package MEMORY

64M Bit (4Mx16) U*t*RAM / 64M Bit (4Mx16) U*t*RAM / 8M Bit (*512Kx16*) SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft.	May 12, 2003	Preliminary
0.1	Revised - Changed ball name from Vccqs to Vccs in Pin Configuration.	July 11, 2003	Preliminary
1.0	Finalized <UtRAM> - Changed tPC from Max 25ns to Min 25ns in the AC Characteristics.	September 22, 2003	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

Multi-Chip Package MEMORY

64M Bit (4Mx16) U*t*RAM / 64M Bit (4Mx16) U*t*RAM / 8M Bit (*512Kx16*) SRAM

FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 111 - ball FBGA Type - 10 x 11mm, 0.8 mm pitch

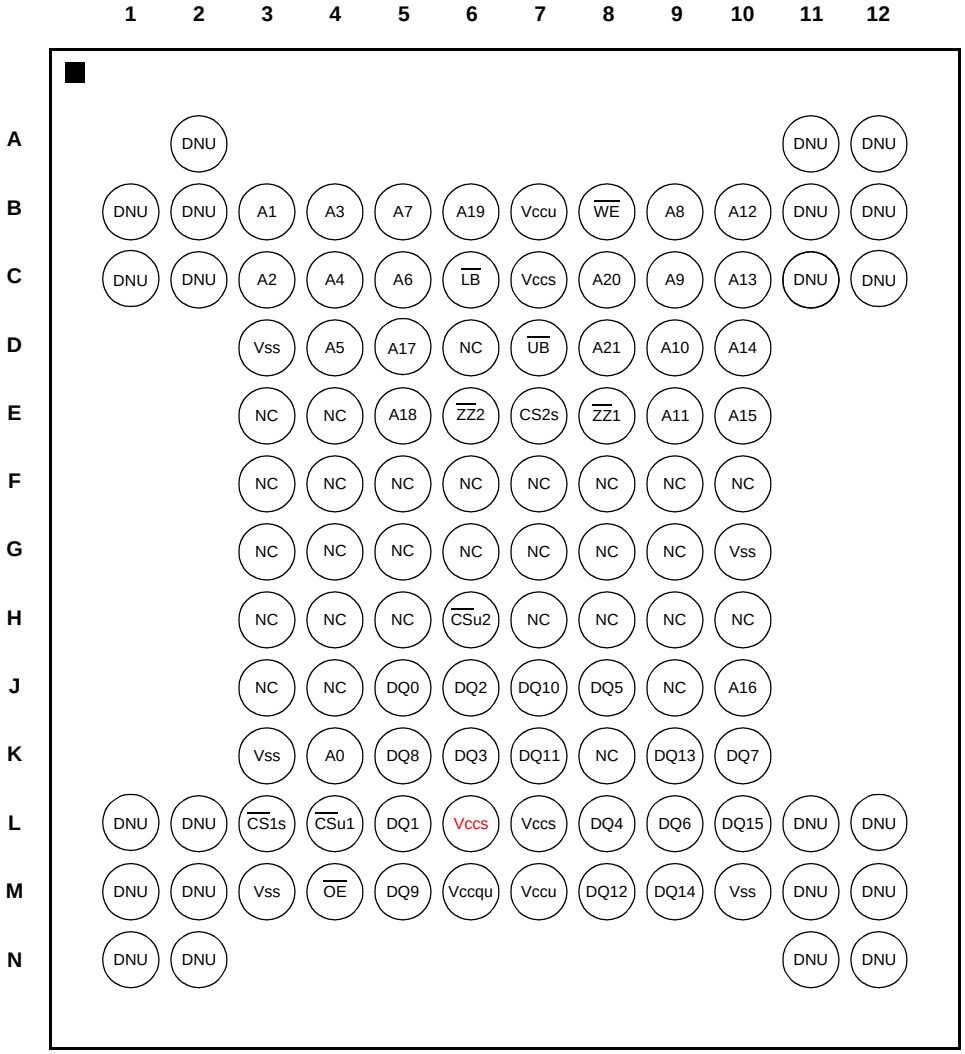
<UtRAM(each device)>
- Power Supply Voltage: 2.7~3.1V
- Organization: 4M x16 bit
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page mode (Read only)
- Deep Power Down: Memory cell data hold invalid

<SRAM>
- Process Technology: Full CMOS
- Organization: 512K x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs

GENERAL DESCRIPTION

The KAJ000A30M is a Multi Chip Package Memory which combines two 64Mbit Unit Transistor CMOS RAM and 8Mbit SRAM.
64Mbit U*t*RAM is organized as 4M x16 bit and 8Mbit SRAM is organized as 512K x16 bit.
The 64Mbit U*t*RAM is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device support page mode operation. The device also supports deep power down mode for low standby current.
The 8Mbit SRAM is fabricated by SAMSUNG′s advanced full CMOS process technology. The device supports low data retention voltage for battery back-up operation with low data retention current.
The KAJ000A30M is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption.
This device is available in 111-ball FBGA Type.

PIN CONFIGURATION



111-FBGA: Top View (Ball Down)

PIN DESCRIPTION

Ball Name	Description	Ball Name	Description
A_0 to A_{18}	Address Input Balls (UtRAM,SRAM)	$\overline{ZZ}2$	Deep Power Down (UtRAM2)
A_{19} to A_{21}	Address Input Balls (UtRAM)	$\overline{CS}u1$	Chip Select (UtRAM1)
DQ_0 to DQ_{15}	Data Input/Output Balls (UtRAM, SRAM)	$\overline{CS}u2$	Chip Select (UtRAM2)
Vccu	Power Supply (UtRAM)	$\overline{CS}1s$	Chip Select (SRAM)
Vccs	Power Supply (SRAM)	CS2s	Chip Select (SRAM)
Vccqu	Data Out Power (UtRAM)	$\overline{WE}$	Write Enable (UtRAM, SRAM)
Vss	Ground (Common)	$\overline{OE}$	Output Enable (UtRAM, SRAM)
$\overline{UB}$	Upper Byte Enable (UtRAM, SRAM)	NC	No Connection
$\overline{LB}$	Lower Byte Enable (UtRAM, SRAM)	DNU	Do Not Use
$\overline{ZZ}1$	Deep Power Down (UtRAM1)		

ORDERING INFORMATION

K A J 00 0 A 3 0 M - F LLL

Samsung
MCP(3 Chip) Memory

Device Type
U*t*RAM+U*t*RAM+SRAM

NOR Flash Density , Vcc , Org.
00 : NONE

NAND Flash Density , Vcc , Org.
0 : NONE

U*t*RAM Density , Vcc , Org.
A : 64Mbit + 64Mbit, 3.0V, x16(Page)

Access Time
L : U*t*RAM : 70ns
L : U*t*RAM : 70ns
L : SRAM : 70ns

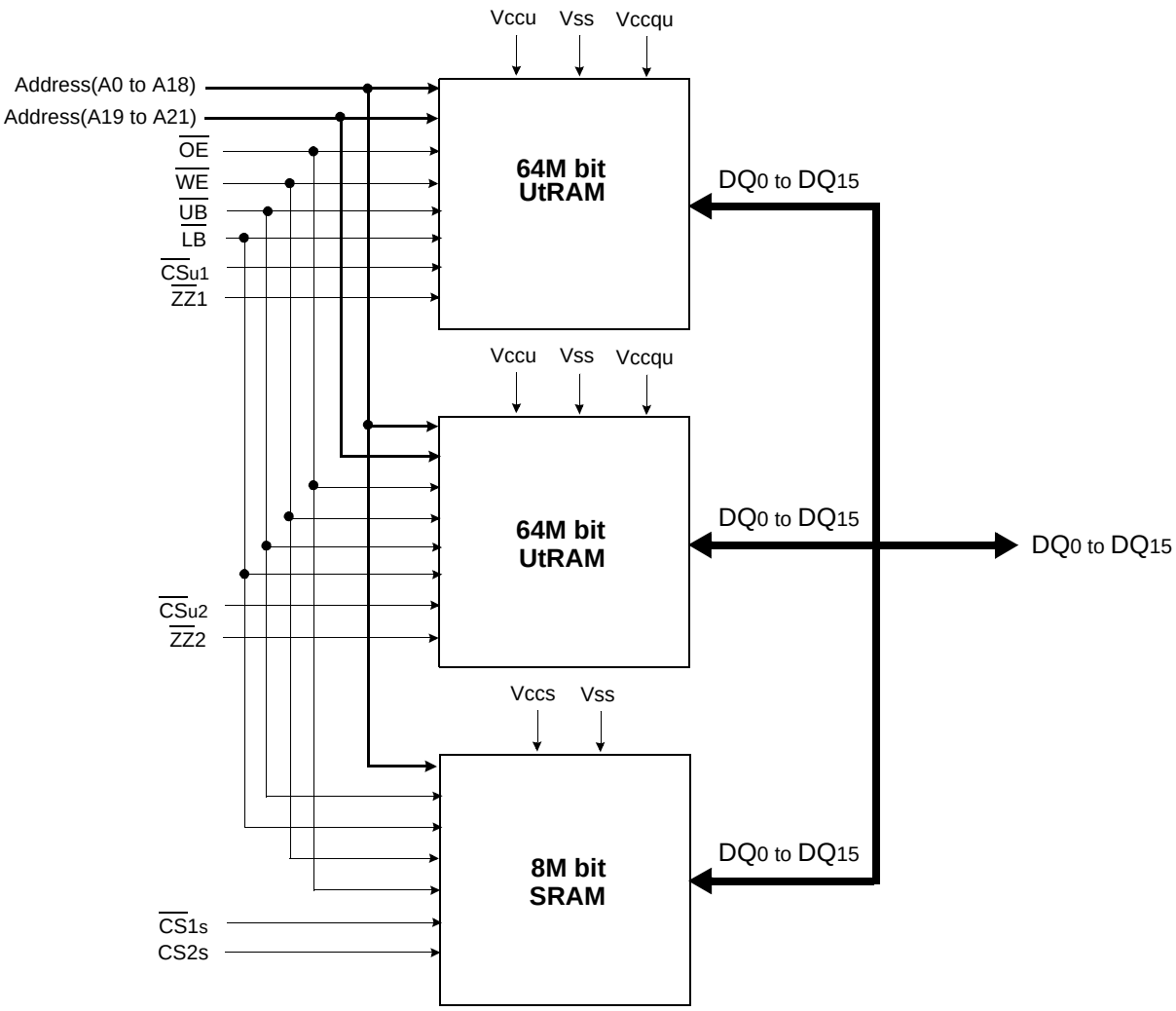
Package
F : FBGA

Version
M : 1st Generation

SDRAM Density , Vcc , Org.
0 : NONE

SRAM Density , Vcc , Org.
3 : 8Mbit, 3.0V, x16

Figure 1. FUNCTIONAL BLOCK DIAGRAM



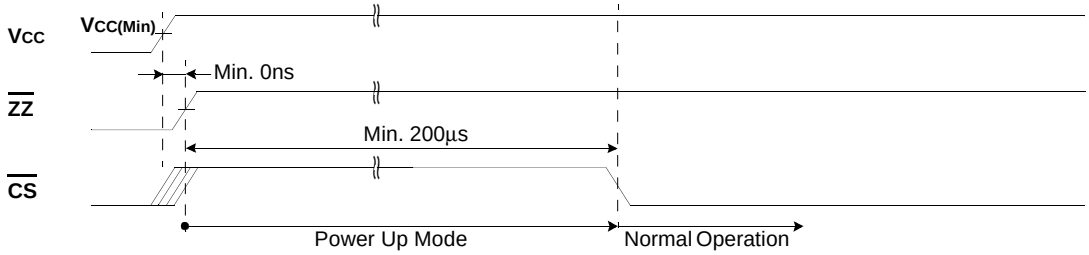
64M Bit(4Mx16)
Page Mode UtRAM

For Each Device

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minimum 200µs with $\overline{CS}$ and $\overline{ZZ}$ high.

TIMING WAVEFORM OF POWER UP



(POWER UP)

1. After V_{CC} reaches V_{CC}(Min.), wait 200µs with $\overline{CS}$ and $\overline{ZZ}$ high. Then you get into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Deep Power Down
L	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

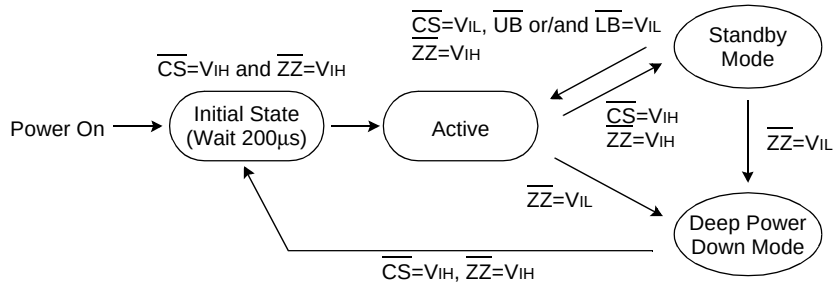
1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

STANDBY MODE STATE MACHINES



STANDBY MODE CHARACTERISTIC

Power Mode	Memory Cell Data	Standby Current(μA)	Wait Time(μs)
Standby	Valid	120	0
Deep Power Down	Invaild	20	200

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	2.9	3.1	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{ZZ}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	15	mA
	I_{CC2}	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{ZZ}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	45	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, $\overline{ZZ}$≥Vcc-0.2V, Other inputs=Vss to Vcc	-	-	120	µA
Deep Power Down	I_{SBD}	$\overline{ZZ}$≤0.2V, Other inputs=Vss to Vcc	-	-	20	µA

1. Typical values are tested at V_{CC}=2.9V, T_A=25°C and not guaranteed.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load: C_L=50pF

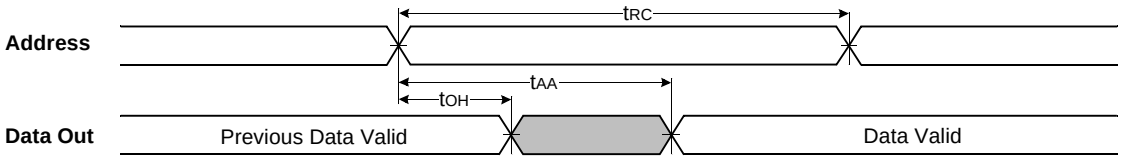
AC CHARACTERISTICS(V_{CC}=2.7~3.1V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	ns
	Page Cycle	t_{PC}	25	-	ns
	Page Access Time	t_{PA}	-	20	ns
Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns

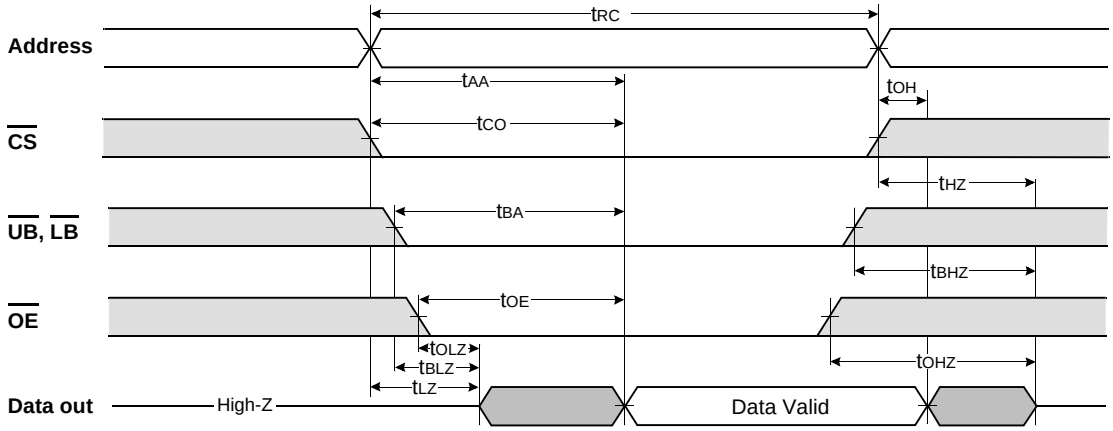
1. t_{WP}(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

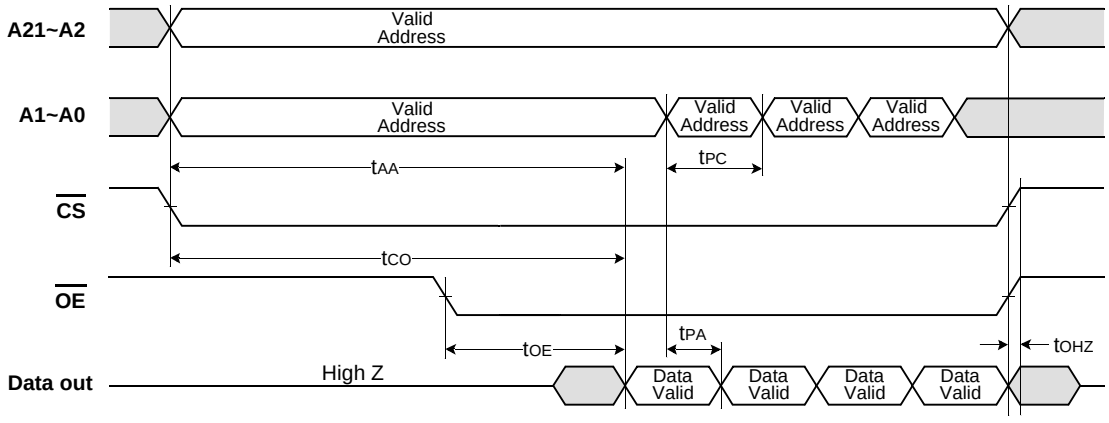
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{ZZ}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=V_{IH})



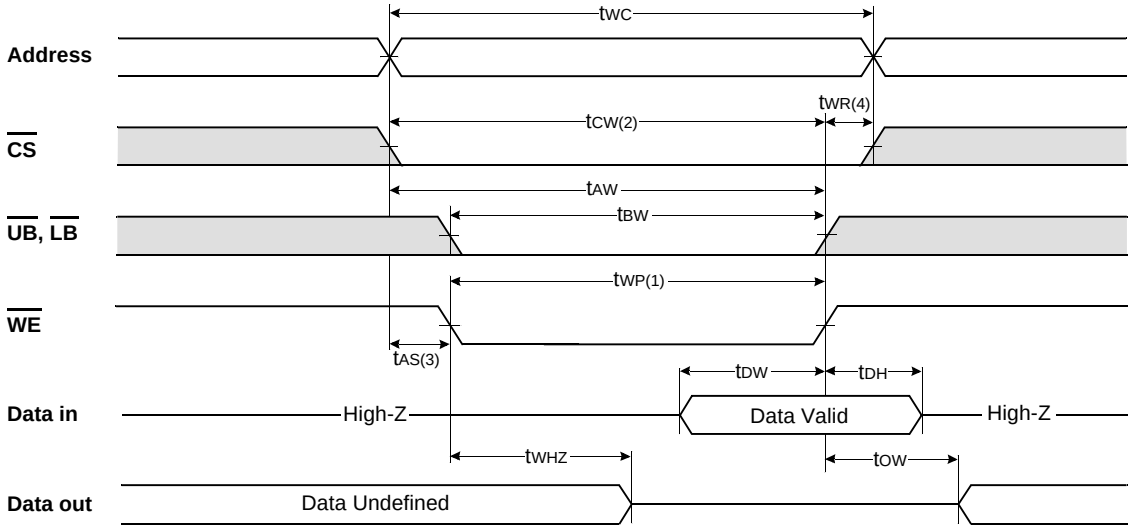
TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)



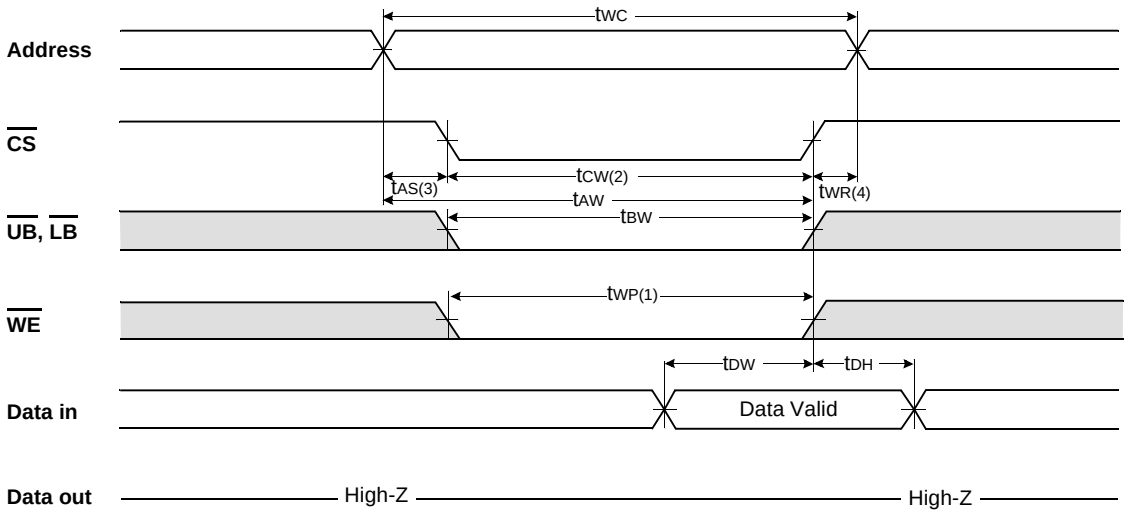
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.

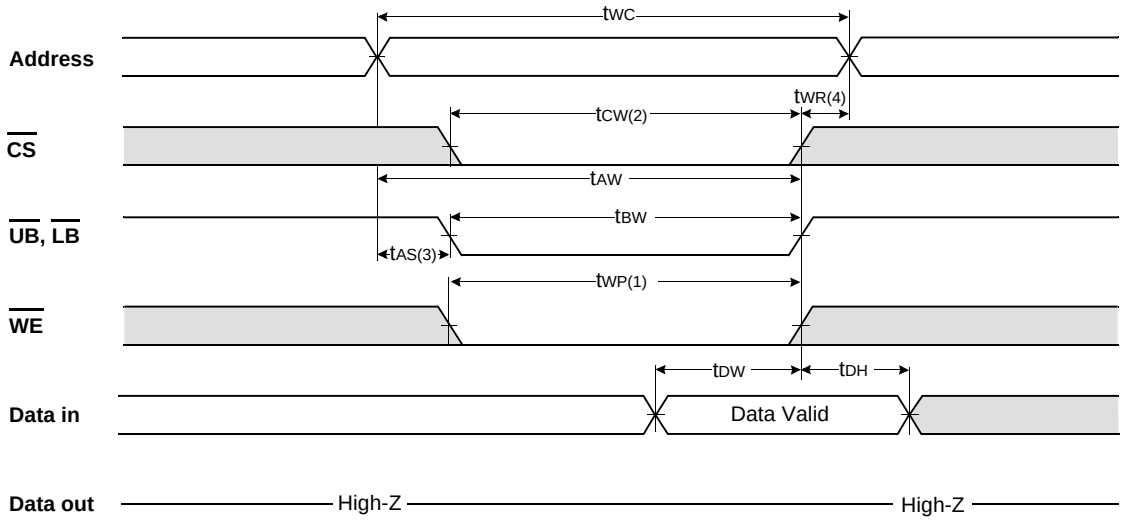
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{ZZ}$=V_{IH})



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled, $\overline{ZZ}$=V_{IH})



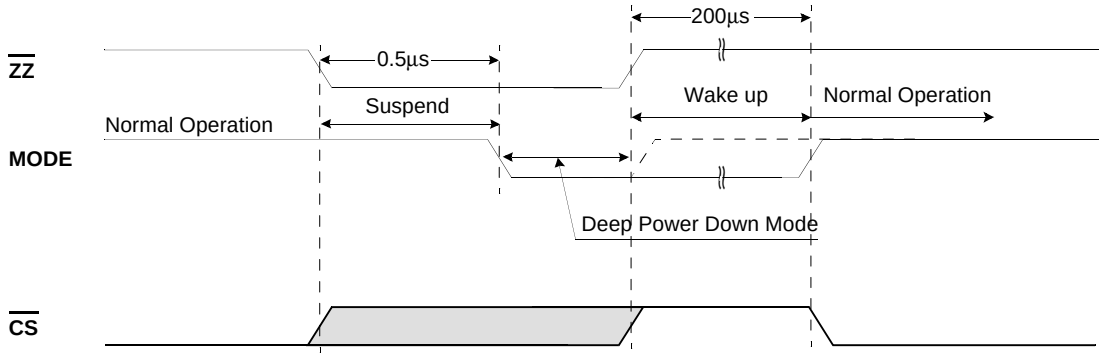
TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}$=V_{IH})



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

TIMING WAVEFORM OF DEEP POWER DOWN MODE ENTRY AND EXIT



(DEEP POWER DOWN MODE)

1. When you toggle $\overline{ZZ}$ pin low, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power Up sequence.

8M Bit(512Kx16) SRAM

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
X[1)]	X[1)]	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1)]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1)]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1)]	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions over 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

Note:
1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTIC

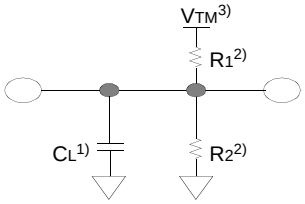
Item	Symbol	Test Conditions		Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH}, V_{IO}=Vss to Vcc		-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100%duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS_2≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	5	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}	70ns	-	-	30	mA
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current(CMOS)	I_{SB1}	Other input =0~Vcc 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or 2) 0V≤CS_2≤0.2V(CS_2 controlled)		-	-	25	µA

1. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(see right): C_L=100pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM} =2.8V

AC CHARACTERISTICS (Vcc=2.7~3.3V, Industrial product: T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	ns
	Output Hold from Address Change	t_{OH}	10	-	ns
Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	50	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	20	ns
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	ns

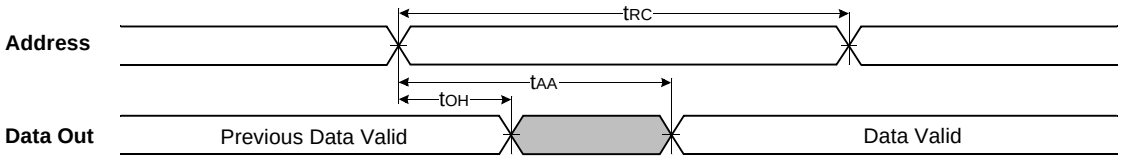
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ2)	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1}$≥Vcc-0.2V1)	1.5	-	3.3	V
Data retention current	I_{DR}	Vcc=1.5V, $\overline{CS_1}$≥Vcc-0.2V1)	-	-	15	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		tRC	-	-	

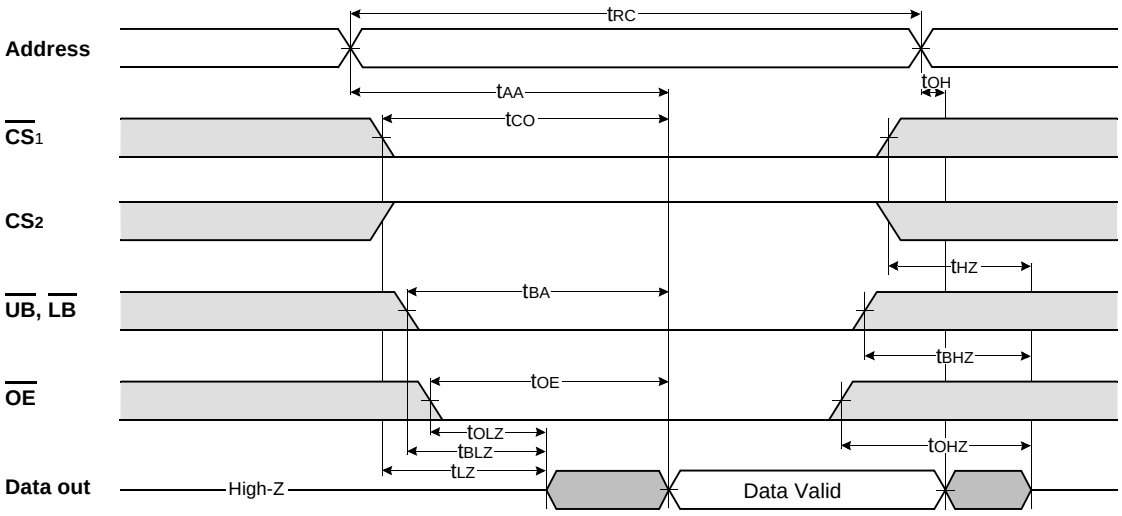
1. 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or
   2) 0≤CS_2≤0.2V(CS_2 controlled)
2. Typical values are measured at T_A=25°C and not 100% tested.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



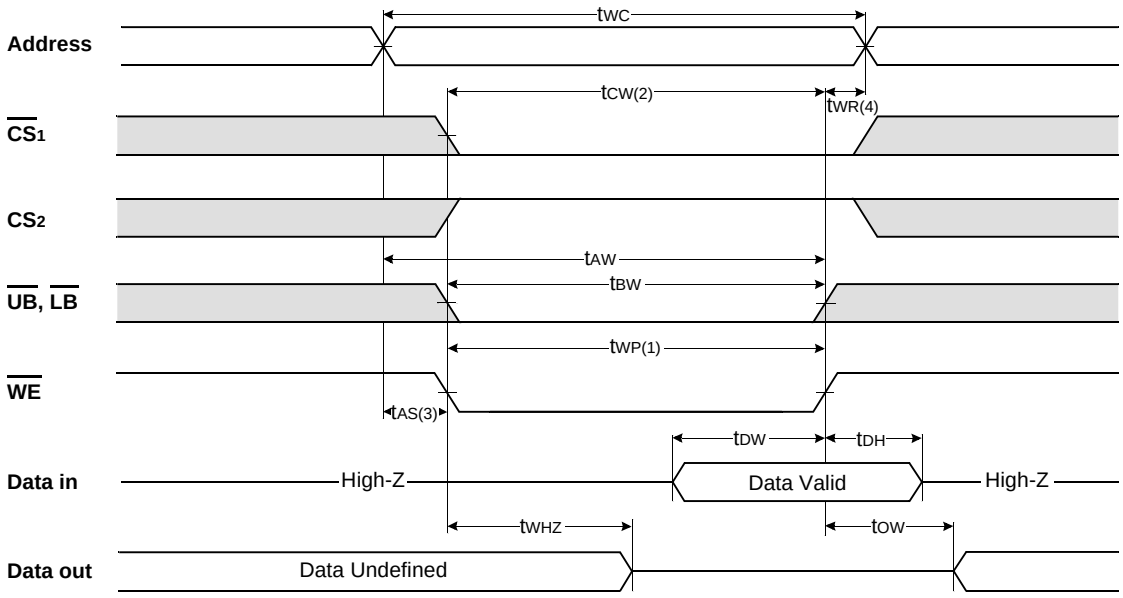
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



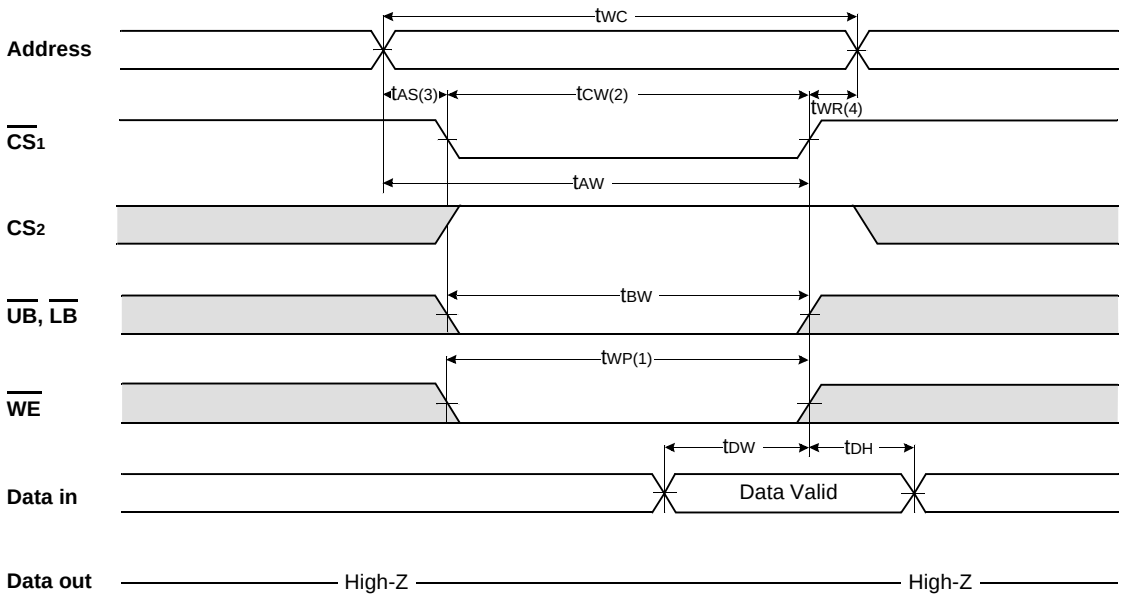
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

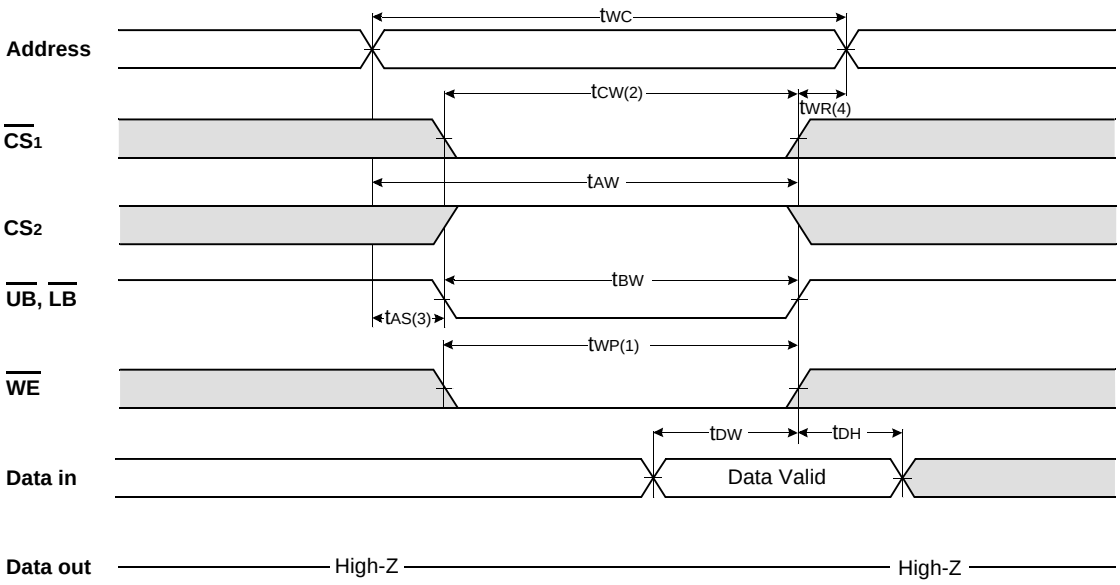
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

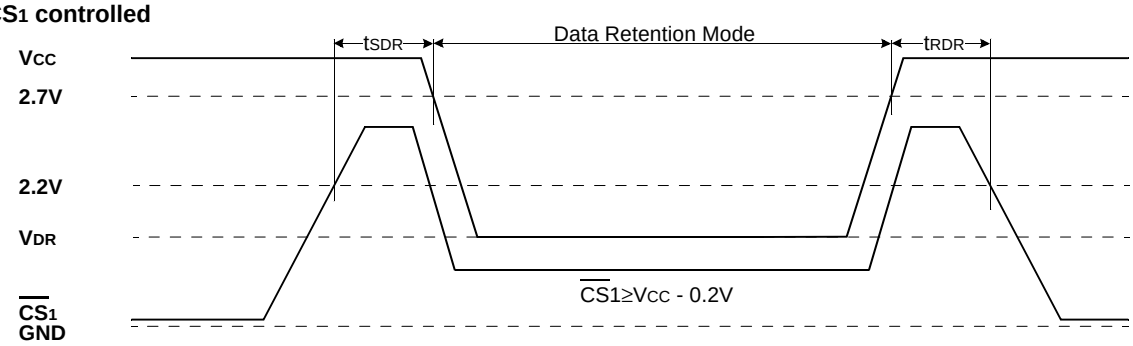


NOTES (WRITE CYCLE)

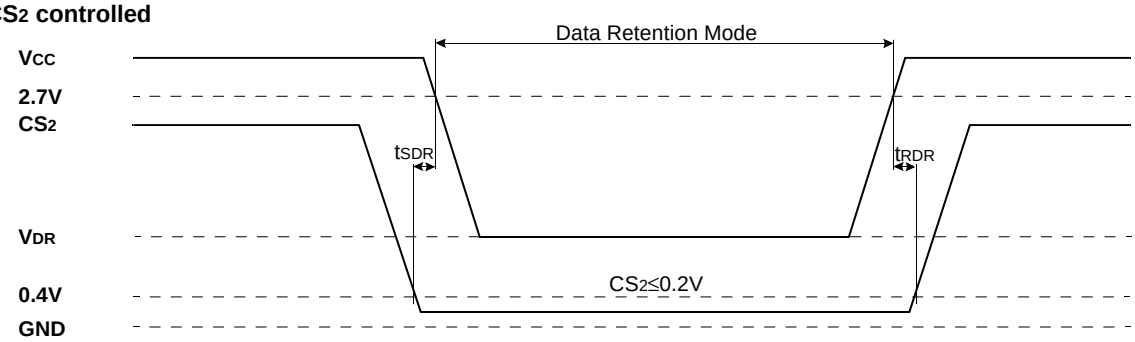
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting UB or LB for single byte operation or simultaneously asserting UB and LB for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS_2 controlled



PACKAGE DIMENSION

111-Ball FINE PITCH BGA Package (measured in millimeters)