4Mx16
Mobile SDRAM
52CSP

(VDD/VDDQ 2.5V/1.8V or 2.5V/2.5V)

Revision 1.4

December 2002

1M x 16Bit x 4 Banks SDRAM in 52CSP

FEATURES

- 2.5V power supply.
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - -. CAS latency (1 & 2 & 3).
  - -. Burst length (1, 2, 4, 8 & Full page).
  - -. Burst type (Sequential & Interleave).
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- DQM for masking.
- Auto refresh.
- 64ms refresh period (4K cycle).
- Commercial Temperature Operation (-25°C ~ 70°C).
  Extended Temperature Operation (-25°C ~ 85°C).
  Industrial Temperature Operation (-40°C ~ 85°C).
- 52Balls CSP(GXXX - Pb, AXXX - Pb Free)

GENERAL DESCRIPTION

The K4S64163LF is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

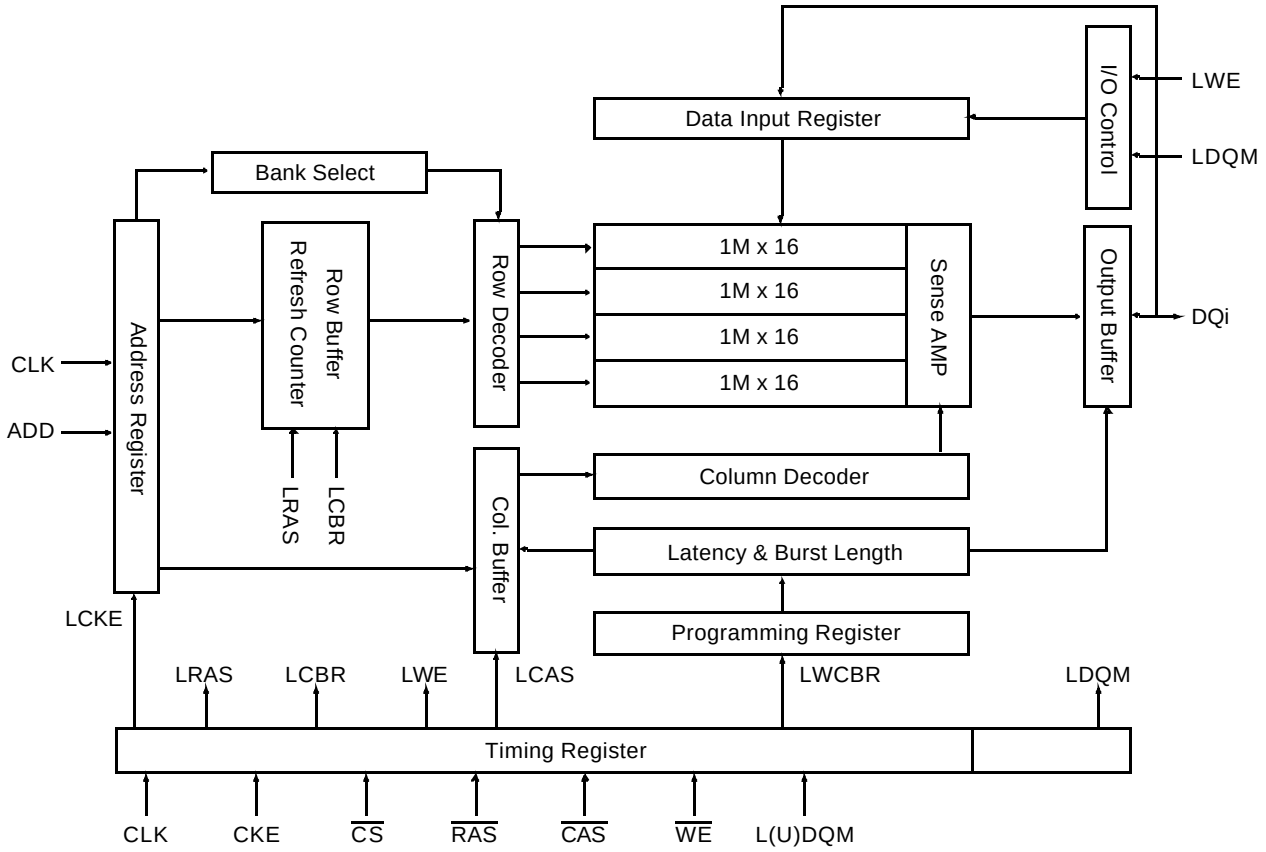
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S64163LF-G(A)L/N/P75	133MHz(CL=3) 105MHz(CL=2)	LVCMOS	52 CSP Pb (Pb Free)
K4S64163LF-G(A)L/N/P1H	105MHz(CL=2)		
K4S64163LF-G(A)L/N/P1L	105MHz(CL=3)*1		
K4S64163LF-G(A)L/N/P15	66MHz(CL=2/3)*2		

-G(A)L ; Low Power, Operating Temp : -25°C ~ 70°C.
-G(A)N ; Low Power, Operating Temp : -25°C ~ 85°C
-G(A)P : Low Power, Operating Temp : -40°C ~ 85°C.

Notes :
1. In case of 40MHz Frequency, CL1 can be supported.
2. In case of 33MHz Frequency, CL1 can be supported.

FUNCTIONAL BLOCK DIAGRAM



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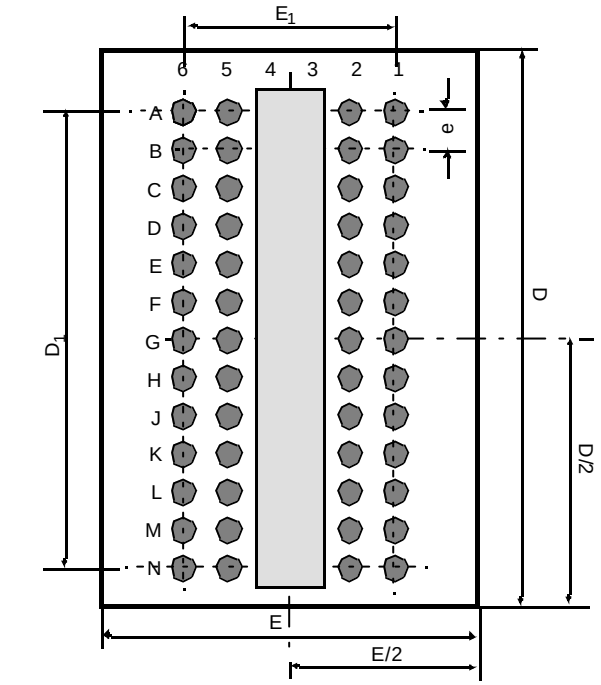
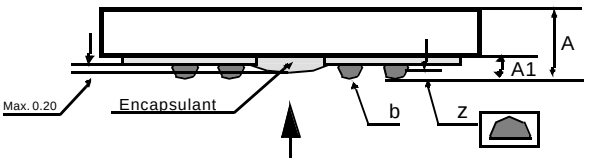
Package Dimension and Pin Configuration

< Bottom View*1 >

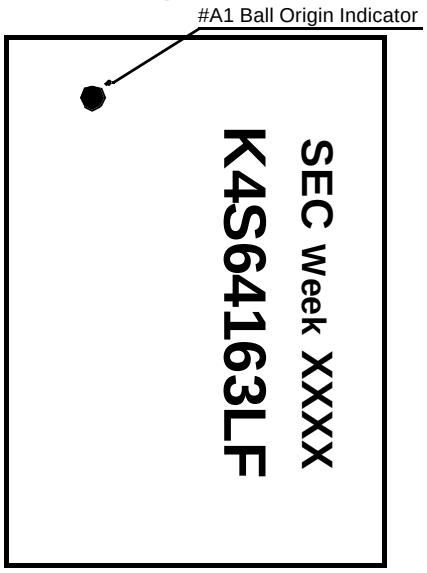


*2: Top View



*1: Bottom View

< Top View*2 >



< Top View*2 >

52Ball(4x13) CSP				
	1	2	5	6
A	Vss	DQ15	DQ0	VDD
B	DQ14	VSSQ	VDDQ	DQ1
C	DQ13	VDDQ	VSSQ	DQ2
D	DQ12	DQ11	DQ4	DQ3
E	DQ10	VSSQ	VDDQ	DQ5
F	DQ9	VDDQ	VSSQ	DQ6
G	DQ8	VDD	Vss	DQ7
H	CLK	UDQM	LDQM	$\overline{WE}$
J	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$
K	A11	A9	BA1	BA0
L	A8	A7	A0	A10
M	A6	A5	A2	A1
N	Vss	A4	A3	VDD

Pin Name	Pin Function
CLK	*System Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A_0 ~ A_{11}	*Address*
BA_0 ~ BA_1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
L(U)DQM	*Data Input/Output Mask*
DQ_0 ~ $_{15}$	*Data Input/Output*
VDD/VSS	*Power Supply/Ground*
VDDQ/VSSQ	*Data Output Power/Ground*

[Unit:mm]

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
A_1	-	0.35	-
E	-	6.60	-
E_1	-	3.75	-
D	-	11.00	-
D_1	-	9.0	-
e	-	0.75	-
b	0.40	0.45	0.5
z	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Notes:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A =Commercial, Extended, Industrial Temperature)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	2.3	2.5	2.7	V	
	V_{DDQ}	1.65	-	2.7	V	
Input logic high voltage	V_{IH}	0.8 x VDDQ	-	V_{DDQ} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V_{OH}	VDDQ - 0.2V	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.2	V	I_{OL} = 0.1mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes:
1. V_{IH} (max) = 3.0V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -1.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 2.5V, T_A = 23°C, f = 1MHz, V_{REF} =0.9V ± 50mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.0	4.0	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.0	4.0	pF	
Address	C_{ADD}	2.0	4.0	pF	
DQ_0 ~ DQ_{15}	C_{OUT}	3.5	6.0	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A =Commercial, Extended, Industrial Temperature)

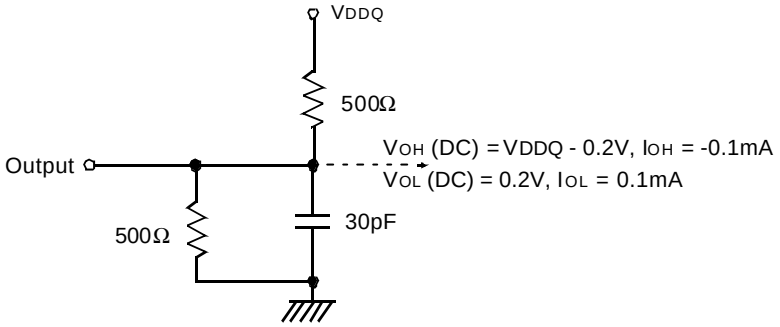
Parameter	Symbol	Test Condition		Version				Unit	Note
				-75	-1H	-1L	-15		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		50	50	45	40	mA	1
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns		0.5				mA	
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		0.5					
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		10				mA	
	$I_{CC2}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		7					
Active Standby Current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5				mA	
	$I_{CC3}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		5					
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20				mA	
	$I_{CC3}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		20				mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		80	65	65	55	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		115	110	100	80	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	-G(A)L	400				uA	3
			-G(A)N						4
			-G(A)P						5

Notes :

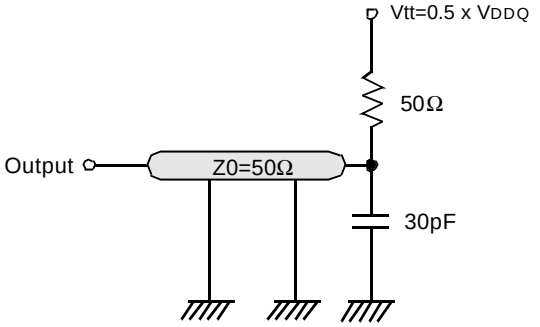
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S64163LF-G(A)L**
4. K4S64163LF-G(A)N**
5. K4S64163LF-G(A)P**
6. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 2.5V ± 0.2V, T_A =Commercial, Extended, Industrial Temperature)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.9 x VDDQ / 0.2	V
Input timing measurement reference level	0.5 x VDDQ	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			- 75	-1H	-1L	-15		
Row active to row active delay		tRRD(min)	15	19	19	30	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	19	19	24	30	ns	1
Row precharge time		tRP(min)	19	19	24	30	ns	1
Row active time		tRAS(min)	45	50	60	60	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	65	70	84	90	ns	1
Last data in to row precharge		tRDL(min)	2				CLK	2,3
Last data in to Active delay		tDAL(min)	tRDL + tRP				ns	3
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	4
Number of valid output data	CAS latency=3		2				ea	5
	CAS latency=2		1					
	CAS latency=1		-		0			

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum tRDL=2CLK and tDAL(=tRDL + tRP) is required to complete both of last data wite command(tRDL) and precharge command(tRP). tRDL=1CLK can be supported only in the case under 100MHz with manual precharge mode.
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-1H		-1L		-15		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	9.5	1000	9.5	1000	15	1000	ns	1
	CAS latency=2		9.5		9.5		12		15			
	CAS latency=1		-		-		25		30			
CLK to valid output delay	CAS latency=3	tSAC		5.4		7		7		9	ns	1,2
	CAS latency=2			7		7		8		9		
	CAS latency=1			-		-		20		24		
Output data hold time	CAS latency=3	tOH	2.5		2.5		2.5		2.5		ns	2
	CAS latency=2		2.5		2.5		2.5		2.5			
	CAS latency=1		-		-		2.5		2.5			
CLK high pulse width		tCH	2.5		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3.5		ns	3
Input setup time		tSS	2.0		2.5		2.5		3.5		ns	3
Input hold time		tSH	1.0		1.5		1.5		2.0		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		7		7		9	ns	
	CAS latency=2			7		7		8		9		
	CAS latency=1			-		-		20		24		

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Note :

1. Samsung are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in samsung electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

SIMPLIFIED TRUTH TABLE (V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Note :

1. OP Code : Operand Code
   $A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).