

512Mb B-die DDR400 SDRAM Specification

60Ball FBGA

Revision 0.0

512Mb B-die Revision History

Revision 0.0 (September, 2003)

- First version for internal review

DDR SDRAM 512Mb B-die (x4, x8, x16)

Key Features

- 200MHz Clock, 400Mbps data rate.
- VDD= +2.6V $\pm$ 0.10V, VDDQ= +2.6V $\pm$ 0.10V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
 - . Read latency 3 (clock) for DDR400 , 2.5 (clock) for DDR333
 - . Burst length (2, 4, 8)
 - . Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe
- Edge aligned data output, center aligned data input
- LDM,UDM for write masking only (x16)
- DM for write masking only (x4,x8)
- Auto & Self refresh
- 7.8us refresh interval(8K/64ms refresh)
- Maximum burst refresh cycle : 8
- 60Ball FBGA package

Ordering Information

Part No.	Org.	Max Freq.	Interface	Package
K4H510438B-GCCC	128M x 4	CC(DDR400@CL=3)	SSTL2	60 FBGA
K4H510838B-GCCC	64M x 8	CC(DDR400@CL=3)	SSTL2	60 FBGA
K4H511638B-GCCC	32M x 16	CC(DDR400@CL=3)	SSTL2	60 FBGA

Operating Frequencies

	CC(DDR333@CL=3)
Speed @CL3	200MHz
CL-tRCD-tRP	3-3-3

*CL : CAS Latency

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Ball Description (**Bottom View**)

128M x 4

1	VSSQ	NC	NC	NC	NC	VREF						
2	NC	VDDQ	VSSQ	VDDQ	VSSQ	VSS	CK	A12	A11	A8	A6	A4
3	VSS	DQ3	NC	DQ2	DQS	DM	$\overline{\text{CK}}$	CKE	A9	A7	A5	VSS
	A	B	C	D	E	F	G	H	J	K	L	M
7	VDD	DQ0	NC	DQ1	NC	NC	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	BA1	A0	A2	VDD
8	NC	VSSQ	VDDQ	VSSQ	VDDQ	VDD	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	BA0	A10/AP	A1	A3
9	VDDQ	NC	NC	NC	NC	NC						

64M x 8

1	VSSQ	NC	NC	NC	NC	VREF						
2	DQ7	VDDQ	VSSQ	VDDQ	VSSQ	VSS	CK	A12	A11	A8	A6	A4
3	VSS	DQ6	DQ5	DQ4	DQS	DM	$\overline{\text{CK}}$	CKE	A9	A7	A5	VSS
	A	B	C	D	E	F	G	H	J	K	L	M
7	VDD	DQ1	DQ2	DQ3	NC	NC	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	BA1	A0	A2	VDD
8	DQ0	VSSQ	VDDQ	VSSQ	VDDQ	VDD	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	BA0	A10/AP	A1	A3
9	VDDQ	NC	NC	NC	NC	NC						

32M x 16

1	VSSQ	DQ14	DQ12	DQ10	DQ8	VREF						
2	DQ15	VDDQ	VSSQ	VDDQ	VSSQ	VSS	CK	A12	A11	A8	A6	A4
3	VSS	DQ13	DQ11	DQ9	UDQS	UDM	$\overline{\text{CK}}$	CKE	A9	A7	A5	VSS
	A	B	C	D	E	F	G	H	J	K	L	M
7	VDD	DQ2	DQ4	DQ6	LDQS	LDM	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	BA1	A0	A2	VDD
8	DQ0	VSSQ	VDDQ	VSSQ	VDDQ	VDD	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	BA0	A10/AP	A1	A3
9	VDDQ	DQ1	DQ3	DQ5	DQ7	NC						

Organization	Row Address	Column Address
128Mx4	A0~A12	A0-A9, A11, A12
64Mx8	A0~A12	A0-A9, A11
32Mx16	A0~A12	A0-A9

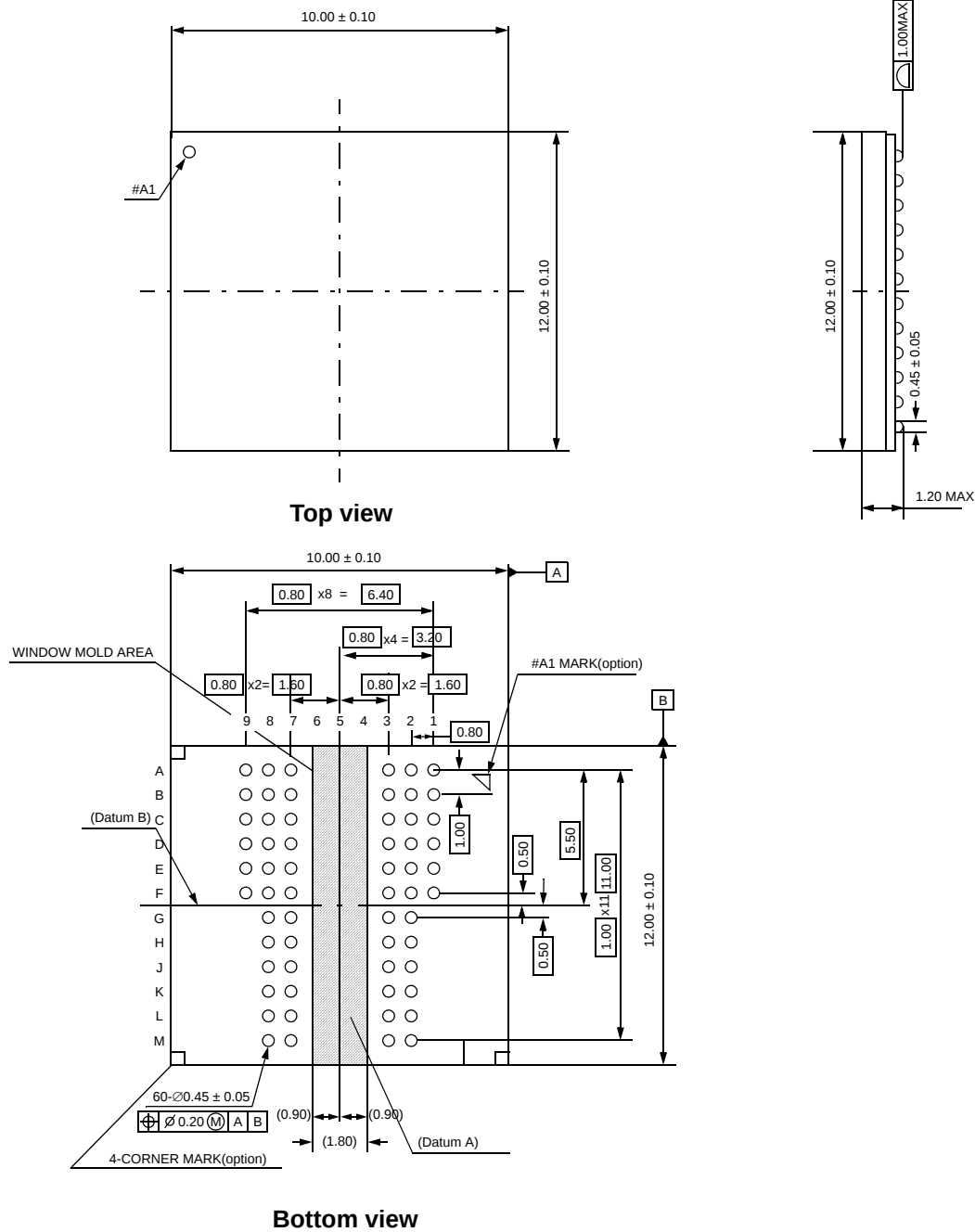
DM is internally loaded to match DQ and DQS identically.

Row & Column address configuration

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Package Physical Dimension (Unit : mm)



60Ball FBGA 512Mb Package Dimension

The diagram illustrates the internal architecture of the Data Input Register (DQI). At the bottom, a **Timing Register** and a **DM Input Register** receive external control signals: $\overline{\text{CK}}$, $\overline{\text{CK}}$, $\overline{\text{CKE}}$, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{LDM}}$. The **Timing Register** outputs $\overline{\text{LCKE}}$, $\overline{\text{LRAS}}$, $\overline{\text{LCBR}}$, $\overline{\text{LWE}}$, $\overline{\text{LCAS}}$, $\overline{\text{LWCBR}}$, and $\overline{\text{CK}}$, $\overline{\text{CK}}$. The **DM Input Register** outputs $\overline{\text{CK}}$, $\overline{\text{CK}}$ and $\overline{\text{LDM}}$. The $\overline{\text{CK}}$, $\overline{\text{CK}}$ signals are distributed to the **Address Register**, **Bank Select**, **Refresh Counter Row Buffer**, **Row Decoder**, **Col. Buffer**, **Data Input Register**, and **I/O Control**. The **Address Register** also receives an **ADD** signal and outputs to the **Bank Select** and **Refresh Counter Row Buffer**. The **Bank Select** outputs to the **Row Decoder**. The **Refresh Counter Row Buffer** receives $\overline{\text{LRAS}}$ and $\overline{\text{LCBR}}$ and outputs to the **Row Decoder**. The **Row Decoder** outputs to the **Sense Amp** and the **Col. Buffer**. The **Sense Amp** consists of four parallel units, each receiving $\overline{\text{LCAS}}$ and outputting x8/16/32 to the **2-bit prefetch** and the **Column Decoder**. The **Column Decoder** outputs to the **Latency & Burst Length** block. The **Latency & Burst Length** block outputs to the **Col. Buffer** and the **Output Buffer**. The **Col. Buffer** outputs to the **Output Buffer**. The **Output Buffer** receives $\overline{\text{LDM}}$ and outputs x4/8/16 to the **I/O Control** and x4/8/16 to the **Data Strobe**. The **I/O Control** receives $\overline{\text{LWE}}$ and $\overline{\text{LDM}}$ and outputs x4/8/16 to the **Data Input Register** and x4/8/16 to the **Data Strobe**. The **Data Input Register** (Serial to parallel) receives x4/8/16 from the **I/O Control** and outputs x8/16/32 to the **Sense Amp**. The **Data Strobe** receives x4/8/16 from the **Output Buffer** and x4/8/16 from the **I/O Control**.

Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	Input	Clock : CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/ $\overline{\text{CK}}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{\text{CK}}$ and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
$\overline{\text{CS}}$	Input	Chip Select : $\overline{\text{CS}}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs : $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
LDM,(UDM)	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0~D7 ; UDM corresponds to the data on DQ8~DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Address Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [0 : 12]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Data Input/Output : Data bus
LDQS,(U)DQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0~D7 ; UDQS corresponds to the data on DQ8~DQ15
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : +2.6V $\pm$ 0.1V
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : +2.6V $\pm$ 0.1V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

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Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9, A11,A12	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
				H	X	X	X	3				
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM(UDM/LDM for x16 only)			H	X				X			8	
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM(x4/8) sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

UDM/LDM(x16 only) sampled at the rising and falling edges of the UDQS/LDQS and Data-in are masked at the both edges (Write UDM/LDM latency is 0).

9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

DDR SDRAM 512Mb B-die (x4, x8, x16)

16M x 8Bit x 4 Banks / 8M x 16Bit x 4 Banks Double Data Rate SDRAM

General Description

The K4H510838B / K4H511638B is 536,870,912 bits of double data rate synchronous DRAM organized as 4x 16,777,216 / 4x 8,388,608 words by 8/16bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 400Mb/s per pin. I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommend operation condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

Recommended operating conditions(Voltage referenced to $V_{SS}=0V$, $T_A=0$ to $70^{\circ}C$)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.5	2.7		5
I/O Supply voltage	V_{DDQ}	2.5	2.7	V	5
I/O Reference voltage	V_{REF}	$0.49 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	V	1
I/O Termination voltage(system)	V_{TT}	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID}(DC)$	0.36	$V_{DDQ}+0.6$	V	3
V-I Matching: Pullup to Pulldown Current Ratio	$V_I(Ratio)$	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	I_{OH}	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	I_{OL}	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	I_{OH}	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	I_{OL}	9		mA	

Note : 1. V_{REF} is expected to be equal to $0.5 \cdot V_{DDQ}$ of the transmitting device, and to track variations in the dc level of same.

Peak-to-peak noise on V_{REF} may not exceed +/-2% of the dc value.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.

5. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM itself may not exceed the DC voltage range of 2.6V +/-100mV.

DDR SDRAM Spec Items & Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK=5ns for DDR400; DQ,DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; CS = high between valid commands.	IDD0
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition; CS = high between valid commands.	IDD1
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); tCK=5ns for DDR400; Vin = Vref for DQ,DQS and DM.	IDD2P
Precharge Floating standby current; CS# >= VIH(min);All banks idle; CKE >= VIH(min); tCK=5ns for DDR400; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	IDD2F
Precharge Quiet standby current; CS# >= VIH(min); All banks idle; CKE >= VIH(min); tCK=5ns for DDR400; Address and other control inputs stable at >= VIH(min) or <=VIL(max); Vin = Vref for DQ ,DQS and DM	IDD2Q
Active power - down standby current ; one bank active; power-down mode; CKE=< VIL (max); tCK=5ns DDR400; Vin = Vref for DQ,DQS and DM	IDD3P
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK=5ns for DDR400; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N
Operating current - burst read; Burst length = 2; reads; contiguous burst; One bank active; address and control inputs changing once per clock cycle; CL=3 at 5ns for DDR400; 50% of data changing on every transfer; Iout = 0 mA	IDD4R
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=3 at tCK=5ns for DDR400; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	IDD4W
Auto refresh current; tRC = tRFC(min) - 14*tCK for DDR400 at tCK=5ns;	IDD5
Self refresh current; CKE =< 0.2V; External clock on; tCK = 5ns for DDR400.	IDD6

Input/Output Capacitance

(V_{DD}=2.6, V_{DDQ}=2.6V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Delta	Unit	Note
Input capacitance (A0 ~ A12, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	CIN1	2	3	0.5	pF	4
Input capacitance(CK, $\overline{CK}$)	CIN2	2	3	0.25	pF	4
Data & DQS input/output capacitance	COUT	4	5	0.5	pF	1,2,3,4
Input capacitance(DM for 8, UDM/LDM for x16)	CIN3	4	5		pF	1,2,3,4

- Note :**
- These values are guaranteed by design and are tested on a sample basis only.
 - Although DM is an input -only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
 - Unused pins are tied to ground.
 - This parameter is sampled. VDDQ = +2.6V +0.1V, VDD = +2.6V +0.1V, f=100MHz, tA=25°C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

DDR SDRAM 512Mb B-die (x4, x8, x16)

< Detailed test conditions for DDR SDRAM IDD1 & IDD7A >

IDD1 : Operating current: One bank operation

1. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs change logic state once per Deselect cycle.

I_{out} = 0mA

2. Timing patterns

- CC(200Mhz,CL=3) : tCK=5ns, CL=3, BL=4, tRCD=3*tCK(CC), tRC=11*tCK(CC), tRAS=8*tCK

Setup : A0 N N R0 N N N N P0 N N

Read : A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing

*50% of data changing at every transfer

IDD7A : Operating current: Four bank operation

1. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on Deselet edge are not changing.

I_{out} = 1mA

2. Timing patterns

- CC(200Mhz,CL=3) : tCK=5ns, CL=3, BL=4, tRCD=3*tCK(CC), tRC=11*tCK(CC), tRAS=8*tCK

Setup : A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N N

Read : A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N N - repeat the same timing with random address changing

*50% of data changing at every transfer

Legend : A = Activate, R=Read, W=Write, P=Precharge, N=NOP

DDR SDRAM 512Mb B-die (x4, x8, x16)

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DDR SDRAM I_{DD} spec table

(V_{DD}=2.7V, T = 10°C)

Symbol		64Mx8	Unit	Notes
		- CC(DDR400@CL=3)		
IDD0		165	mA	
IDD1		185	mA	
IDD2P		5	mA	
IDD2F		30	mA	
IDD2Q		25	mA	
IDD3P		35	mA	
IDD3N		95	mA	
IDD4R		200	mA	
IDD4W		240	mA	
IDD5		265	mA	
IDD6	Normal	5	mA	
	Low power	3	mA	Optional
IDD7A		430	mA	

Symbol		32Mx16	Unit	Notes
		- CC(DDR400@CL=3)		
IDD0		165	mA	
IDD1		190	mA	
IDD2P		5	mA	
IDD2F		30	mA	
IDD2Q		25	mA	
IDD3P		55	mA	
IDD3N		100	mA	
IDD4R		230	mA	
IDD4W		280	mA	
IDD5		265	mA	
IDD6	Normal	5	mA	
	Low power	3	mA	Optional
IDD7A		450	mA	

AC Operating Conditions

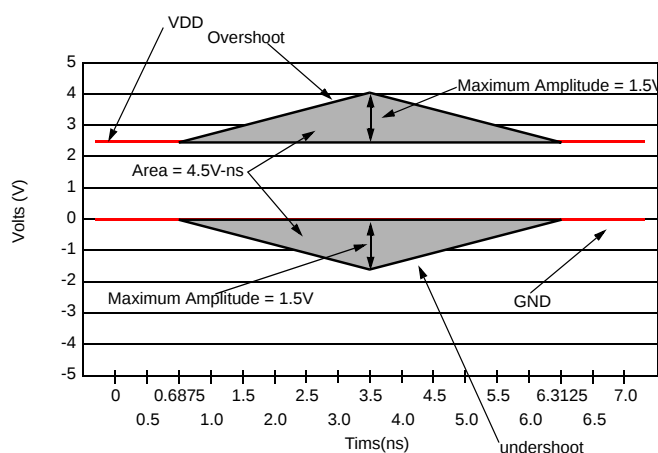
Parameter/Condition	Symbol	Min	Max-10	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V _{IH} (AC)	V _{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V _{IL} (AC)		V _{REF} - 0.31	V	
Input Differential Voltage, CK and CK inputs	V _{ID} (AC)	0.7	V _{DDQ} +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V _{IX} (AC)	0.5*V _{DDQ} -0.2	0.5*V _{DDQ} +0.2	V	2

Notes :

1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

AC Overshoot/Undershoot specification for Address and Control Pins

Parameter	Specification
	DDR400
Maximum peak amplitude allowed for overshoot	1.5V
Maximum peak amplitude allowed for undershoot	1.5V
The area between the overshoot signal and VDD must be less than or equal to	4.5V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5V-ns



AC overshoot/Undershoot Definition

AC Operating Conditions

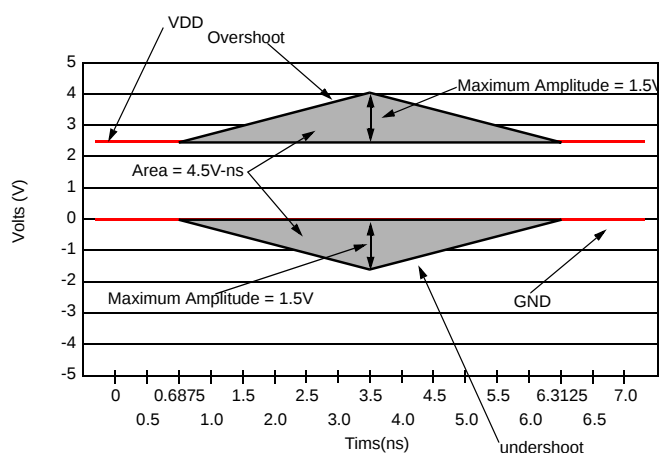
Parameter/Condition	Symbol	Min	Max-10	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V _{IH} (AC)	V _{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V _{IL} (AC)		V _{REF} - 0.31	V	
Input Differential Voltage, CK and CK inputs	V _{ID} (AC)	0.7	V _{DDQ} +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V _{IX} (AC)	0.5*V _{DDQ} -0.2	0.5*V _{DDQ} +0.2	V	2

Notes :

1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

AC Overshoot/Undershoot specification for Address and Control Pins

Parameter	Specification
	DDR400
Maximum peak amplitude allowed for overshoot	1.5V
Maximum peak amplitude allowed for undershoot	1.5V
The area between the overshoot signal and VDD must be less than or equal to	4.5V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5V-ns



AC overshoot/Undershoot Definition

DDR SDRAM 512Mb B-die (x4, x8, x16)

AC Timing Parameters and Specifications

Parameter	Symbol	- CC(DDR400@CL=3)		Unit	Note
		Min	Max		
Row cycle time	tRC	55		ns	
Refresh row cycle time	tRFC	70		ns	
Row active time	tRAS	40	70K	ns	
RAS to CAS delay	tRCD	15		ns	
Row precharge time	tRP	15		ns	
Row active to Row active delay	tRRD	10		ns	
Write recovery time	tWR	15		ns	
Internal write to read command delay	tWTR	2		tCK	
Clock cycle time	CL=3.0	5	10	ns	16
	CL=2.5	6	12	ns	
Clock high level width	tCH	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	tCK	
DQS-out access time from CK/CK	tDQSCK	-0.55	+0.55	ns	
Output data access time from CK/CK	tAC	-0.65	+0.65	ns	
Data strobe edge to output data edge	tDQSQ	-	0.4	ns	13
Read Preamble	tRPRE	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.72	1.28	tCK	
Write preamble setup time	tWPRES	0		ps	5
Write preamble	tWPRE	0.25		tCK	
Write postamble	tWPST	0.4	0.6	tCK	4
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK	
DQS-in high level width	tDQSH	0.35		tCK	
DQS-in low level width	tDQSL	0.35		tCK	
Address and Control Input setup time	tIS	0.6		ns	h,7~10
Address and Control Input hold time	tIH	0.6		ns	h,7~10
Data-out high impedance time from CK/CK	tHZ	-	tAC max	ns	3
Data-out low impedance time from CK/CK	tLZ	tAC min	tAC max	ns	3
Mode register set cycle time	tMRD	2		tCK	
DQ & DM setup time to DQS, slew rate 0.5V/ns	tDS	0.4		ns	i, j
DQ & DM hold time to DQS, slew rate 0.5V/ns	tDH	0.4		ns	i, j
DQ & DM input pulse width	tDIPW	1.75		ns	9
Control & Address input pulse width for each input	tIPW	2.2		ns	9
Refresh interval time	tREFI		7.8	us	6
Output DQS valid window	tQH	tHP -tQHS	-	ns	12
Clock half period	tHP	min tCH/tCL	-	ns	11, 12

DDR SDRAM 512Mb B-die (x4, x8, x16)

Preliminary
DDR SDRAM

Parameter	Symbol	- CC(DDR400@CL=3)		Unit	Note
		Min	Max		
Data hold skew factor	tQHS		0.5	ns	12
Auto Precharge write recovery + precharge time	tDAL	-	-	ns	14
Exit self refresh to non-READ command	tXSNR	75		ns	15
Exit self refresh to READ command	tXSRD	200	-	tCK	

Component Notes

1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
2. The value of V_{IX} is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the dc level of the same.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
5. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
6. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
7. For command/address input slew rate ≥ 0.5 V/ns
8. For CK & $\overline{CK}$ slew rate ≥ 0.5 V/ns
9. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
10. Slew Rate is measured between $V_{OH}(ac)$ and $V_{OL}(ac)$.
11. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
12. $tQH = tHP - tQHS$, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
13. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
14. $tDAL = (tWR/tCK) + (tRP/tCK)$
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR400(CC) at CL=3 and tCK=5ns $tDAL = (15 \text{ ns} / 5 \text{ ns}) + (15 \text{ ns} / 5 \text{ ns}) = \{(3) + (3)\} \text{CLK}$
 $tDAL = 6 \text{ clocks}$
15. In all circumstances, tXSNR can be satisfied using $tXSNR = tRFC_{min} + 1 \cdot tCK$
16. The only time that the clock frequency is allowed to change is during self-refresh mode.

DDR SDRAM 512Mb B-die (x4, x8, x16)

System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR400 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR400			
PARAMETER	SYMBOL	MIN	MAX	Units	Notes
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	V/ns	a, k

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tIS	tIH	Units	Notes
0.5 V/ns	0	0	ps	h
0.4 V/ns	+50	0	ps	h
0.3 V/ns	+100	0	ps	h

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tDS	tDH	Units	Notes
0.5 V/ns	0	0	ps	j
0.4 V/ns	+75	+75	ps	j
0.3 V/ns	+150	+150	ps	j

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	tDS	tDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	i
+/- 0.25 V/ns	+50	+50	ps	i
+/- 0.5 V/ns	+100	+100	ps	i

Table 5 : Output Slew Rate Characteristic (X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g

Table 6 : Output Slew Rate Characteristic (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS	DDR400		
PARAMETER	MIN	MAX	Notes
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	-	e,k

System Notes :

a. Pullup slew rate is characterized under the test conditions as shown in Figure 1.

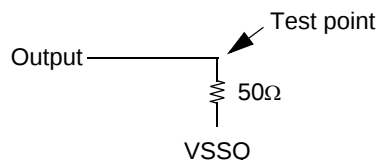


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

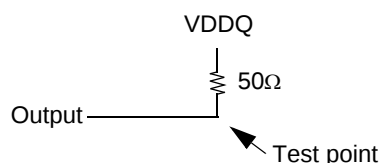


Figure 2 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)

Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)

Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example : For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching from either high to low, or low to high.

For Maximum slew rate, only one DQ is switching from either high to low, or low to high.

The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions

Typical : 25 °C (T Ambient), VDDQ = 2.6V, typical process

Minimum : 70 °C (T Ambient), VDDQ = 2.5V, slow - slow process

Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOP11 package devices only.

h. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

i. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

The delta rise/fall rate is calculated as:

$$\{1/(\text{Slew Rate1})\} - \{1/(\text{Slew Rate2})\}$$

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

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- j. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC - AC slew rate and the DC- DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.
- k. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotony.