
Document Title

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
Rev. 0.0	- Preliminary specification release		Preliminary
Rev. 0.1	- Change specification format. No change was made in parameters.	April, 1997	Preliminary
Rev. 0.2	- Updated Part Number and Pin Description. Updated and added Input/Output Voltage Level and V _{DDQ} Updated DC Characteristics and Pin Capacitance. Updated AC Characteristics, Test Conditions and Timing Wave Form. For JTAG, updated Vendor Definition and added tsvch/tchsx.	Jan. 1998	Preliminary
Rev. 0.3	- Updated PECL Clock Input Level, Output Leakage Current Updated 119 BGA Package Thermal Characteristics	Aug. 1998	Preliminary
Rev. 1.0	- Final specification release	Dec. 1998	Final
Rev. 2.0	- Single ended LVCMOS clock operation added	Oct. 2000	

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

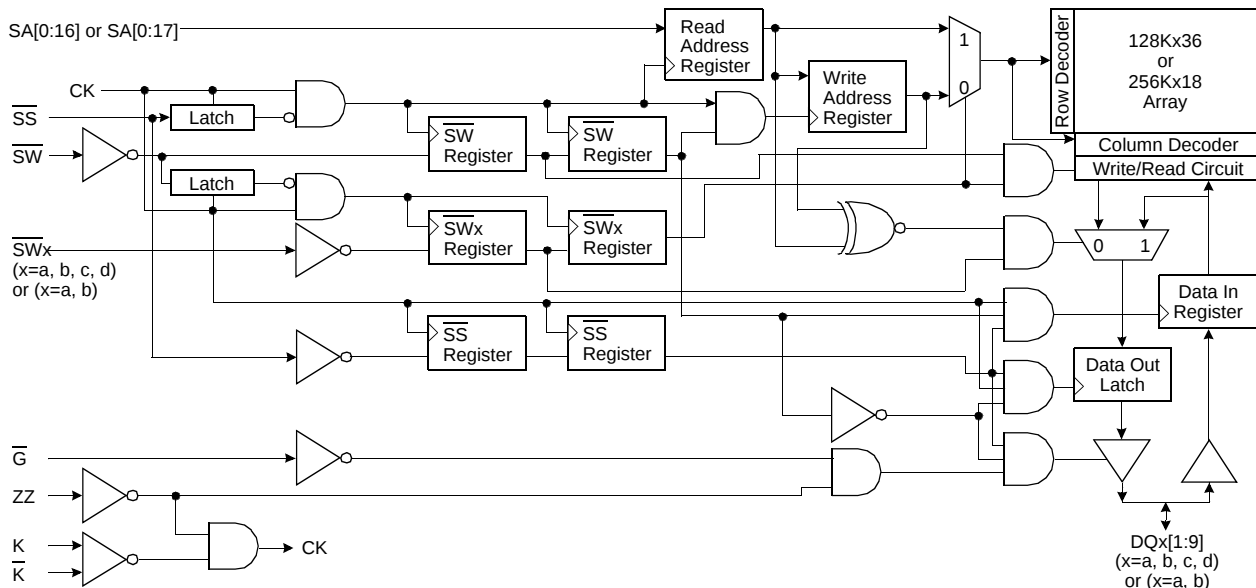
128Kx36 & 256Kx18 Synchronous Pipelined SRAM

FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/ Output Power Supply.
- LVTTTL 3.3V Input and Output Levels.
- Differential, PECL Clock Inputs K, $\bar{K}$, or Single ended LVCMOS Clock
- Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mmx22mm).

Organiza-tion	Part Number	Cycle Time	Access Time
128Kx36	K7P403623M-H65	6	6.5
	K7P403623M-H70	6.5	7.0
	K7P403623M-H75	7	7.5
256Kx18	K7P401823M-H65	6	6.5
	K7P401823M-H70	6.5	7.0
	K7P401823M-H75	7	7.5

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\bar{K}$	Differential Clocks(PECL Level)	VDDQ	Output Power Supply
SA _n	Synchronous Address Input	M ₁ , M ₂	Read Protocol Mode Pins (M ₁ =VDD, M ₂ =VSS)
DQ _n	Bi-directional Data Bus	$\bar{G}$	Asynchronous Output Enable
$\bar{SW}$	Synchronous Global Write Enable	$\bar{SS}$	Synchronous Select
$\bar{SW}_a$	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\bar{SW}_b$	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\bar{SW}_c$	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\bar{SW}_d$	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	VSS	GND
VDD	Core Power Supply	NC	No Connection

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7P403623M(128Kx36)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA ₁₃	SA ₁₀	NC	SA ₇	SA ₄	V _{DDQ}
B	NC	NC	SA ₉	NC	SA ₈	NC	NC
C	NC	SA ₁₂	SA ₁₁	V _{DD}	SA ₆	SA ₅	NC
D	DQC ₈	DQC ₉	V _{SS}	NC*	V _{SS}	DQb ₉	DQb ₈
E	DQC ₆	DQC ₇	V _{SS}	$\overline{SS}$	V _{SS}	DQb ₇	DQb ₆
F	V _{DDQ}	DQC ₅	V _{SS}	$\overline{G}$	V _{SS}	DQb ₅	V _{DDQ}
G	DQC ₃	DQC ₄	$\overline{SWc}$	NC*	$\overline{SWb}$	DQb ₄	DQb ₃
H	DQC ₁	DQC ₂	V _{SS}	NC*	V _{SS}	DQb ₂	DQb ₁
J	V _{DDQ}	V _{DD}	NC***	V _{DD}	NC***	V _{DD}	V _{DDQ}
K	DQd ₁	DQd ₂	V _{SS}	K	V _{SS}	DQa ₂	DQa ₁
L	DQd ₃	DQd ₄	$\overline{SWd}$	$\overline{K}$	$\overline{SWa}$	DQa ₄	DQa ₃
M	V _{DDQ}	DQd ₅	V _{SS}	$\overline{SW}$	V _{SS}	DQa ₅	V _{DDQ}
N	DQd ₆	DQd ₇	V _{SS}	SA ₁₆	V _{SS}	DQa ₇	DQa ₆
P	DQd ₈	DQd ₉	V _{SS}	SA ₀	V _{SS}	DQa ₉	DQa ₈
R	NC	SA ₁₅	M ₁	V _{DD}	M ₂	SA ₂	NC
T	NC	NC	SA ₁₄	SA ₁	SA ₃	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC**	V _{DDQ}

NOTE : 1. NC* is used for the Boundary Scan.
2. NC** is reserved for TRST input.
3. NC*** is reserved for HSTL interface.

KM718FV4022(256Kx18)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA ₁₃	SA ₁₀	NC	SA ₇	SA ₄	V _{DDQ}
B	NC	NC	SA ₉	NC	SA ₈	NC	NC
C	NC	SA ₁₂	SA ₁₁	V _{DD}	SA ₆	SA ₅	NC
D	DQb ₁	NC	V _{SS}	NC*	V _{SS}	DQa ₉	NC
E	NC	DQb ₂	V _{SS}	$\overline{SS}$	V _{SS}	NC	DQa ₈
F	V _{DDQ}	NC	V _{SS}	$\overline{G}$	V _{SS}	DQa ₇	V _{DDQ}
G	NC	DQb ₃	$\overline{SWb}$	NC*	NC	NC	DQa ₆
H	DQb ₄	NC	V _{SS}	NC*	V _{SS}	DQa ₅	NC
J	V _{DDQ}	V _{DD}	NC***	V _{DD}	NC***	V _{DD}	V _{DDQ}
K	NC	DQb ₅	V _{SS}	K	V _{SS}	NC	DQa ₄
L	DQb ₆	NC	NC	$\overline{K}$	$\overline{SWa}$	DQa ₃	NC
M	V _{DDQ}	DQb ₇	V _{SS}	$\overline{SW}$	V _{SS}	NC	V _{DDQ}
N	DQb ₈	NC	V _{SS}	SA ₁₆	V _{SS}	DQa ₂	NC
P	NC	DQb ₉	V _{SS}	SA ₁	V _{SS}	NC	DQa ₁
R	NC	SA ₁₅	M ₁	V _{DD}	M ₂	SA ₂	NC
T	NC	SA ₁₇	SA ₁₄	NC	SA ₃	SA ₀	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC**	V _{DDQ}

NOTE : 1. NC* is used for the Boundary Scan.
2. NC** is reserved for TRST input.
3. NC*** is reserved for HSTL interface.

FUNCTION DESCRIPTION

The K7P403623M and K7P401823M are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262,144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential PECL level K clocks or single ended LVCMOS clock are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are both sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}[a:d]$ are valid to signal that a valid operations is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}[a:d]$ signal which 9-bit bytes will be written. Timing of $\overline{SW}[a:d]$ is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(t_{ZZR}) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SWa}$	$\overline{SWb}$	$\overline{SWc}$	$\overline{SWd}$	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	X	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	V _{DD}	-0.5 to 3.9	V
Output Supply Voltage Relative to Vss	V _{DDQ}	V _{DD}	V
Voltage on any I/O pin Relative to Vss	V _{TERM}	-0.5 to V _{DD} +0.5	V
Maximum Power Dissipation	P _D	3	W
Output Short-Circuit Current	I _{OUT}	25	mA
Operating Temperature	T _{OPR}	0 to 70	°C
Storage Temperature	T _{STG}	-55 to 125	°C

NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V _{DD}	3.15	3.3	3.45	V	
Output Power Supply Voltage	V _{DDQ}	2.35	2.5	3.45	V	
Input High Level	V _{IH}	1.7	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.7	V	
PECL Clock Input High Level	V _{IH} -PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	V _{IL} -PECL	1.490	-	1.825	V	1
Clock Input Signal Voltage	V _{IN}	-0.3	-	3.45	V	2
Clock Input Differential Voltage	V _{DIF} -CLK	0.2	-	V _{DD} +0.6	V	2
Clock Input Common Mode Voltage	V _{CM} -CLK	1.1	-	2.1	V	2
Operating Junction Temperature	T _J	10	-	110	°C	

NOTE

1. For operation with differential PECL clock inputs.
2. For operation with single ended LVCMOS clock input.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V _{IN} =V _{IH} or V _{IL} , ZZ & SS=V _{IL})	I _{DD65} I _{DD7} I _{DD75}	-	600 550 500	mA	1, 2
Average Power Supply Operating Current-x18 (V _{IN} =V _{IH} or V _{IL} , ZZ & SS=V _{IL})	I _{DD65} I _{DD7} I _{DD75}	-	550 500 450	mA	1, 2
Power Supply Standby Current (V _{IN} =V _{IH} or V _{IL} , ZZ=V _{IH})	I _{SB}	-	60	mA	1
Input Leakage Current (V _{IN} =V _{SS} or V _{DDQ})	I _{LI}	-1	1	μA	
Output Leakage Current (V _{OUT} =V _{SS} or V _{DDQ} , ZZ=V _{IH} , $\bar{G}$ =V _{IH})	I _{LO}	-1	1	μA	
Output High Voltage(I _{OH} =-4mA) for V _{DDQ} =3.3V Output High Voltage(I _{OH} =-4mA) for V _{DDQ} =2.5V	V _{OH1} V _{OH2}	2.4 2.0	V _{DDQ}	V	
Output Low Voltage(I _{OL} =4mA)	V _{OL}	V _{SS}	0.4	V	

NOTE : 1. Minimum cycle. I_{OUT}=0mA.

PIN CAPACITANCE

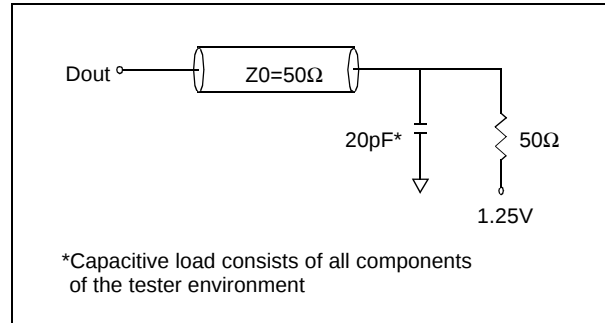
Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C _{IN}	4	5	pF
Output Capacitance	C _{OUT}	7	8	pF

NOTE : Periodically sampled and not 100% tested. (dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V _{DD}	3.15~3.45	V
Output Power Supply Voltage	V _{DDQ}	2.4~2.6	V
Input High/Low Level	V _{IH} /V _{IL}	1.7/0.7	V
Clock Input High/Low Level(PECL)	V _{IH} /V _{IL}	2.4/1.5	V
Input Rise/Fall Time	T _R /T _F	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T _R /T _F	1.0/1.0	ns
Input and Out Timing Reference Level		1.25	V
Clock Input Timing Reference Level		Cross Point	V

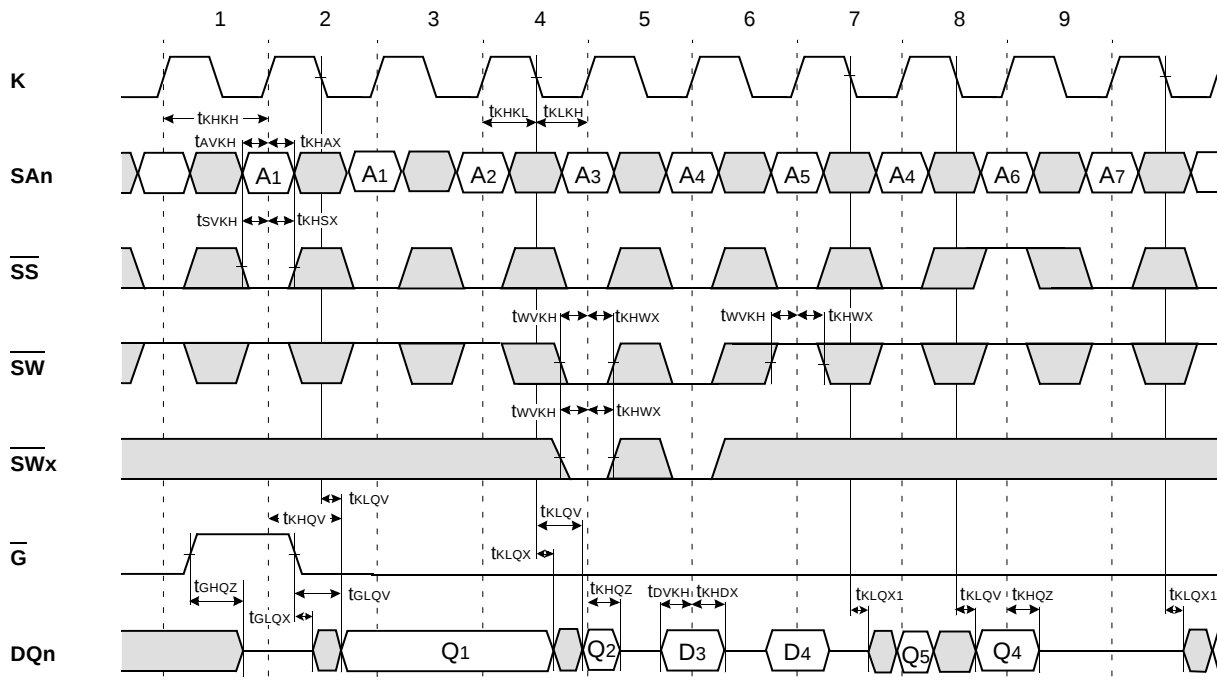
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol	-65		-70		-75		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t _{KHKH}	6.0	-	6.5	-	7.0	-	ns	
Clock High Pulse Width	t _{KHKL}	2.0	-	2.0	-	2.0	-	ns	
Clock Low Pulse Width	t _{KLKH}	2.0	-	2.0	-	2.0	-	ns	
Clock High to Output Valid	t _{KHQV}	-	6.5	-	7.0	-	7.5	ns	
Clock Low to Output Valid	t _{KLQV}	-	2.5	-	2.5	-	3.0	ns	
Clock Low to Output Hold	t _{KLQX}	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	t _{AVKH}	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	t _{KHAX}	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	t _{DVKH}	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	t _{KHDX}	1.0	-	1.0	-	1.0	-	ns	
SW, SW[a:d] Setup Time	t _{WVKH}	0.5	-	0.5	-	0.5	-	ns	
SW, SW[a:d] Hold Time	t _{KHWX}	1.0	-	1.0	-	1.0	-	ns	
SS Setup Time	t _{SVKH}	0.5	-	0.5	-	0.5	-	ns	
SS Hold Time	t _{KHSX}	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	t _{KHQZ}	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	t _{KLQX1}	0.5	-	0.5	-	0.5	-	ns	
$\bar{G}$ High to Output High-Z	t _{GHQZ}	-	2.5	-	3.0	-	3.5	ns	
$\bar{G}$ Low to Output Low-Z	t _{GLQX}	0.5	-	0.5	-	0.5	-	ns	
$\bar{G}$ Low to Output Valid	t _{GLQV}	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	t _{ZZE}	-	6.5	-	7.0	-	7.5	ns	
ZZ Low to Recovery(Wake-up Time)	t _{ZZR}	-	6.0	-	6.5	-	7.0	ns	

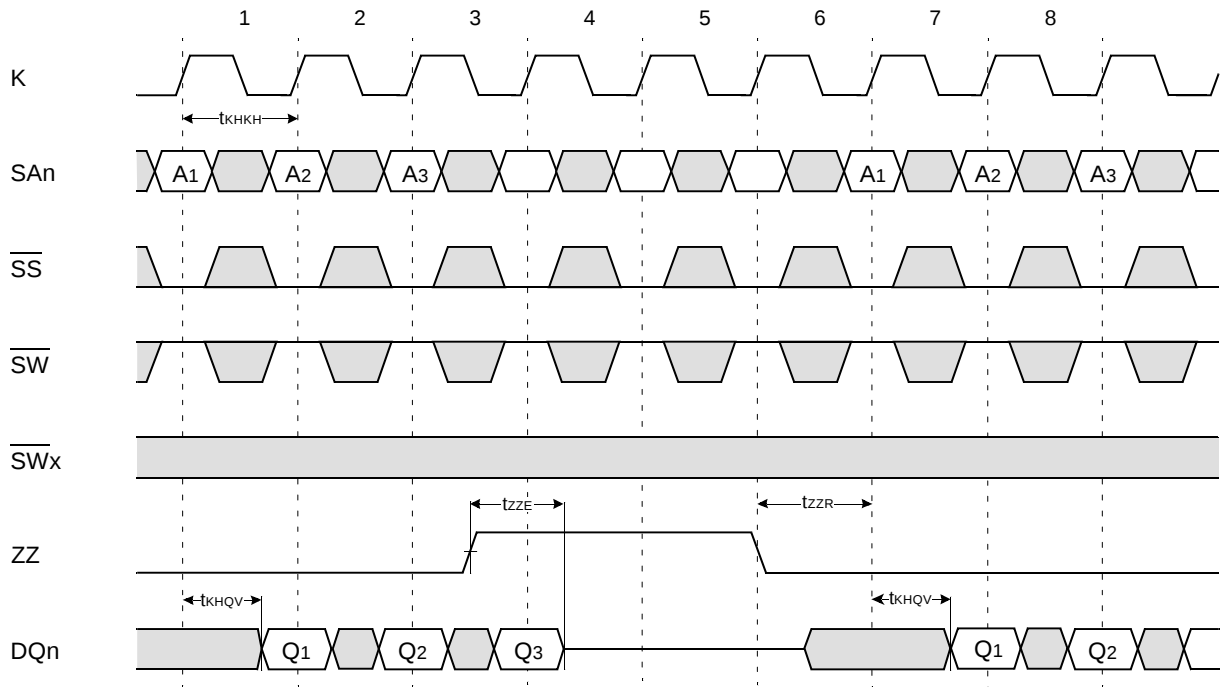
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES



NOTE

1. D3 is the input data written in memory location A3.
2. Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.
3. Data is valid at the output at the later of t_{KHQV} following the rising clock edge, or t_{KLQV} following the following clock edge.
4. When SS is sampled high or SW is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than t_{KHQZ} following the rising clock edge.
5. When SS is low and SW is high on the rising edge of clock, the outputs go into Low-Z state (being driven) no earlier than t_{KLQX1} following the next falling edge of clock.
6. When the SRAM is deselected, the output goes Hi-Z at t_{KHQZ} following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until t_{KLQX1} after the falling clock edge.

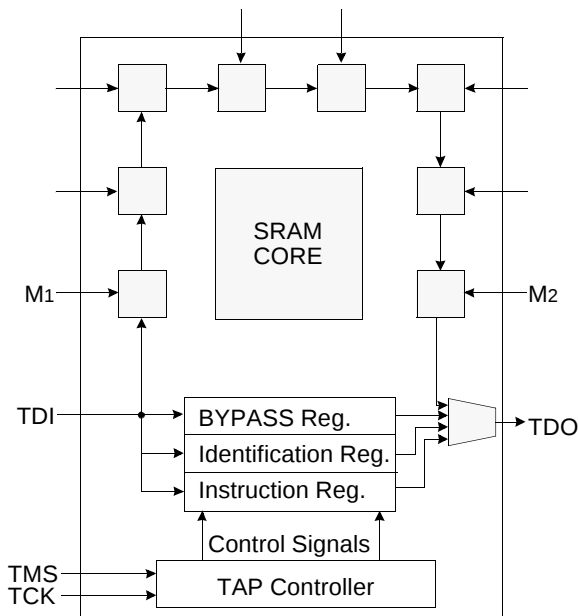
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



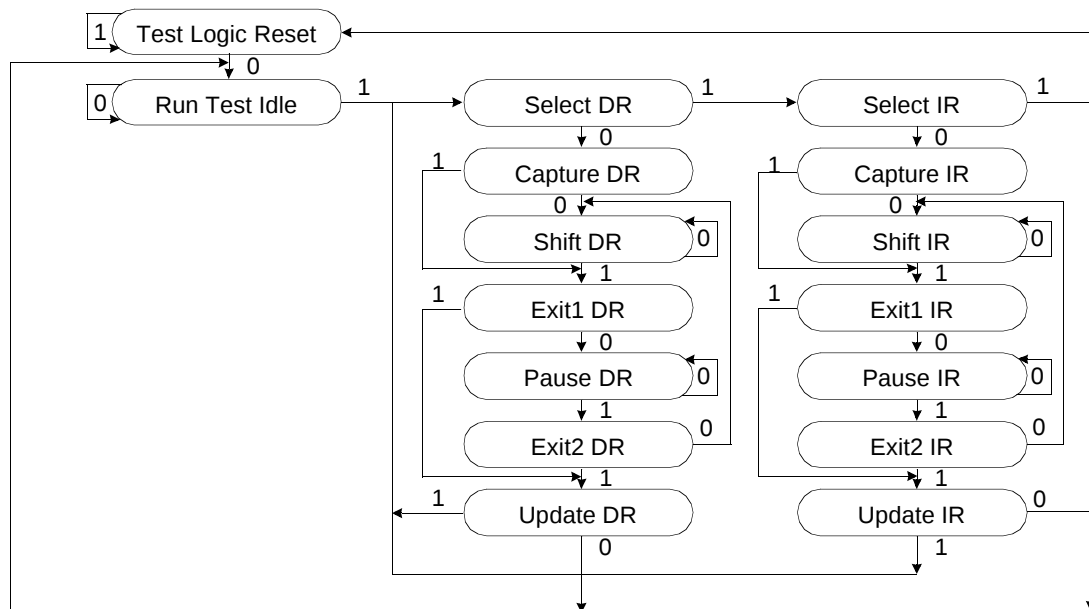
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to VSS when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	xxxxxx	00001001110	1
256Kx18	0000	00110 00011	xxxxxx	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA ₉		SA ₈	5B	35
37	2B	NC		NC	6B	34
38	3A	SA ₁₀		SA ₇	5A	33
39	3C	SA ₁₁		SA ₆	5C	32
40	2C	SA ₁₂		SA ₅	6C	31
41	2A	SA ₁₃		SA ₄	6A	30
42	2D	DQc ₉		DQb ₉	6D	29
43	1D	DQc ₈		DQb ₈	7D	28
44	2E	DQc ₇		DQb ₇	6E	27
45	1E	DQc ₆		DQb ₆	7E	26
46	2F	DQc ₅		DQb ₅	6F	25
47	2G	DQc ₄		DQb ₄	6G	24
48	1G	DQc ₃		DQb ₃	7G	23
49	2H	DQc ₂		DQb ₂	6H	22
50	1H	DQc ₁		DQb ₁	7H	21
51	3G	$\overline{SWc}$		$\overline{SWb}$	5G	20
52	4D	NC		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	NC		$\overline{K}$	4L	17
55	4H	NC		$\overline{SWa}$	5L	16
56	4M	$\overline{SW}$		DQa ₁	7K	15
57	3L	$\overline{SWd}$		DQa ₂	6K	14
58	1K	DQd ₁		DQa ₃	7L	13
59	2K	DQd ₂		DQa ₄	6L	12
60	1L	DQd ₃		DQa ₅	6M	11
61	2L	DQd ₄		DQa ₆	7N	10
62	2M	DQd ₅		DQa ₇	6N	9
63	1N	DQd ₆		DQa ₈	7P	8
64	2N	DQd ₇		DQa ₉	6P	7
65	1P	DQd ₈		ZZ	7T	6
66	2P	DQd ₉		SA ₃	5T	5
67	3T	SA ₁₄		SA ₂	6R	4
68	2R	SA ₁₅		SA ₁	4T	3
69	4N	SA ₁₆		SA ₀	4P	2
70	3R	M ₁		M ₂	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA ₉		SA ₈	5B	25
27	2B	NC		NC	6B	24
28	3A	SA ₁₀		SA ₇	5A	23
29	3C	SA ₁₁		SA ₆	5C	22
30	2C	SA ₁₂		SA ₅	6C	21
31	2A	SA ₁₃		SA ₄	6A	20
				DQa ₉	6D	19
32	1D	DQb ₁				
33	2E	DQb ₂				
				DQa ₈	7E	18
				DQa ₇	6F	17
34	2G	DQb ₃				
				DQa ₆	7G	16
				DQa ₅	6H	15
35	1H	DQb ₄				
36	3G	$\overline{SWb}$				
37	4D	NC		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	NC		$\overline{K}$	4L	12
40	4H	NC		$\overline{SWa}$	5L	11
41	4M	$\overline{SW}$		DQa ₄	7K	10
42	2K	DQb ₅		DQa ₃	6L	9
43	1L	DQb ₆				
44	2M	DQb ₇		DQa ₂	6N	8
45	1N	DQb ₈		DQa ₁	7P	7
				ZZ	7T	6
46	2P	DQb ₉		SA ₃	5T	5
47	3T	SA ₁₄		SA ₂	6R	4
48	2R	SA ₁₅				
49	4N	SA ₁₆		SA ₁	4P	3
50	2T	SA ₁₇		SA ₀	6T	2
51	3R	M ₁		M ₂	5R	1

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.15	3.3	3.45	V	
Input High Level	V _{IH}	2.0	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.8	V	
Output High Voltage(I _{OH} =-2mA)	V _{OH}	2.4	-	V _{DD}	V	
Output Low Voltage(I _{OL} =2mA)	V _{OL}	V _{SS}	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

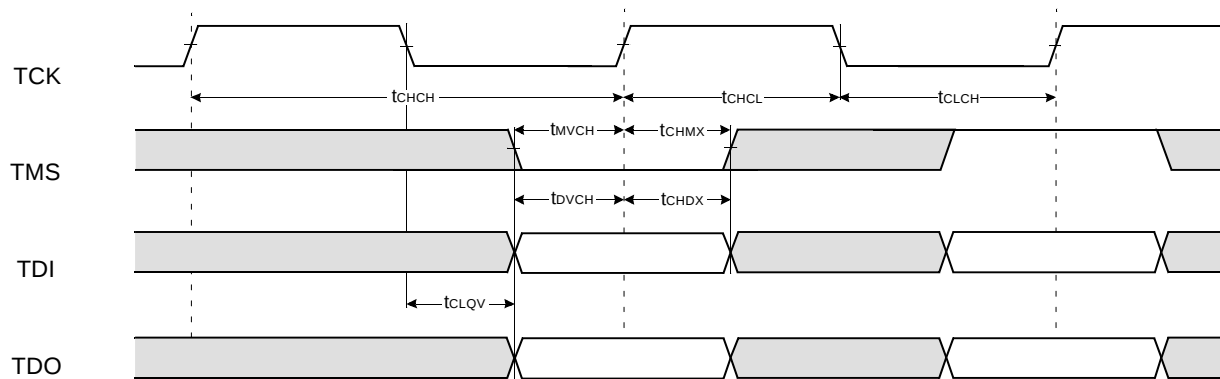
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load.

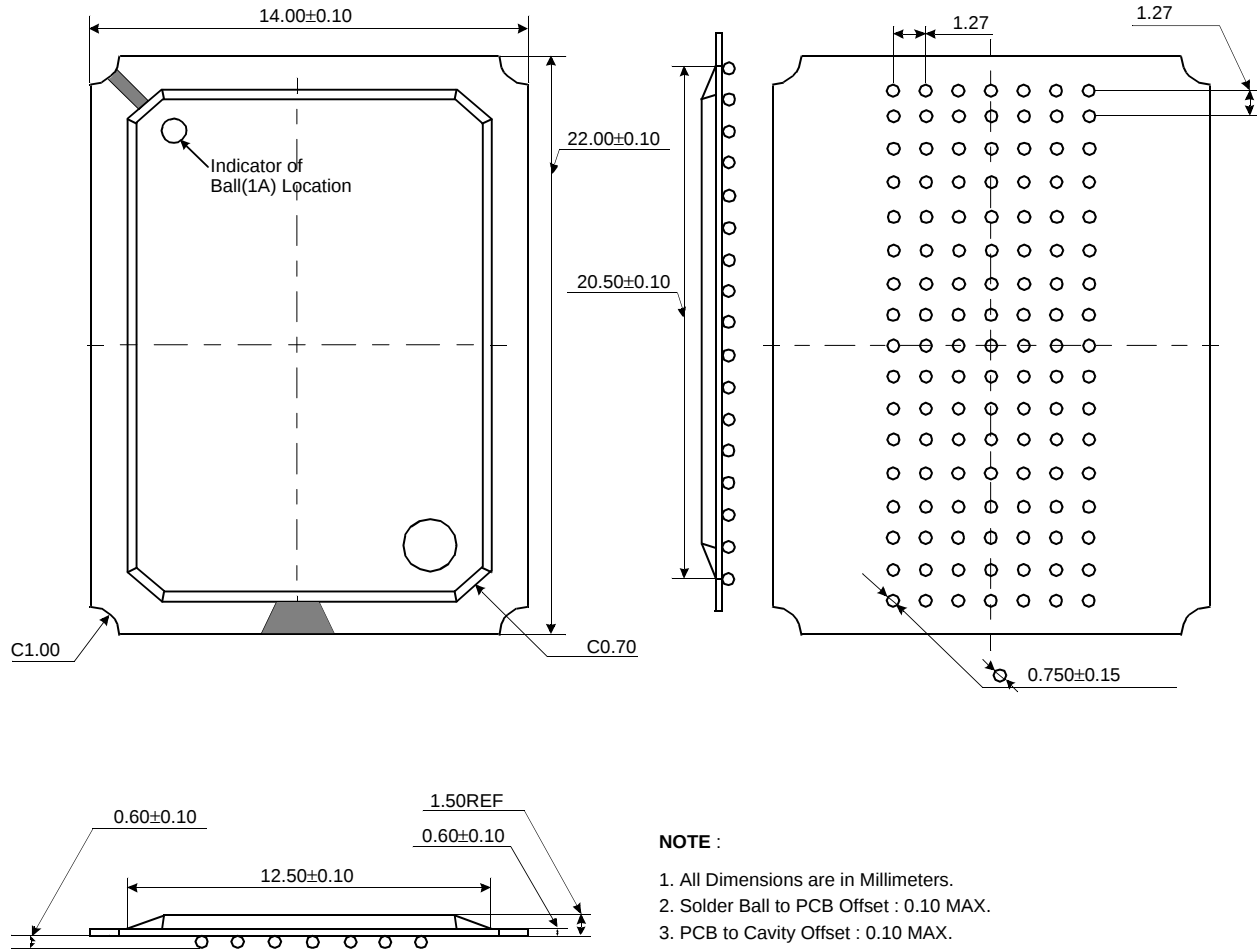
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{dvCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{svCH}	5	-	ns	
SRAM Input Hold Time	t _{chsX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Junction to Ambient(at air flow of 1m/sec)	Theta_JA	-	-	17	°C/W	
Junction to Case	Theta_JC	-	-	4	°C/W	
Junction to Solder Ball	Theta_JB	-	-	10	°C/W	