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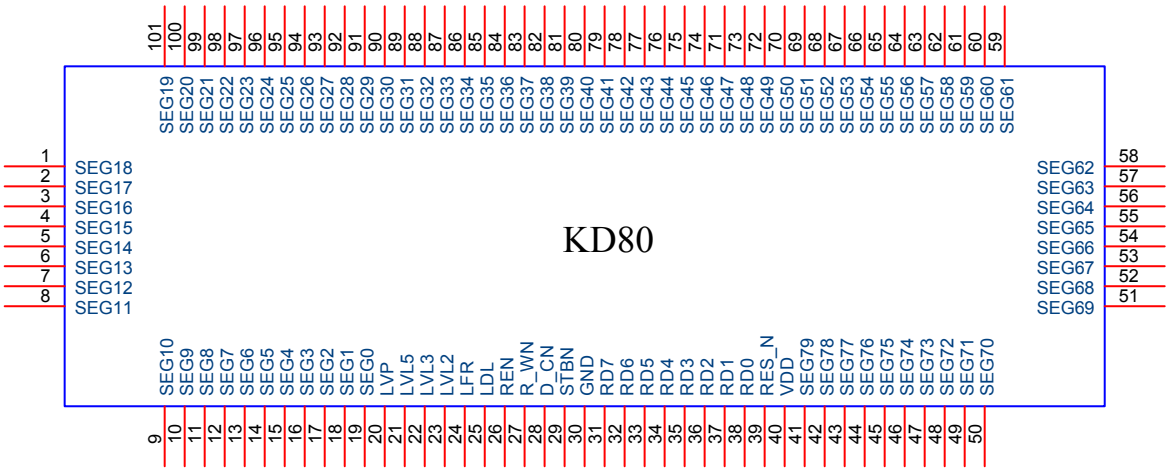
1. General Description

KD80 is a member of peripheral IC series developed by King Billion Electronics Co. It is a black and white LCD Segment Extender. This chip must be used with KB's Type III or Type IV LCD Driver. This chip interfaces with KB's MCU with provisions of Segment Extender Interface LFR and LDL. KB's MCUs control KD80 through a command interface. The MCU can read/write display patterns to graphic mode display RAM by first setting up the target address, selecting the driver configuration, and then enabling the driver. KD80 can support four different configurations: 32 COM, 48 COM, 64 COM and 80 COM selectable by command register. The KD80 uses some of the memory as display RAM, while the memory not used for display can be access as general-purpose memory.

2. Features

- ✓ 80 output LCD segment driver.
- ✓ Operating Range: 2.4V ~ 5.5V
- ✓ LCD Operating Voltage: < 9.0V
- ✓ Four LCD Configurations: 32, 48, 64, or 80 COM.
- ✓ Built-in dual-port display RAM: 2K bytes
- ✓ Command mode interface.
- ✓ Spare RAM for general purpose.

3. Pin Description



Pin #	Pin Name	I/O	Description
41..101 1..19	SEG[79..0]	O	LCD Segment Outputs
20	LVP	I	Charge Pump Output. These input pins must wire with master IC respectively. That means LVP with LVP, LVL5 with LVL5, …, LDL with LDL. Please refer application circuit for details.
21	LVL5	I	LCD Bias Voltage 5
22	LVL3	I	LCD Bias Voltage 3
23	LVL2	I	LCD Bias Voltage 2
24	LFR	I	LCD frame.
25	LDL	I	LCD data load.
26	REN	I	For RAM or Command Register Read/Write enable(0). This pin can be fixed at low.
27	R_WN	I	Read(1)/write(0) selection.

28	D_CN	I	Data(1)/Command(0) selection.
29	STBN	I	RAM or command R/W strobe(0)
30	GND	P	Power Ground Input
31..38	RD[7:0]	B	Command/Data I/O port. All these pins are in push-pull mode
39	RES_N	I	RESET PIN
40	VDD	P	Positive Power Input. Adding 0.1 µF capacitor as by-pass capacitor on power pins is necessary.(within 1 cm distance)

4. LCD RAM Map

There are four driving modes (32 COM、48 COM、64 COM and 80 COM) for KD80.

32 COM:

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	Page 6	SEG [71:64]	SEG [79:72]
COM0	7E0H	7C0H	7A0H	780H	760H	740H	720H	700H	COM0	6E0H	6C0H
COM1	7E1H	7C1H	7A1H	781H	761H	741H	721H	701H	COM1	6E1H	6C1H
:	:	:	:	:	:	:	:	:	:	:	:
COM15	7EFH	7CFH	7AFH	78FH	76FH	74FH	72FH	70FH	COM15	6EFH	6CFH
COM16	7F0H	7D0H	7B0H	790H	770H	750H	730H	710H	COM16	6F0H	6D0H
:	:	:	:	:	:	:	:	:	:	:	:
COM30	7FEH	7DEH	7BEH	79EH	77EH	75EH	73EH	71EH	COM30	6FEH	6DEH
COM31	7FFH	7DFH	7BFH	79FH	77FH	75FH	73FH	71FH	COM31	6FFH	6DFH

48 COM:

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	Page 6	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	Page 5	SEG [71:64]	SEG [79:72]
COM0	7C0H	780H	740H	700H	COM0	6C0H	680H	640H	600H	COM0	5C0H	580H
COM1	7C1H	781H	741H	701H	COM1	6C1H	681H	641h	601H	COM1	5C1H	581H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	COM15	6CFH	68FH	64FH	60FH	COM15	5CFH	58FH
COM16	7D0H	790H	750H	710H	COM16	6D0H	690H	650H	610H	COM16	5D0H	590H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	COM31	6DFH	69FH	65FH	61FH	COM31	5DFH	59FH
COM32	7E0H	7A0H	760H	720H	COM32	6E0H	6A0H	660H	620H	COM32	5E0H	5A0H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM46	7EEH	7AEH	76EH	72EH	COM46	6EEH	6AEH	66EH	62EH	COM46	5EEH	5AEH
COM47	7EFH	7AFH	76FH	72FH	COM47	6EFH	6AFH	66FH	62FH	COM47	5EFH	5AFH

64 COM:

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	Page 6	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	Page 5	SEG [71:64]	SEG [79:72]
COM0	7C0H	780H	740H	700H	COM0	6C0H	680H	640H	600H	COM0	5C0H	580H
COM1	7C1H	781H	741H	701H	COM1	6C1H	681H	641H	601H	COM1	5C1H	581H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	COM15	6CFH	68FH	64FH	60FH	COM15	5CFH	58FH
COM16	7D0H	790H	750H	710H	COM16	6D0H	690H	650H	610H	COM16	5D0H	590H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	COM31	6DFH	69FH	65FH	61FH	COM31	5DFH	59FH
COM32	7E0H	7A0H	760H	720H	COM32	6E0H	6A0H	660H	620H	COM32	5E0H	5A0H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM47	7EFH	7AFH	76FH	72FH	COM47	6EFH	6AFH	66FH	62FH	COM47	5EFH	5AFH
COM48	7F0H	7B0H	770H	730H	COM48	6F0H	6B0H	670H	630H	COM48	5F0H	5B0H
:	:	:	:	:	:	:	:	:	:	:	:	:
COM62	7FEH	7BEH	77EH	73EH	COM62	6FEH	6BEH	67EH	63EH	COM62	5FEH	5BEH
COM63	7FFH	7BFH	77FH	73FH	COM63	6FFH	6BFH	67FH	63FH	COM63	5FFH	5BFH

80 COM：

Page 7:3	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	SEG [71:64]	SEG [79:72]
COM0	780H	700H	680H	600H	580H	500H	480H	400H	380H	300H
COM1	781H	701H	681H	601H	581H	501H	481H	401H	381H	301H
:	:	:	:	:	:	:	:	:	:	:
COM15	78FH	70FH	68FH	60FH	58FH	50FH	48FH	40FH	38FH	30FH
COM16	790H	710H	690H	610H	590H	510H	490H	410H	390H	310H
:	:	:	:	:	:	:	:	:	:	:
COM31	79FH	71FH	69FH	61FH	59FH	51FH	49FH	41FH	39FH	31FH
COM32	7A0H	720H	6A0H	620H	5A0H	520H	4A0H	420H	3A0H	320H
:	:	:	:	:	:	:	:	:	:	:
COM47	7AFH	72FH	6AFH	62FH	5AFH	52FH	4AFH	42FH	3AFH	32FH
COM48	7B0H	730H	6B0H	630H	5B0H	530H	4B0H	430H	3B0H	330H
:	:	:	:	:	:	:	:	:	:	:
COM62	7BFH	73FH	6BFH	63FH	5BFH	53FH	4BFH	43FH	3BFH	33FH
COM63	7C0H	740H	6C0H	640H	5C0H	540H	4C0H	440H	3C0H	340H
:	:	:	:	:	:	:	:	:	:	:
COM78	7CEH	74EH	6CEH	64EH	5CEH	54EH	4CEH	44EH	3CEH	34EH
COM79	7CFH	74FH	6CFH	64FH	5CFH	54FH	4CFH	44FH	3CFH	34FH

5. Command Interface

KB's MCU with Segment Extender Interface controls KD80 by an 8-bit parallel data/command bus. The D_CN and R_WN pins select current activity to be a Command read/write or Data Read/Write. The STBN signal is the active low strobe signal to read/write to the command registers or read/write RAM content. There are 3 command registers which can be read/write in cyclic order. The command sequence are reset by any read/write to data or power-on reset or REN = 1 or RES_N = 0. The COM counter are reset to 00H by LEP = 0 or LFR signal transient.

cmd seq	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset
1	A7	A6	A5	A4	A3	A2	A1	A0	0x00
2	LEP	WR_INC	RD_INC	-	A11	A10	A9	A8	0x20
3	KS	COMS1	COMS0	-			-	-	

The address of display RAM can be configured to increment with each Read or Write access by setting the WR_INC and RD_INC bit of CMD2 register.

A11 ~ A0: display RAM address
RD_INC: address auto increment when read
WR_INC: address auto increment when write

WR_INC	RD_INC	A [11:0]
0	0	Automatically increment by one with each data read/write access
0	1	Automatically increment by one with each data write access

1	0	Automatically increment by one with each data read access
1	1	No automatically increment by one

LEP: LCD enable, 0: disable, 1: enable

COMS[1..0]: LCD Configuration

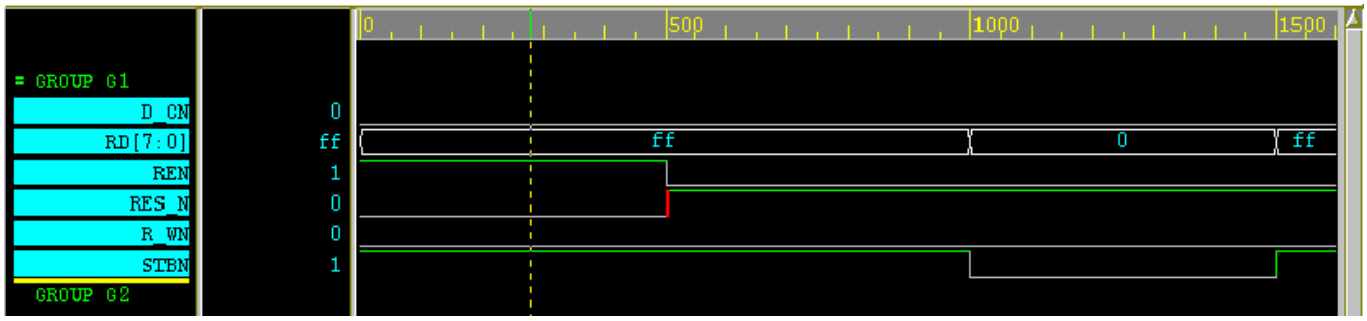
COMS[1]	COMS[0]	LCD configuration
0	0	32 COM
0	1	48 COM
1	0	64 COM
1	1	80 COM

KS:

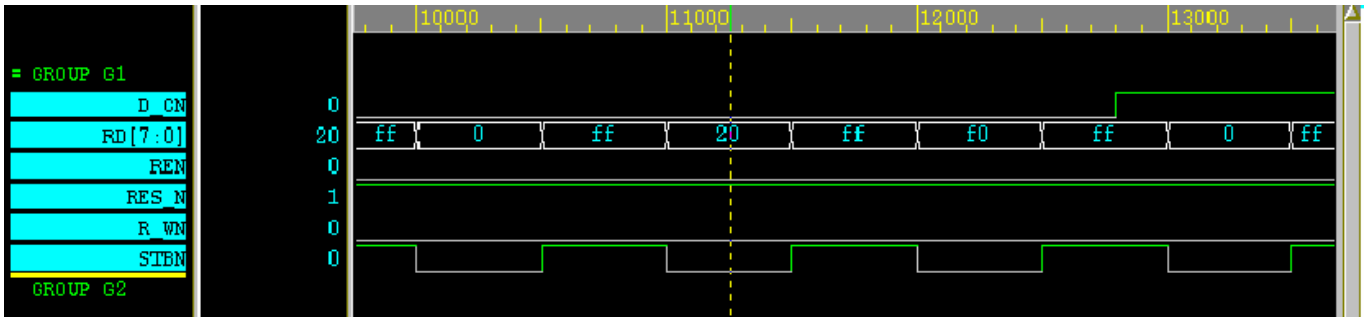
KS	Key Scan Function
0	Disable
1	Enable

6. Timing Diagram

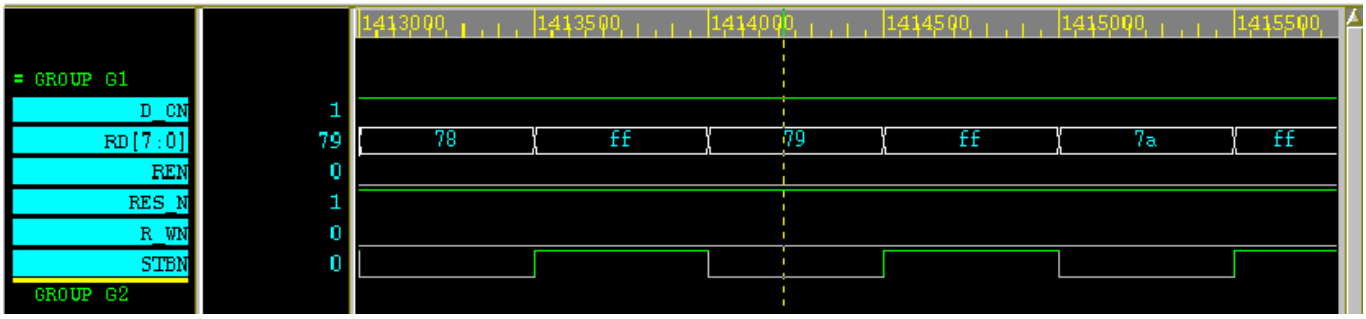
1. reset



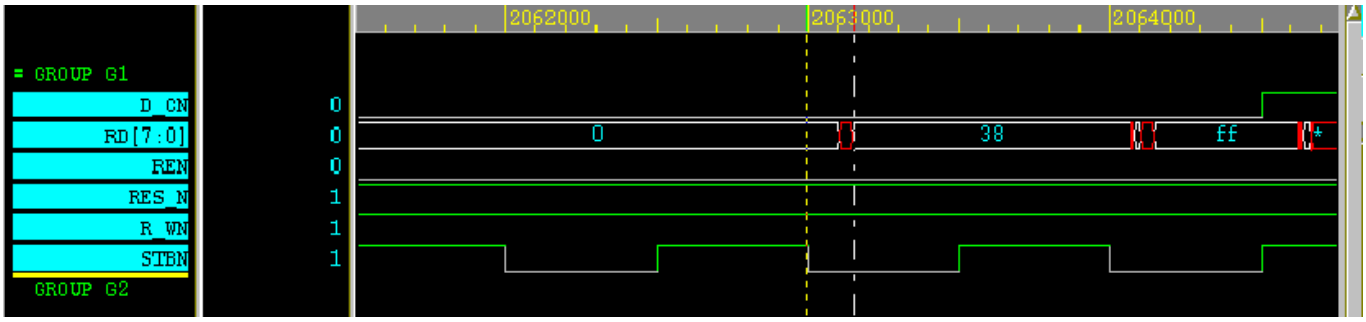
2. command_write



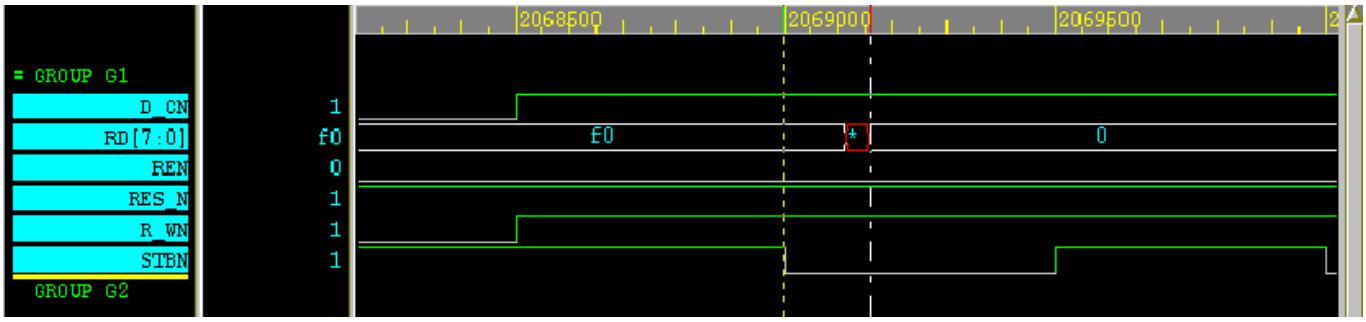
3. data write



4. command read



5. data read



7. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{DD}	-0.5V ~ 8.0V	
Input Voltage	V_{IN}	-0.5V ~ V_{DD}+0.5V	
Output Voltage	V_O	-0.5V ~ V_{DD}+0.5V	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

8. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{DD}	2.4V ~ 5.5V	
LCD operating voltage	V_{LVP}	< 8.5	
	V_{IH}	0.9 V_{DD} ~ V_{DD}	

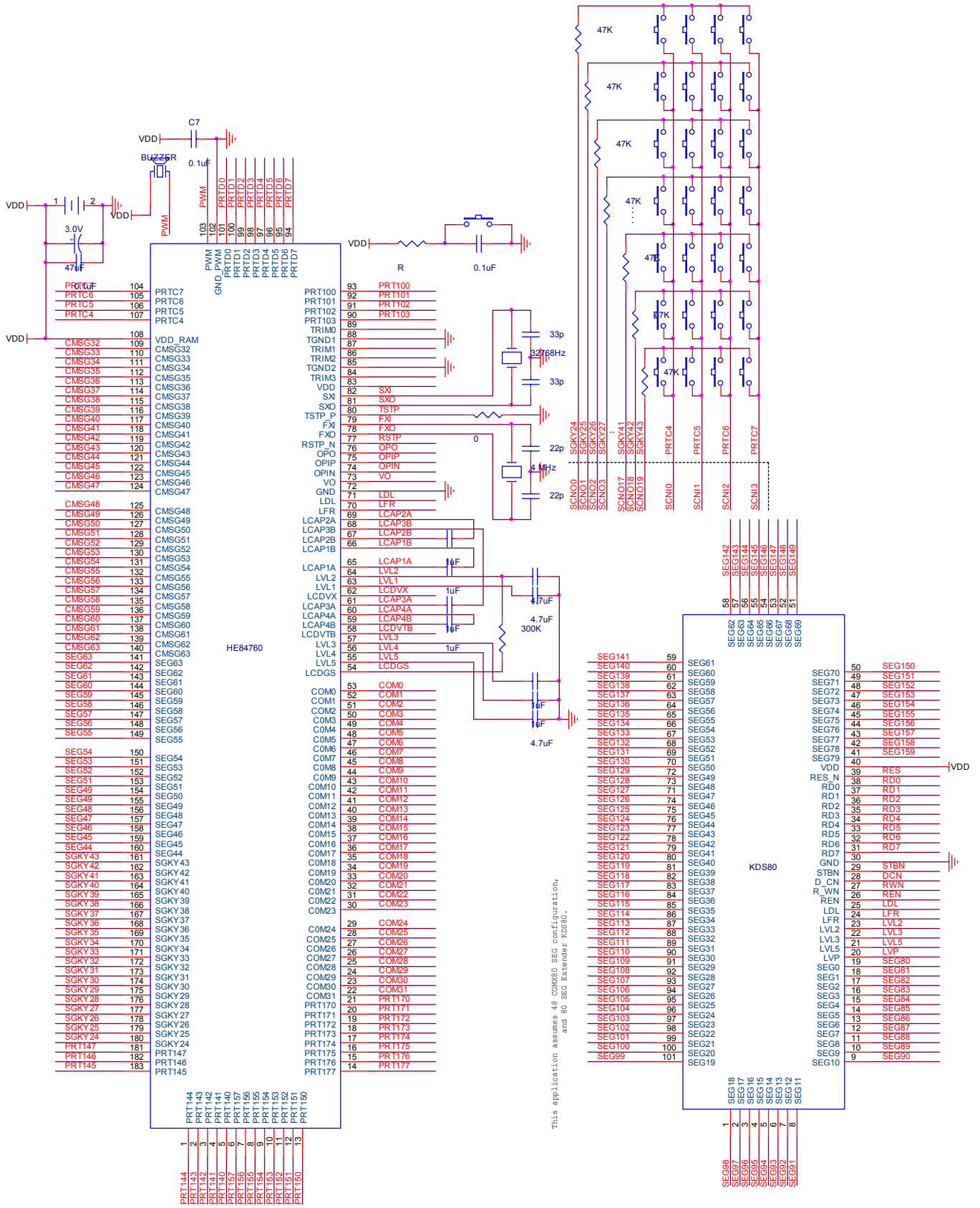
Input Voltage	V_{IH}	0.9 V_{DD} ~ V_{DD}	
	V_{IL}	0.0V ~ 0.1V_{DD}	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

9. AC/DC Characteristics

Test Condition: Temperature: 25℃, VDD: 3V±10%

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Current	I_{DD}		200	220	μA	
Standby mode current	I_{STBY}			1	μA	
Input high voltage	V_{IH}	0.8			V_{DD}	Input pins
Input low voltage	V_{IL}			0.2	V_{DD}	Input pins
Input leakage current	I_{IL}		20		μA	V_{IL} = GND, VDD
Input Hysteresis Width	V_{HYS}		1/3		V_{DD}	Input pins Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)
Output source current	I_{OH}	2.0			mA	RD[7..0], V_{OL}=2.0V
Output sink current	I_{OL}	2.0			mA	RD[7..0], V_{OL}=0.4V

10. Application Circuit



11. Updated History

Version	Date	Revised Description
V1.0	2003/10/31	KD80 is renamed from KDS80.