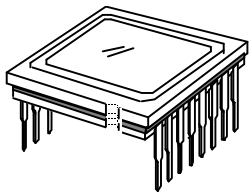
INTRODUCTION

The KC73133C is an interline transfer progressive scan type square pixel CCD area image sensor of 1/3 inch optical format developed for VGA. The electron accumulation time can be changed by the electronic shutter function and it is possible to obtain a frame still image without a mechanical shutter. High resolution and good color reproduction are accomplished by using mosaic R, G, B primary color filters. It is suitable for still cameras and PC input cameras.

16Pin Cer DIP



FEATURES

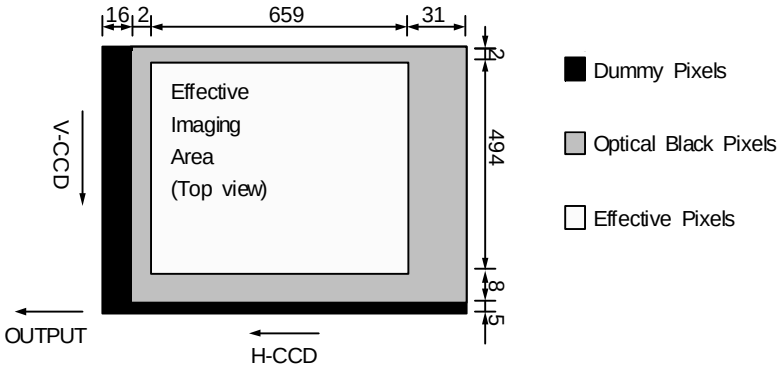
- 330K Pixel Progressive-scan CCD
- High Vertical Resolution (480 TV lines)
- Square Unit Pixel for VGA Format
- No Substrate Voltage Adjustment
- No DC bias on Reset Clock
- R, G, B Mosaic On-Chip Color Filter
- Optical Size 1/3 inch Format
- Variable Speed Electronic Shutter
- Low Smear
- High Antiblooming
- Horizontal Register 5V Drive

ORDERING INFORMATION

Device	Package	Operating
KC73133C	16Pin Cer DIP 450mil	-10 °C ~ +60 °C

STRUCTURE

- Number of Total Pixels: 692(H) × 504(V)
- Number of Effective Pixels: 659(H) × 494(V)
- Chip Size: 6.00mm(H) × 4.95mm(V)
- Unit Pixel Size: 7.40μm(H) × 7.40μm(V)
- Optical Blacks & Dummies: Refer to Figure Below



BLOCK DIAGRAM

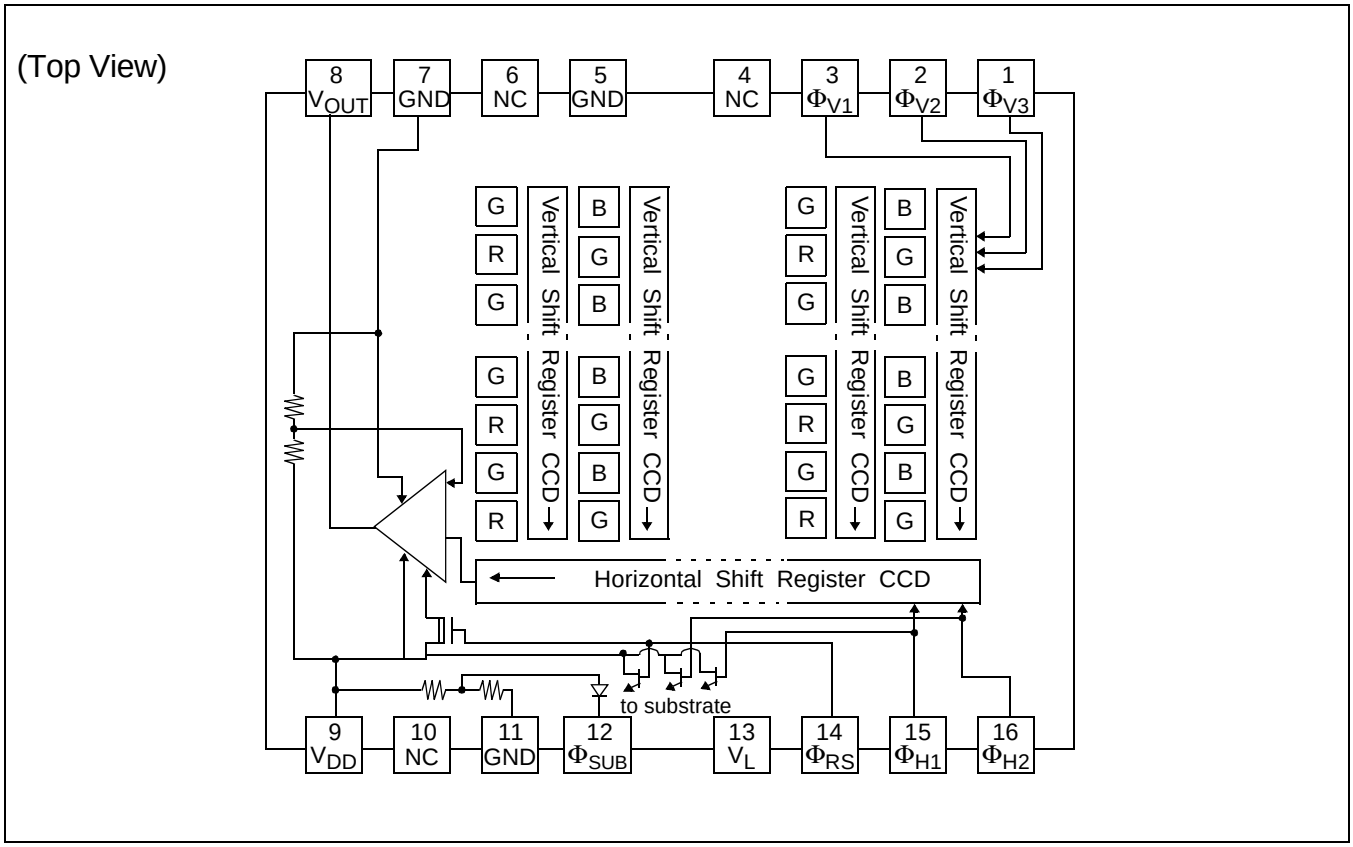


Figure 1. Block Diagram

PIN DESCRIPTION

Table 1. Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	Φ_{V3}	Vertical CCD transfer clock 3	9	V_{DD}	Output stage drain bias
2	Φ_{V2}	Vertical CCD transfer clock 2	10	NC	No connection
3	Φ_{V1}	Vertical CCD transfer clock 1	11	GND	Ground
4	NC	No connection	12	Φ_{SUB}	Substrate clock
5	GND	Ground	13	V_L	Protection circuit bias
6	NC	No connection	14	Φ_{RS}	Reset gate clock
7	GND	Ground	15	Φ_{H1}	Horizontal CCD transfer
8	V_{OUT}	Signal output	16	Φ_{H2}	Horizontal CCD transfer

ABSOLUTE MAXIMUM RATINGS (1)

Table 2. Absolute Maximum Ratings

Characteristics	Symbols	Min.	Max.	Unit
Substrate clock voltage	Φ_{SUB} - GND	-0.3	40	V
	Φ_{SUB} - V_{DD}	-0.3	40	V
	Φ_{SUB} - V_{OUT}	-0.3	40	V
Supply voltage	V_{DD}, V_{OUT} - GND	-0.3	17	V
Vertical clock input voltage	Φ_{V1} - V_L	-0.3	17	V
	Φ_{V2}, Φ_{V3} - V_L	-0.3	32	V
	Φ_{V1} - Φ_{SUB}	-40	17 (2)	V
	$\Phi_{V2,}$ Φ_{V3} - Φ_{SUB}	-40	32	V
Horizontal clock input voltage	Φ_{H1}, Φ_{H2} - GND	-0.3	17	V
	Φ_{H1}, Φ_{H2} - V_L	-0.3	17	V
	Φ_{H1}, Φ_{H2} - Φ_{SUB}	-40	substrate DC bias (3)	V
Output clock input voltage	Φ_{RS} - V_L	-0.3	17	V
	Φ_{RS} - Φ_{SUB}	-40	substrate DC bias (2)	V
	Φ_{RS} - GND	-0.3	17 (2)	V
Protection circuit bias voltage	Φ_{SUB} - V_L	-16	40	V
	GND - V_L	-0.3	17	V
Operating temperature	T_{OP}	-10	60	°C
Storage temperature	T_{STG}	-30	80	°C

NOTE:

1. The device can be destroyed, if the applied voltage or temperature is higher than the absolute maximum rating voltage or temperature.
2. V_{DD} bias must be operated before reset pulse operation.
3. Substrate DC bias(OFD bias) must be operated before horizontal, reset pulse operation.

DC CHARACTERISTICS

Table 3. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Output stage drain bias	V_{DD}	14.55	15.0	15.45	V	
Protection circuit bias voltage	V_L	The lowest vertical clock level				
Substrate clock	Φ_{SUB}	NOTE			V	
Output stage drain current	I_{DD}		5.0		mA	

NOTE: A DC bias (OFD bias) is generated within the CCD.

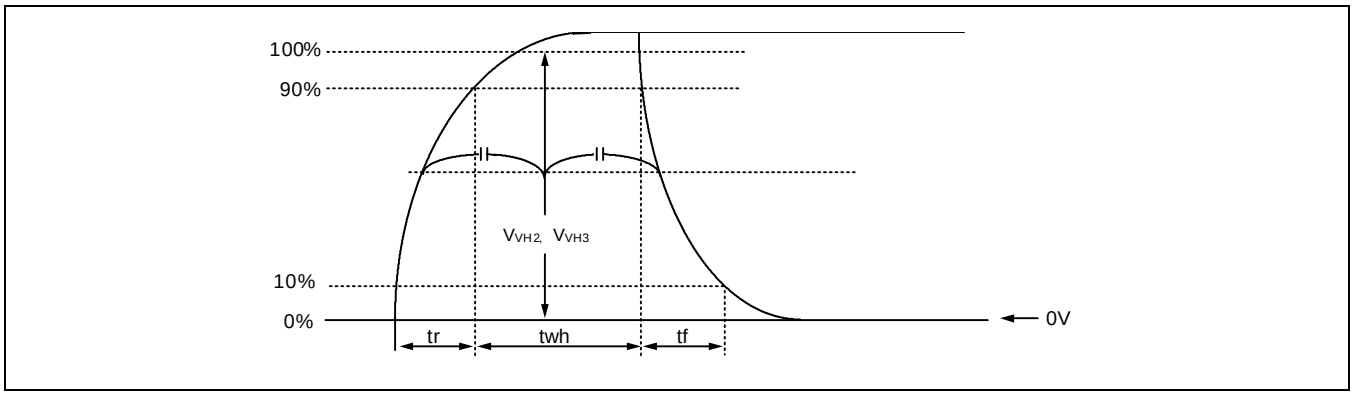
CLOCK VOLTAGE CONDITIONS

Table 4. Clock Voltage Conditions

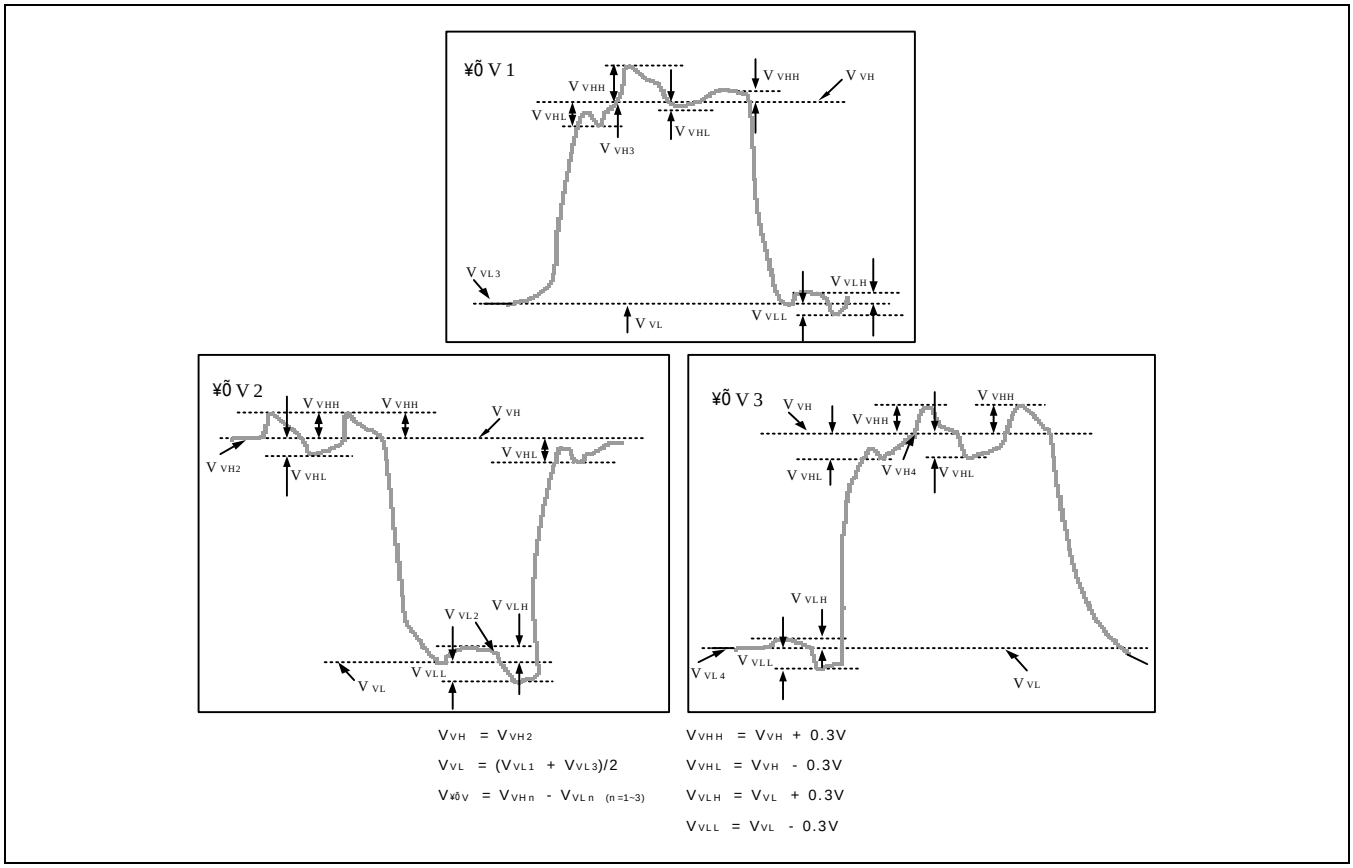
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Read-out clock voltage	V_{VH2}, V_{VH3}	14.55	15.0	15.45	V	High
Vertical transfer clock voltage	V_{VM1} ~ V_{VM3}	-0.05	0.0	0.05	V	Middle
	V_{VL1} ~ V_{VL3}	-8.0	-7.5	-7.0	V	Low
Horizontal transfer clock voltage	V_{HH1}, V_{HH2}	4.75	5.0	5.25	V	High
	V_{HL1}, V_{HL2}	-0.05	0.0	0.05	V	Low
Charge reset clock voltage	V_{RSH}	4.75	5.0	5.25	V	High
	V_{RSL}	-0.05	0.0	0.05	V	Low
Substrate clock voltage	$V_{\Phi SUB}$	21.5	22.5	23.5	V	Shutter

DRIVE CLOCK WAVEFORM CONDITIONS

Read Out Clock Waveform



Vertical Transfer Clock Waveform



$V_{VH} = V_{VH2}$

$V_{VL} = (V_{VL1} + V_{VL3})/2$

$V_{¥õV} = V_{VHn} - V_{VLn}$ (n=1~3)

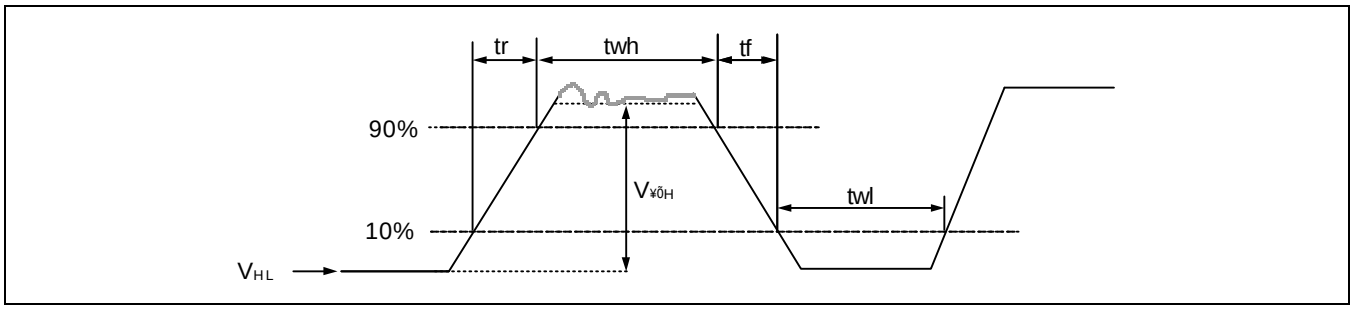
$V_{VHH} = V_{VH} + 0.3V$

$V_{VHL} = V_{VH} - 0.3V$

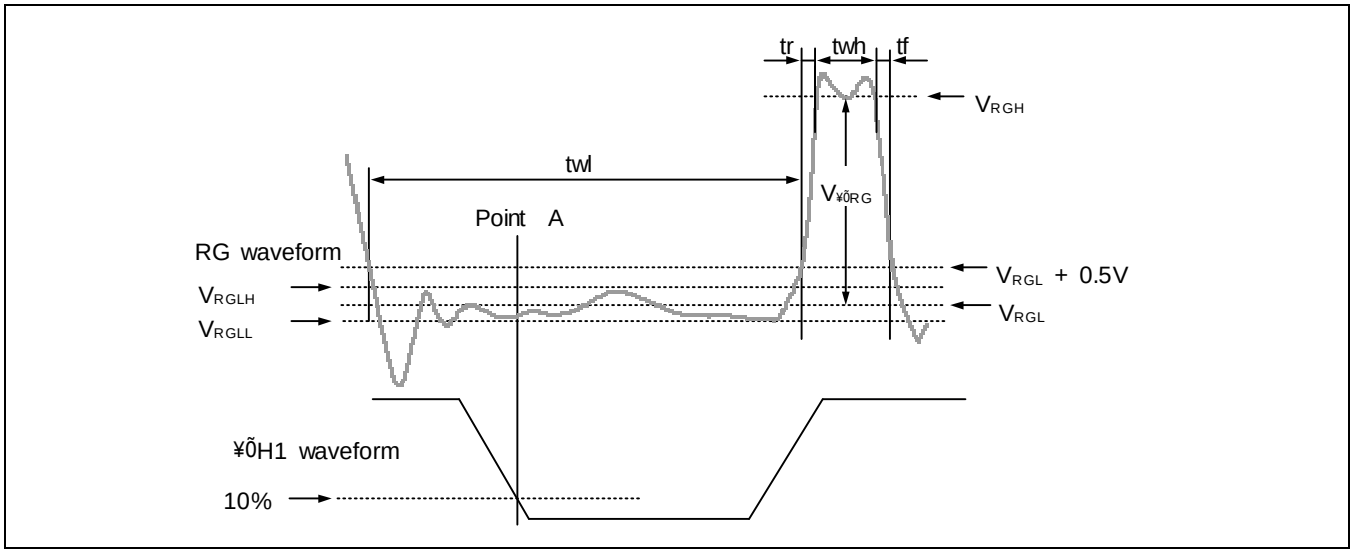
$V_{VLH} = V_{VL} + 0.3V$

$V_{VLL} = V_{VL} - 0.3V$

Horizontal Transfer Clock Waveform Diagram



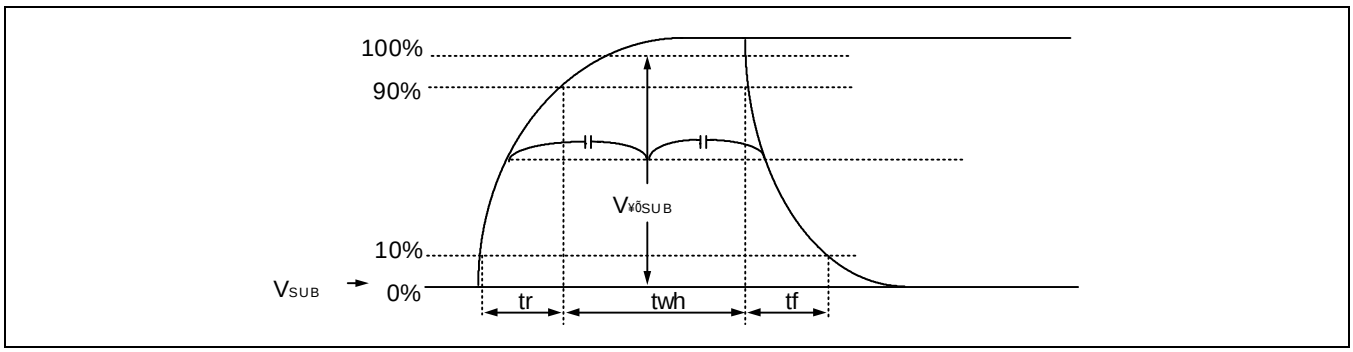
Reset Gate Clock Waveform Diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram about to R_G rise

$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$, $V_{FRG} = V_{RGH} - V_{RGL}$

Substrate Clock Waveform



SAMSUNG ELECTRONICS

CLOCK EQUIVALENT CIRCUIT CONSTANT

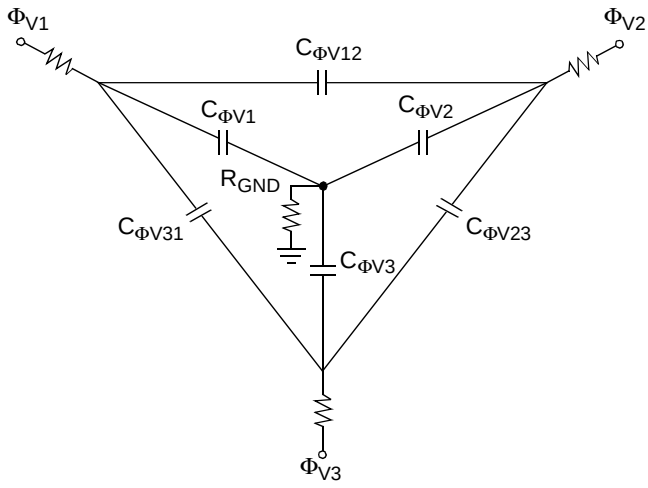
Table 5. Clock Equivalent Circuit Constant

Item	Symbol	twh			twl			tr			tf			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Read-out clock	Φ_{VH}	2.3	2.5						0.5			0.5		μs
Vertical clock	Φ_{V1}, Φ_{V2} Φ_{V3}										15		350	ns
Horizontal clock	Φ_{H1}	24	30		25	31.5			10	17.5		10	17.5	ns
	Φ_{H2}	26.5	31.5		25	30			10	15		10	15	ns
Reset clock	Φ_{RG}	11	13			62.5			3			3		ns
Substrate clock	Φ_{SUB}	1.5	1.8							0.5			0.5	μs

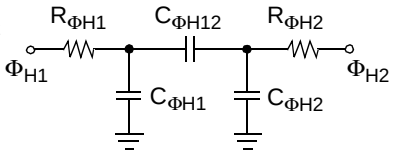
EQUIVALENT CIRCUIT PARAMETERS

Table 6. Equivalent Circuit Parameters

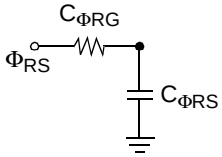
Item	Symbol	Typ.	Unit
Capacitance between vertical transfer clock and GND	$C_{\Phi V1}$	1,700	pF
	$C_{\Phi V2}$	1,700	pF
	$C_{\Phi V3}$	2,100	pF
Capacitance between vertical transfer clocks	$C_{\Phi V12}$	2,700	pF
	$C_{\Phi V23}$	2,100	pF
	$C_{\Phi V31}$	1,100	pF
Capacitance between horizontal transfer clock and GND	$C_{\Phi H1}$, $C_{\Phi H2}$	117	pF
Capacitance between horizontal transfer clocks	$C_{\Phi H12}$	39	pF
Capacitance between reset gate clock and GND	$C_{\Phi RS}$	10	pF
Vertical transfer clock serial resistor	$R_{\Phi V1}$, $R_{\Phi V2}$	30	Ω
	$R_{\Phi V3}$	25	Ω
Horizon tal transfer clock serial resistor	$C_{\Phi H1}$, $C_{\Phi H2}$	10	Ω
Reset gate clock serial resistor	$R_{\Phi RS}$	100	Ω
Vertical transfer clock ground resistor	R_{GND}	15	Ω



Vertical Clock Equivalent Circuit



Horizontal Clock Equivalent Circuit



Reset Clock Equivalent Circuit

SAMSUNG ELECTRONICS

OPERATING CHARACTERISTICS

Device Temperature = 25 °C

Table 7. Operating Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
G sensitivity	Sg	38	45		mV/lux	1
Sensitivity ratio	Rr	0.3	0.45	0.6		1
	Rb	0.4	0.55	0.7		
Saturation signal	Y_{SAT}	550			mV	2
Smear	SM		0.005	0.015		3
Blooming margin	BM	1,000			times	4
Uniformity	U			20	%	5
Dark signal (NOTE)	D			2	mV	6
Dark shading (NOTE)	ΔD			1	mV	7
Color uniformity	DS_{Gr}, DS_{Gb}			8	%	8
Line stripe W, R, G, B	L_{CG}, L_{CR}, L_{CB}			3.8	%	9

NOTE: Test Temperature = 60 °C

TESTING SYSTEM

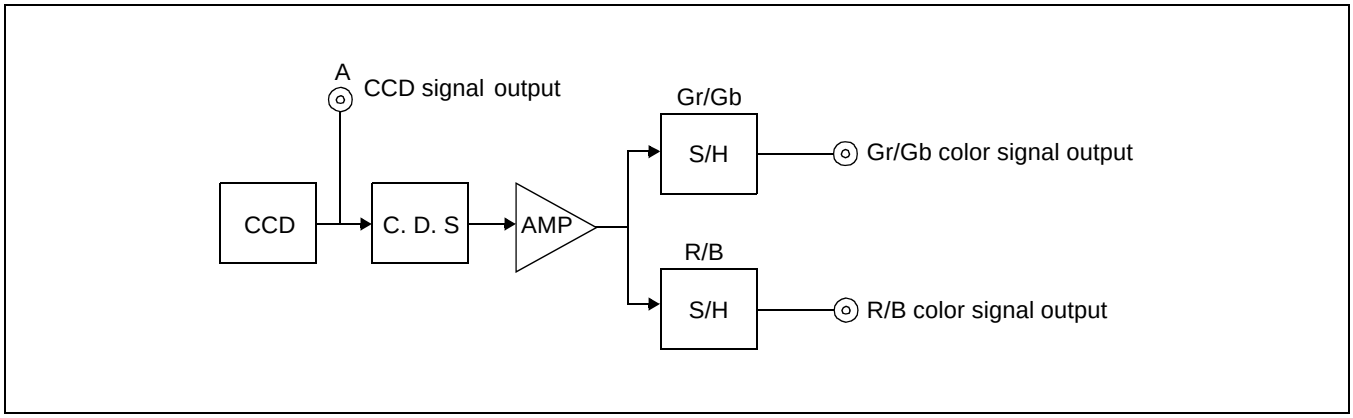


Figure 2. Testing System

TEST CONDITION

1. Use a light source with color temperature of 3,200K hallogen lamp and CM-500S for IR cut filter.
   The light source is adjusted in accordance with the average value of Y signals indicated in each item.

COLOR FILTER ARRAY

The color filter array of this image sensor is shown below. This primary mosaic CFA is used with the operation of frame mode, where all of the photosensors are read out sequencially.

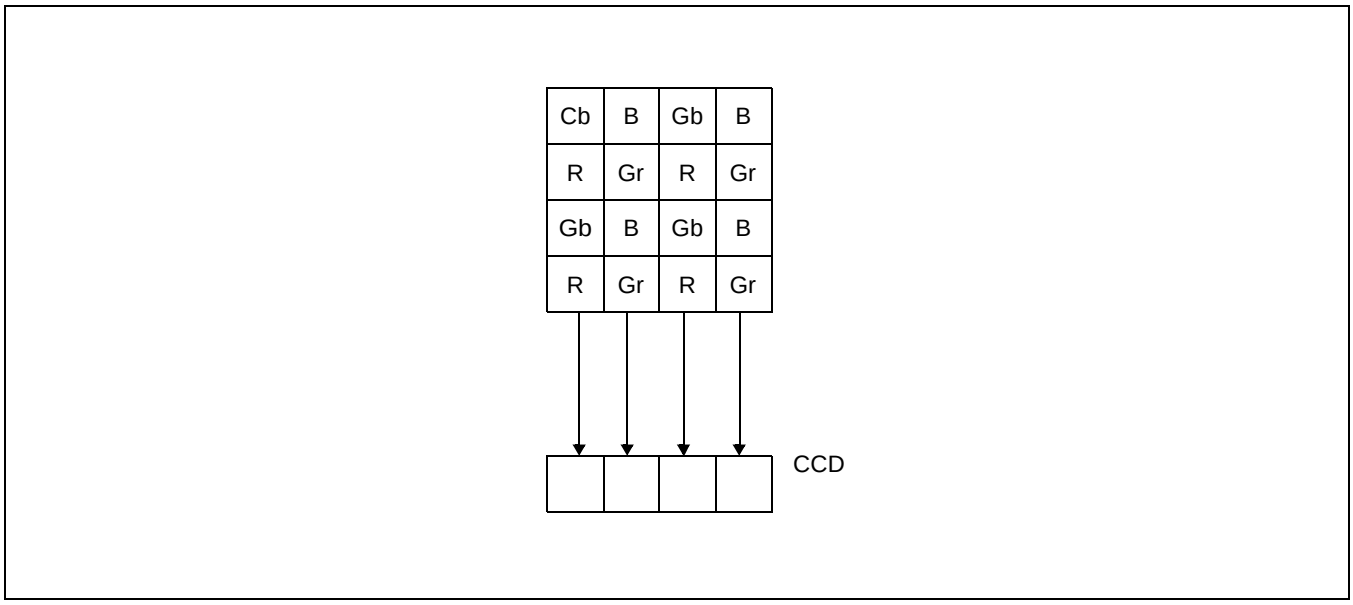


Figure 3. Color Filter Array

TEST METHODS

1. Measure the light intensities(L) when the average illuminance output value(Y) of green pixels Gr is equal to the standard illuminance output value of 150mV (Y_A), and when it is equal to half of 150mV, 1/2 $\times Y_A$. repeat for Gb. and calculate Sgr, Sgb, and Sg.

$$S_{gr} = \frac{Y_A - \frac{1}{2}Y_A}{L_{YA} - L_{\frac{1}{2}YA}},\ S_{gb} = \frac{Y_A - \frac{1}{2}Y_A}{L_{YA} - L_{\frac{1}{2}YA}},\ S_g = S_{gr} + S_{gb}$$

The sensitivities for red and blue pixels, Sr and Sb, are also measured in the same way.

$$R_r = \frac{S_r}{S_g},\ R_b = \frac{S_b}{S_g}$$

2. Adjust the light intensity to 15 times of the value with which Y is Y_A, then measure the averaged illuminance output value (Y = Y_{SAT}).

3. When the Gr pixel signal value, Ygr is 150mV, mearsure the Gb, R, B pixel signal values, Ygb, Yr, and Yb respectively. Adjust the light intensity until 500 times of the illumination under which 150 mV of Gr pixels value is obtained, is reached. Remove the read-out clock and drain the signal in photosensors by electronic shutter operation during the horizontal blanking time without changing other clocks. Measure the maximum output value YSM regardless of the pixel type..

$$SM = Y_{SM} \div \frac{Y_{gr} + Y_{gb} + Y_r + Y_b}{4} \times \frac{1}{500} \times \frac{1}{10} \times 100(\%)$$

4. Measure the light intensity(L_{BM}) on which the Y signal output value of the optical black pixels (OBP) is rapidly increased with the increasing light intensity.

$$BM = \frac{L_{BM}}{L_{YA}}$$

5. Measure the maximum and minimum illuminance output value (Y_{MAX}, Y_{MIN}) when the light intensity is adjusted to make Y to be Y_A.

$$U = \frac{Y_{MAX} - Y_{MIN}}{Y_A} \times 100(\%)$$

6. Measure Y_D with the horizontal idling time transfer level as reference, when the device ambient temperature is 60 °C and all of the light sources are shielded.

7. Follow test method 6, measure the maximum (D_{MAX}) and minimum illuminance output (D_{MIN}).

$$\Delta D = D_{MAX} - D_{MIN}$$

8. When the Gr pixel signal value is 150mV, measure the maximum and minimum output pixel values ($Y_{MAX(Gr)}$), $Y_{MIN(Gr)}$), Repeat for Gb, R, B under the each pixel value,150mV

$$DSi = \frac{Y_{MAX(i)} + Y_{MIN(i)}}{Y_i} \times 100(\%)$$

where i = Gr, Gb, R, B

9. Adjust the light intensity to make the each pixel value, 150mV, using red(R), green(G) and blue(B) optical filters respectively and measure the differences (ΔY_R, ΔY_G, ΔY_B) between the signal lines.

$$Lci = \frac{\Delta Y_i}{150mV} \times 100(\%)$$

where i = R, G, B

SPECTRAL RESPONSE CHARACTERISTICS

Excluding Light Source Characteristics

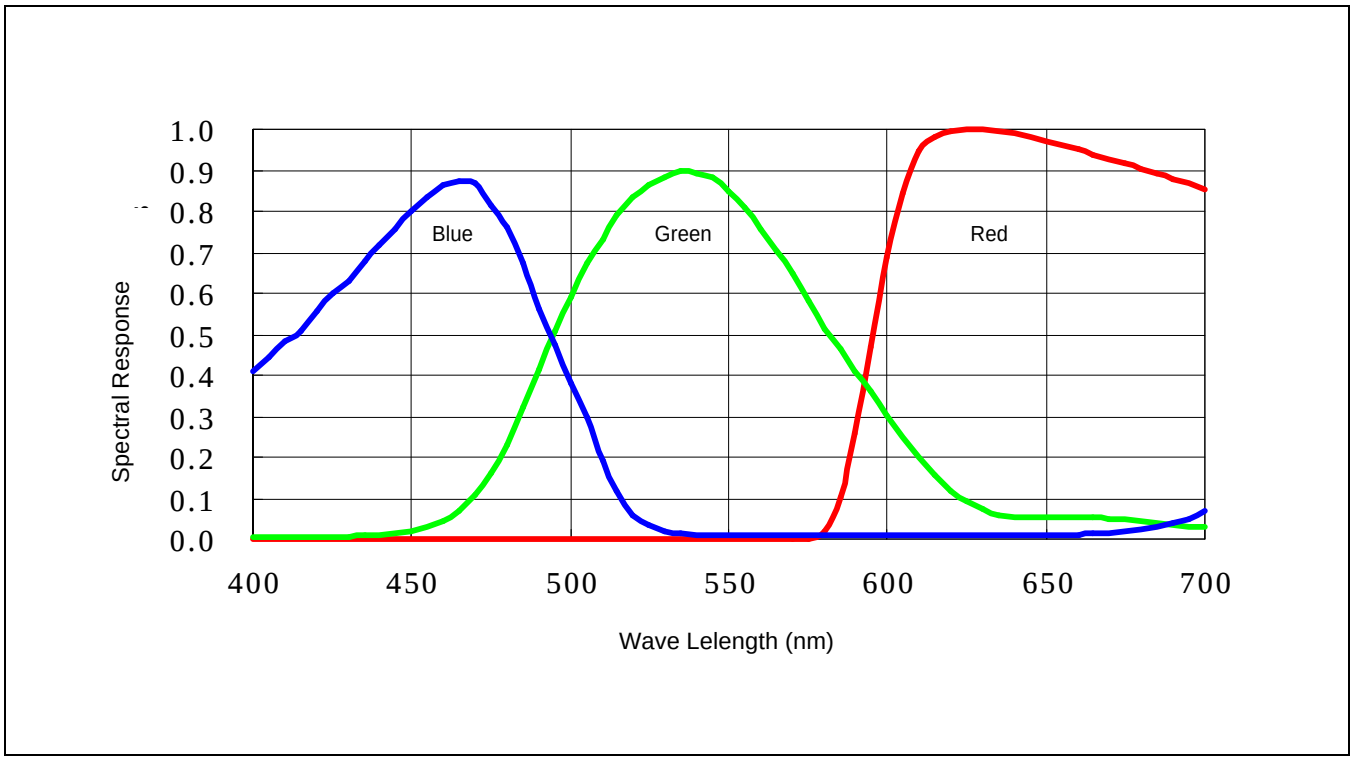


Figure 4. Spectral Response Characteristics

APPLICATION CIRCUITS

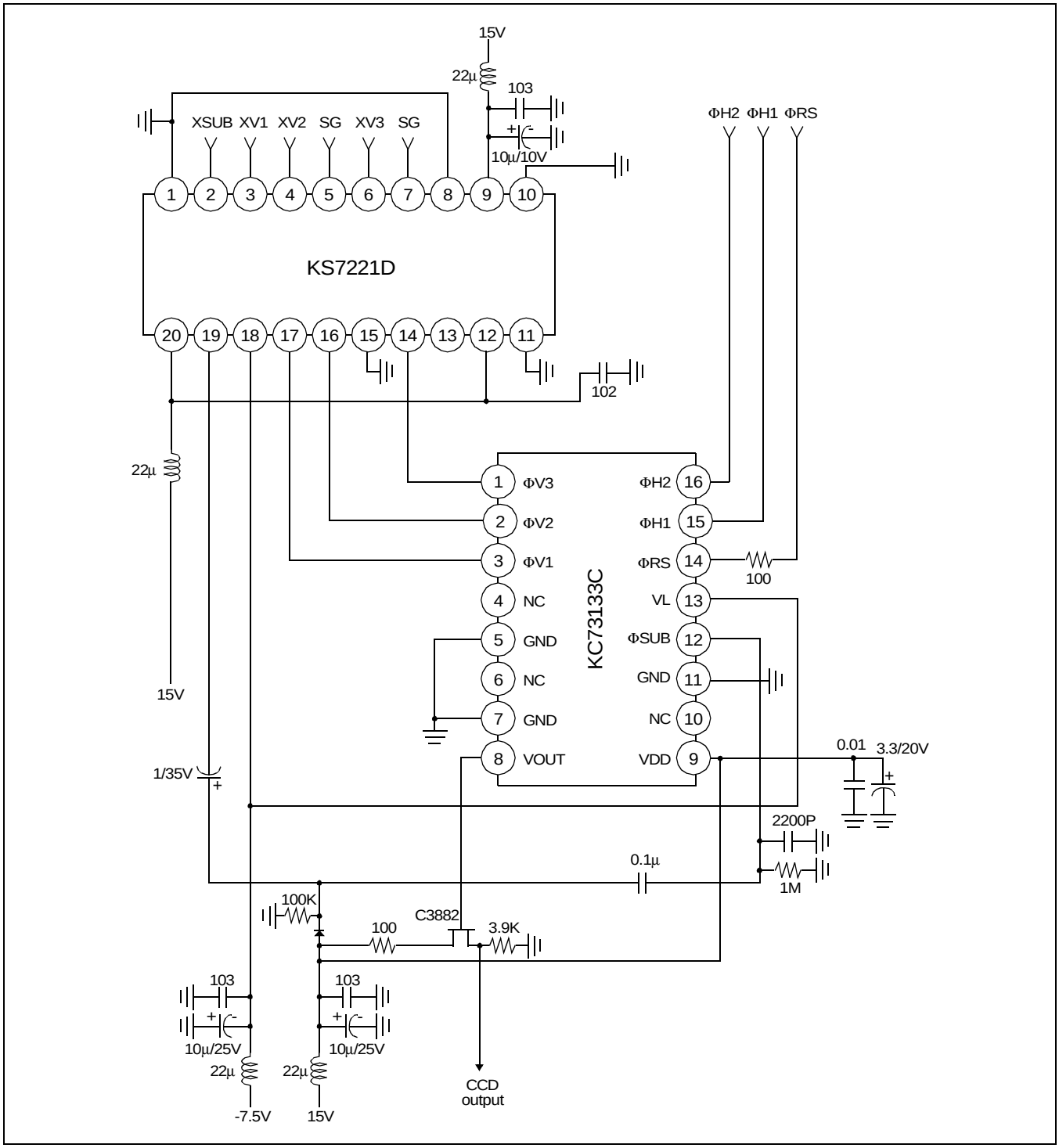


Figure 5. Application Circuits

READ-OUT CLOCK TIMING CHART

1/30 sec noninterlace transfer

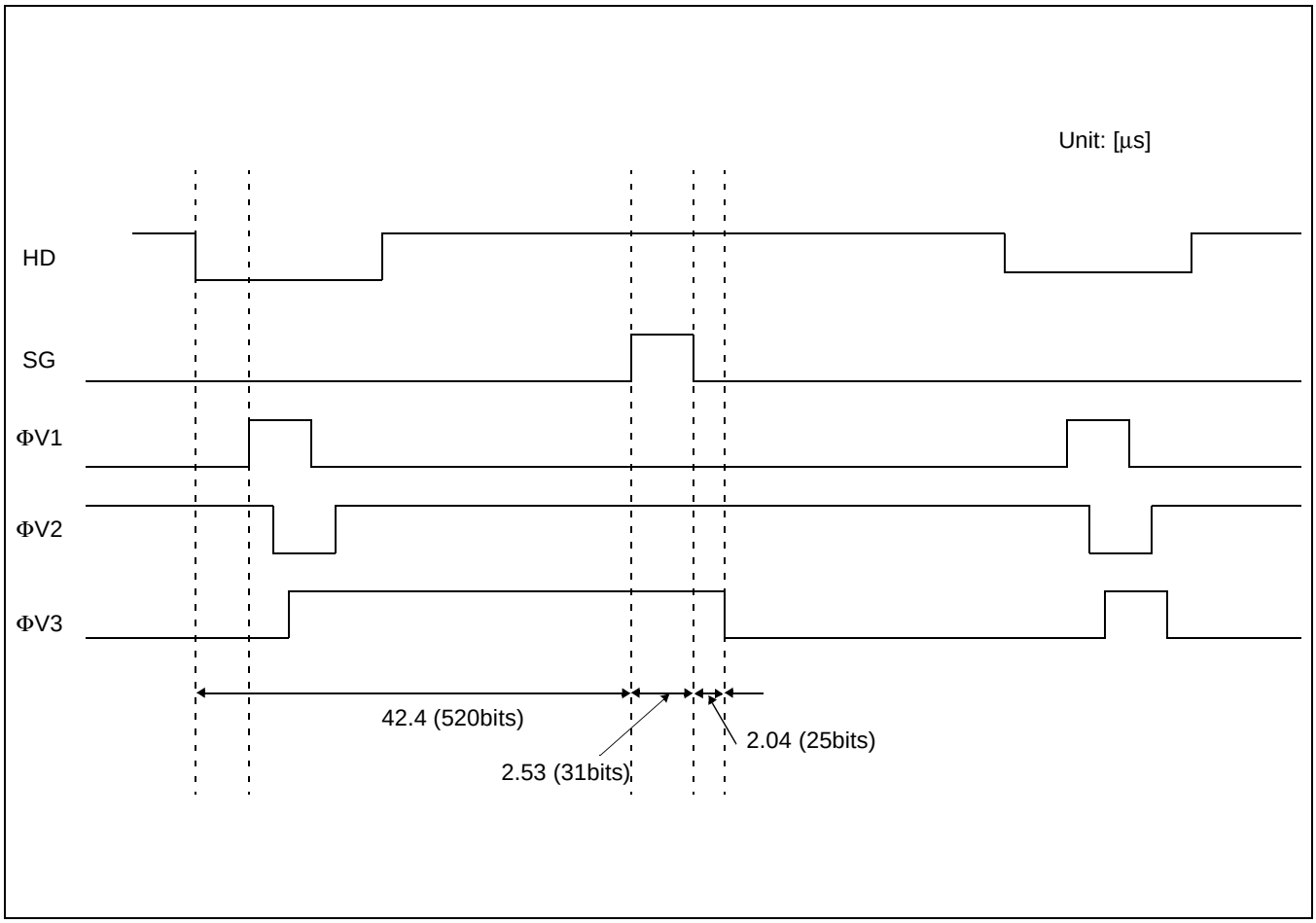


Figure 6. Read-out Clock Timing Chart

CLOCK TIMING CHART (VERTICAL SYNC.)

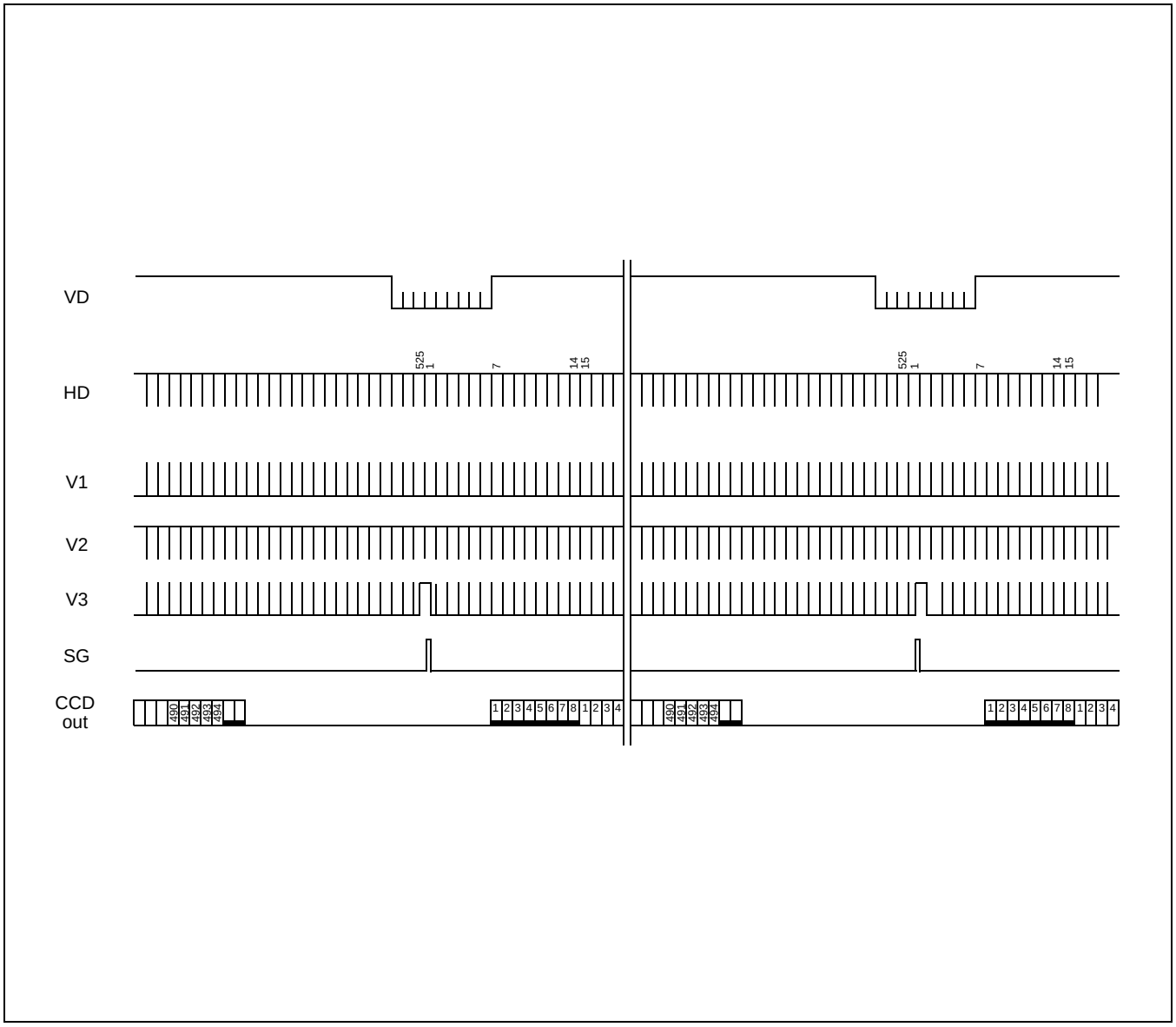


Figure 7. Clock Timing Chart (Vertical Sync.)

CLOCK TIMING CHART (HORIZONTAL SYNC.)

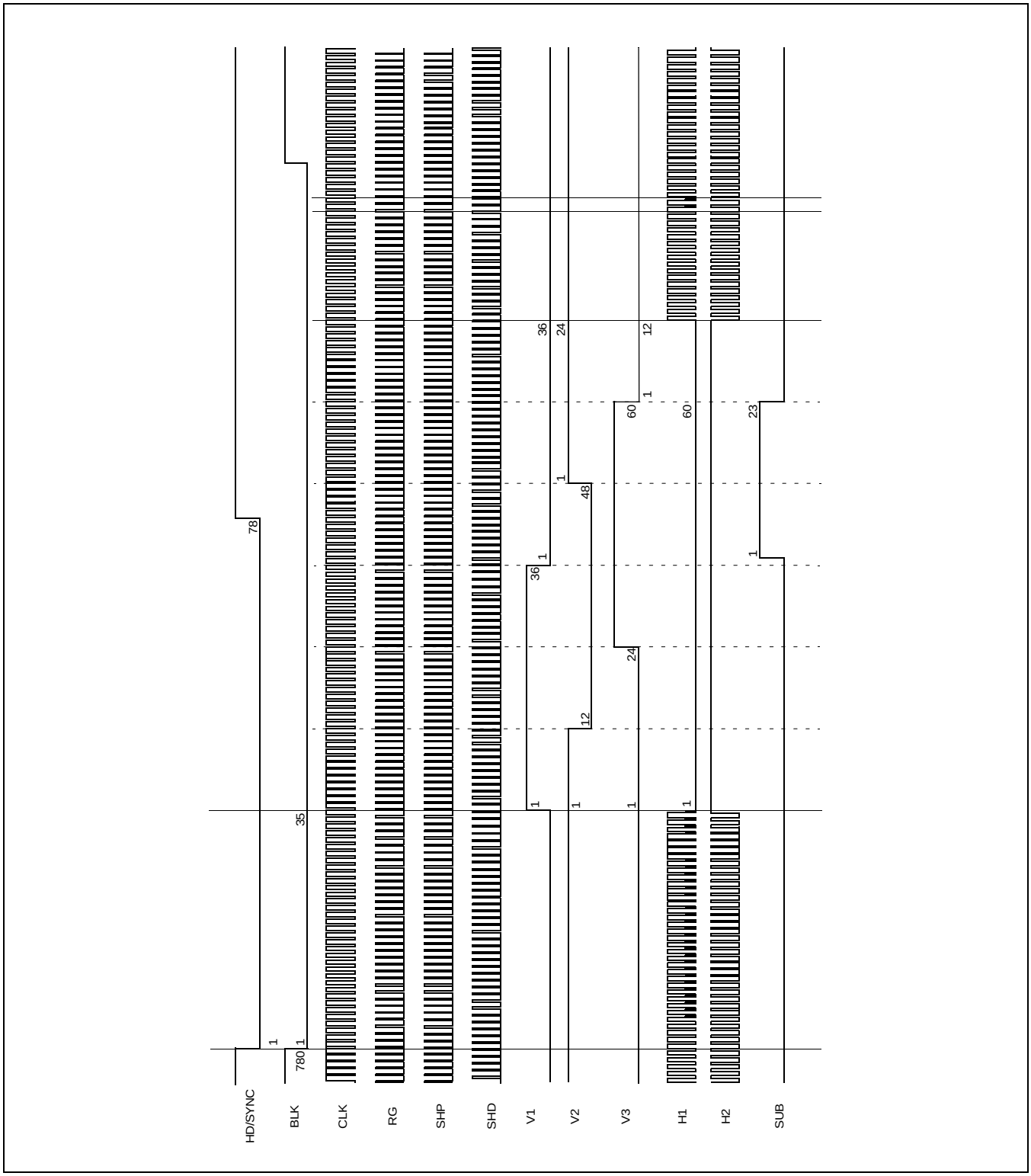


Figure 8. Clock Timing Chart (Horizontal Sync.)

PACKAGE DIMENSIONS

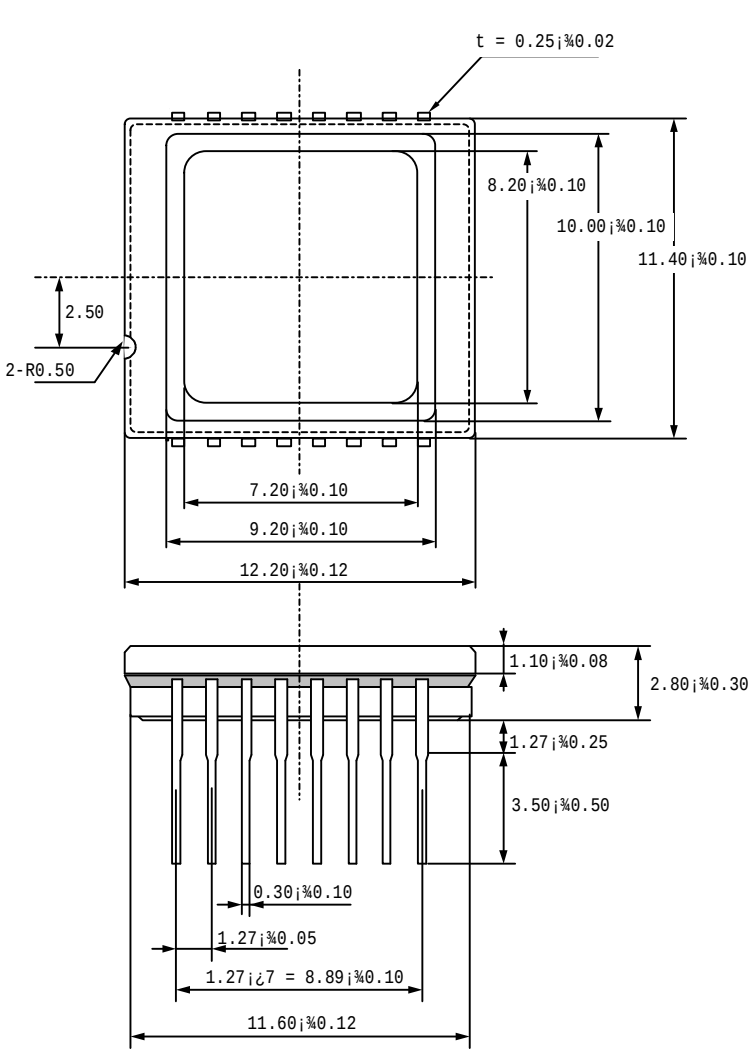


Figure 9. Package Dimensions

SAMSUNG ELECTRONICS

HANDLING INSTRUCTIONS

- Static Charge Prevention

  CCD image sensors can be easily damaged by static discharge. Before handling, be sure to take the following protective measures.

  — Use non chargeable gloves, clothes or material. Also use conductive shoes.
  — When handling directly, use an earth band.
  — Install a conductive mat on the floor or working table to prevent generation of static electricity.
  — Ionized air is recommended for discharging when handling CCD image sensor.
  — For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

- Soldering
  — Make sure the package temperature does not exceed 80 °C.
  — Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and and remount, cool sufficiently.
  — To dismount an imaging device, do not use a solder suction equipment. When using an electronic disoldering tool, use a thermal controller of the zero cross on/off type and connect to ground.

- Dust and Dirt Protection
  — Operate in the clean environments (around class 1000 will be appropriate).
  — Do not either touch glass plates by hand or have object come in contact with glass surface. Should dirt stick to a glass surface blow it off with an air blow (for dirt stuck through static electricity ionized air is recommended).
  — Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be caerful not to scratch the glass.
  — Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
  — When a protective tape is applied before shipping, just before use remove the tape applied electrostatic protection. Do not reuse the tape.

- Do not expose to strong light (sun rays) for long period, color filter are discolored.

- Exposure to high temperature or humidity will affect the characteristics. accordingly avoid storage or usage in such conditions.

- CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.