

Document Title**256Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	March 16, 2000	Preliminary
1.0	Finalized	April 20, 2000	Final
1.01	Errata correction - Removed TTL Compatible'from Features	October 26, 2001	Final

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256K x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 256K x16 bit
- Power Supply Voltage: 3.0~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs
- Package Type: 48-FBGA-6.10x8.50

GENERAL DESCRIPTION

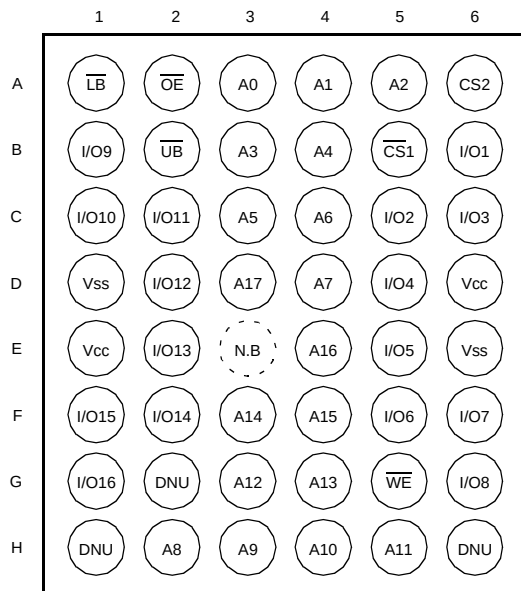
The K6F4016V6D families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{sb1} , Typ.)	Operating (I _{cc1} , Max)	
K6F4016V6D-F	Industrial(-40~85°C)	3.0~3.6V	55 ¹⁾ /70ns	0.5μA	4mA	48-FBGA-6.10x8.50

1. The parameter is measured with 30pF test load.

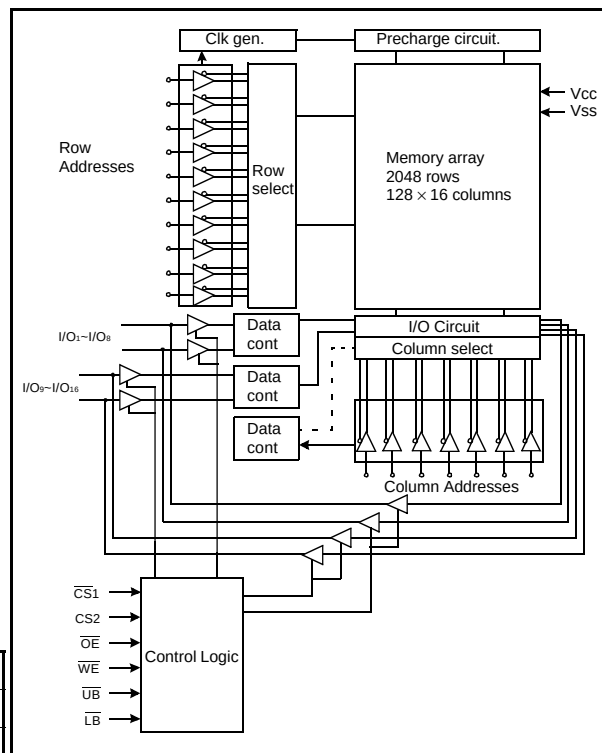
PIN DESCRIPTION



48-FBGA: Top View (Ball Down)

Name	Function	Name	Function
$\overline{CS_1}$, CS_2	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O ₉₋₁₆)
A ₀ –A ₁₇	Address Inputs	$\overline{LB}$	Lower Byte(I/O ₁₋₈)
I/O ₁ –I/O ₁₆	Data Inputs/Outputs	DNU	Do Not Use
N.B	No Ball		

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F4016V6D-FF55 K6F4016V6D-FF70	48-FBGA, 55ns, 3.3V 48-FBGA, 70ns, 3.3V

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.5V	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 4.6V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	-0.3 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	2	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	45	mA
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V($\overline{CS}_1$ controlled) or CS ₂ ≤0.2V(CS ₂ controlled), Other inputs=0~V _{CC}	-	0.5	15 ¹⁾	μA

1. Super low power product=7μA with special handling.

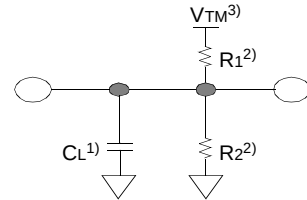
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (See right): $C_L = 100\text{pF} + 1\text{TTL}$ $C_L = 30\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$ 3. $V_{TM} = 2.8\text{V}$ AC CHARACTERISTICS ($V_{CC} = 3.0 \sim 3.6\text{V}$, Industrial product: $T_A = -40$ to 85°C)

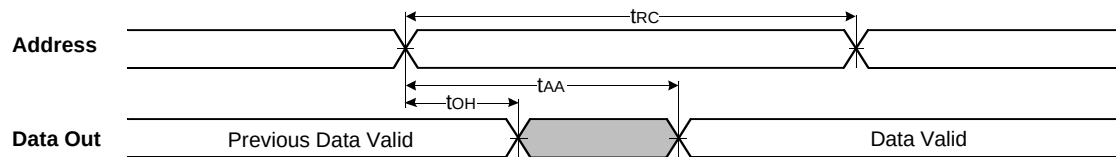
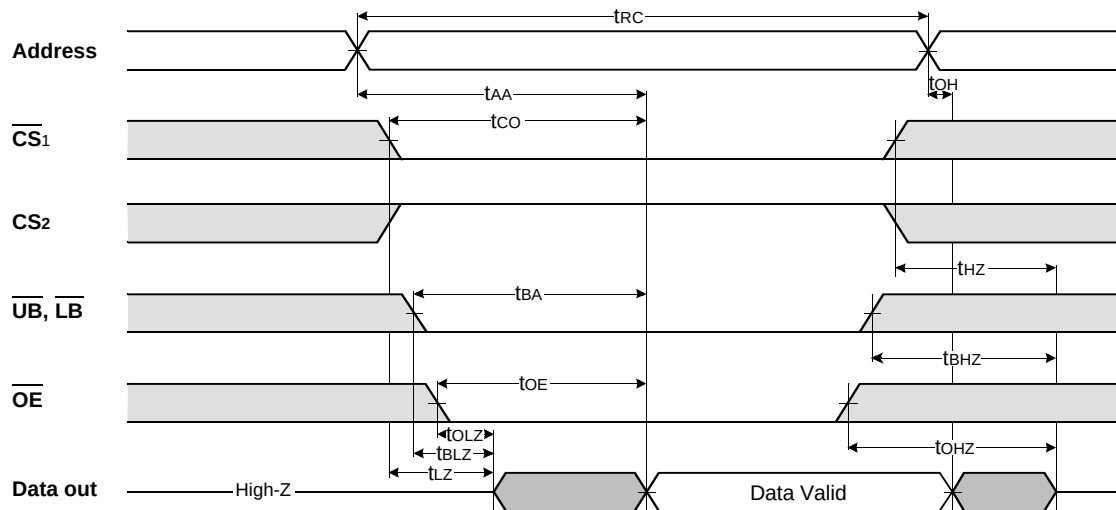
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t _{RC}	55	-	70	-	ns
	Address Access Time	t _{AA}	-	55	-	70	ns
	Chip Select to Output	t _{CO}	-	55	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	25	-	35	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	55	-	70	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Enable to Low-Z Output	t _{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	20	0	25	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Disable to High-Z Output	t _{BHZ}	0	20	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	20	0	25	ns
	Output Hold from Address Change	t _{OH}	10	-	10	-	ns
Write	Write Cycle Time	t _{WC}	55	-	70	-	ns
	Chip Select to End of Write	t _{CW}	45	-	60	-	ns
	Address Set-up Time	t _{AS}	0	-	0	-	ns
	Address Valid to End of Write	t _{AW}	45	-	60	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	45	-	60	-	ns
	Write Pulse Width	t _{WP}	40	-	50	-	ns
	Write Recovery Time	t _{WR}	0	-	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	20	0	20	ns
	Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
	Data Hold from Write Time	t _{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	VDR	$\overline{\text{CS}}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	1.5	-	3.6	V
Data retention current	IDR	$V_{CC} = 1.5\text{V}$, $\overline{\text{CS}}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	-	1	3 ⁽²⁾	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t _{RDR}		t _{RC}	-	-	

1. $\overline{\text{CS}}_1 \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS}}_2 \geq V_{CC} - 0.2\text{V}$ ($\overline{\text{CS}}_1$ controlled) or $\overline{\text{CS}}_2 \leq 0.2\text{V}$ ($\overline{\text{CS}}_2$ controlled).2. Super low power product = $2\mu\text{A}$ with special handling.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES (READ CYCLE)

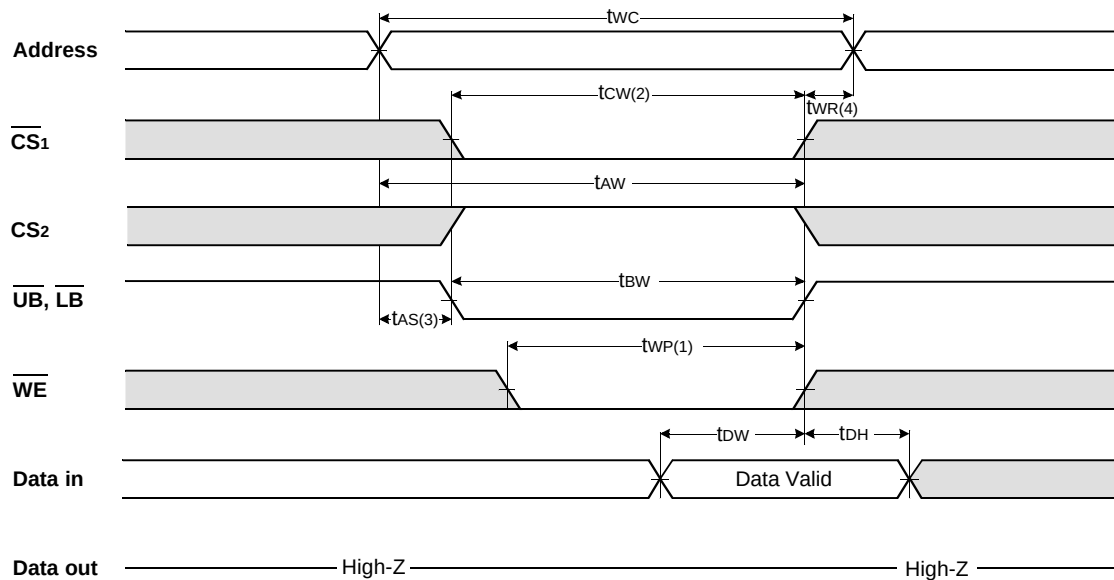
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

The diagram illustrates the timing relationships for the 74VHC04-00. The signals shown are Address, CS1, CS2, UB, LB, WE, Data in, and Data out. The timing parameters are defined as follows:

- Address:** The signal is active during the t_{WC} (Write Cycle) period.
- CS1:** The signal is active during the $t_{CW(2)}$ (Chip Select 1 to Write Cycle) period.
- CS2:** The signal is active during the $t_{WR(4)}$ (Chip Select 2 to Write Cycle) period.
- UB, LB:** The signals are active during the t_{AW} (Address Valid to Write Cycle) and t_{BW} (Data Valid to Write Cycle) periods.
- WE:** The signal is active during the $t_{WP(1)}$ (Write Enable to Write Cycle) period.
- Data in:** The signal is High-Z during the $t_{AS(3)}$ (Address Strobe to Write Cycle) period. It becomes Data Valid during the t_{DW} (Data Valid to Write Cycle) period and returns to High-Z during the t_{DH} (Data Hold to Write Cycle) period.
- Data out:** The signal is Data Undefined during the t_{WHZ} (Write Hold to High-Z) period. It becomes Data Valid during the t_{OW} (Output Valid to Write Cycle) period and returns to High-Z during the t_{OH} (Output Hold to High-Z) period.

The diagram illustrates the timing relationships for the 28C02 EPROM. The signals shown are Address, CS1, CS2, UB, LB, WE, Data in, and Data out. The timing parameters are defined as follows:

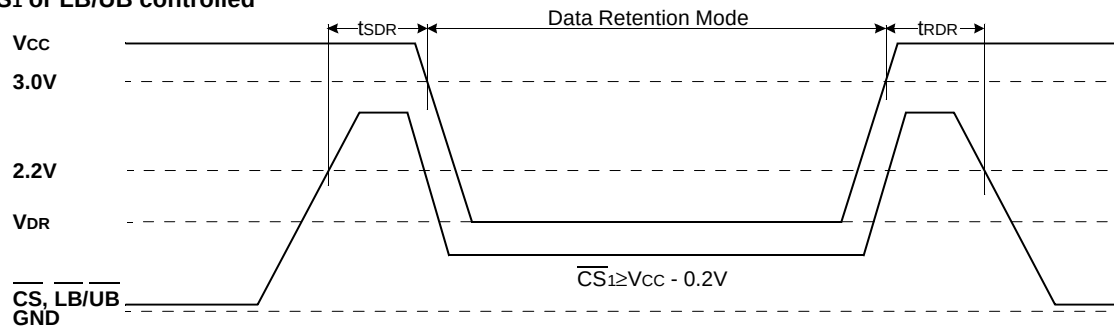
- Address:** The duration of the address pulse is t_{WC} .
- CS1:** The setup time before CS1 goes low is $t_{AS(3)}$. The pulse width of CS1 is $t_{CW(2)}$. The time from CS1 going high to the data bus becoming high-Z is $t_{WR(4)}$. The total access time from CS1 going low to data being valid is t_{AW} .
- CS2:** The pulse width of CS2 is t_{BW} .
- UB, LB:** The pulse width of the chip enable signals is $t_{WP(1)}$.
- WE:** The pulse width of the write enable signal is $t_{WP(1)}$.
- Data in:** The data is valid for a duration of t_{DW} after CS1 goes high and t_{DH} before CS1 goes high.
- Data out:** The data bus is in a High-Z state during the address pulse and after CS1 goes high.

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

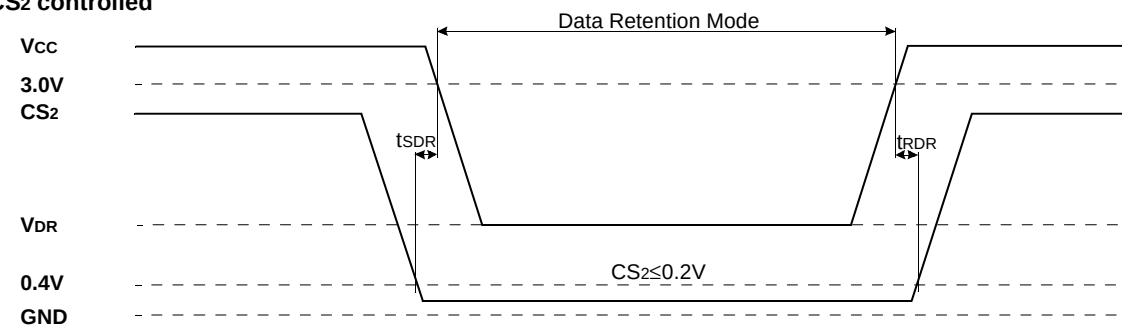
NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low $\overline{WE}$. A write begins when $\overline{CS1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

 $\overline{CS1}$ or $\overline{LB}/\overline{UB}$ controlled

CS2 controlled



PACKAGE DIMENSION

Unit: millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

