

Document Title

256Kx16 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	July 4, 1998	Preliminary
0.01	Errata correction	August 17, 1998	
1.0	Finalize - Specified CSP type. - Errata correction	November 16, 1998	Final

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256Kx16 bit Low Power and Low Voltage CMOS StaticRAM

FEATURES

- Process Technology: TFT
- Organization: 256K x16
- Power Supply Voltage
K6T4016U6C Family: 2.7~3.3V
- Low Data Retention Voltage: 2.0V(Min)
- Three State Outputs
- Dual CS and standby control by $\overline{UB}$, $\overline{LB}$
- Package Type: 48- μ BGA-6.10x8.90

GENERAL DESCRIPTION

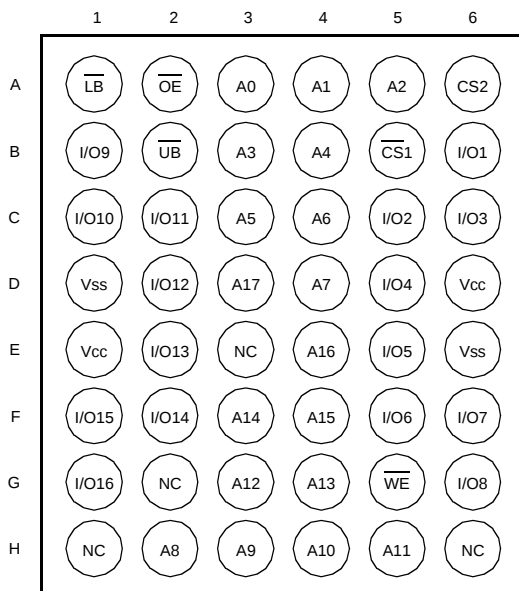
The K6T4016U6C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6T4016U6C-F	Industrial(-40~85°C)	2.7~3.3V	70 ¹ /85/100ns	20 μ A	45mA	48- μ BGA-6.10x8.90

1. The parameter is measured with 30pF test load.

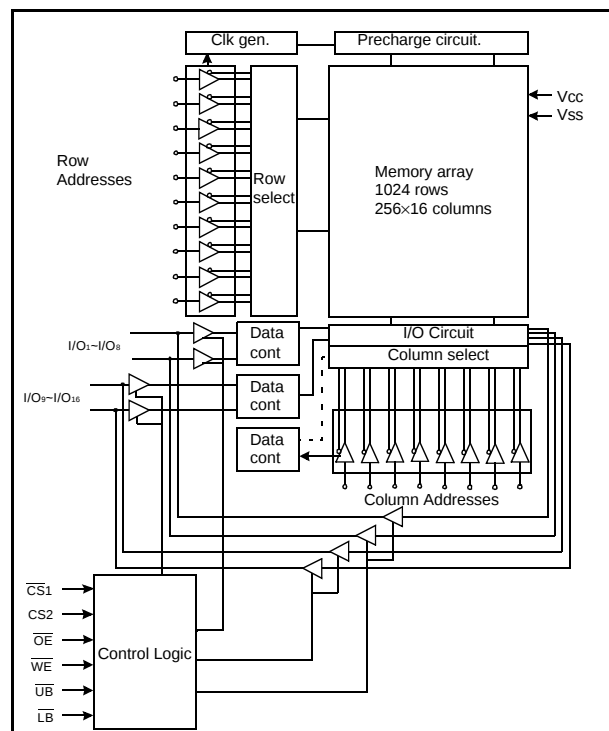
PIN DESCRIPTION



48-ball CSP - Top View (Ball Down)

Name	Function	Name	Function
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
A0~A17	Address Inputs	$\overline{LB}$	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6T4016U6C-ZF70	48-μBGA, 70ns, 3.0V, LL
K6T4016U6C-ZF85	48-μBGA, 85ns, 3.0V, LL
K6T4016U6C-ZF10	48-μBGA, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T4016U6C Family	2.7	3.0	3.3	V
Ground	V _{SS}	K6T4016U6C Family	0	0	0	V
Input high voltage	V _{IH}	K6T4016U6C Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	K6T4016U6C Family	-0.3 ³⁾	-	0.6	V

Note:

1. T_A=-40 to 85°C, otherwise specified2. Overshoot: V_{CC}+2.0V in case of pulse width ≤30ns.

3. Undershoot: -2.0V in case of pulse width ≤30ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	4	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS_1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	6	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	45	mA
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS_1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V($\overline{CS_1}$ controlled) or CS ₂ ≤0.2V(CS ₂ controlled), Other inputs=0~V _{CC}	-	-	20	μA

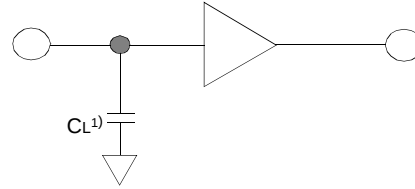
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load(see right): $C_L=100\text{pF}+1\text{TTL}$ $C_L=30\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=2.7\sim 3.3\text{V}$, Industrial product: $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	40	-	50	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to data output	t _{BA}	-	70	-	85	-	100	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ enable to low-Z output	t _{BLZ}	10	-	10	-	10	-	ns
	Output hold from address change	t _{OH}	10	-	10	-	15	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	25	0	30	ns
	$\overline{\text{OE}}$ disable to high-Z output	t _{OHZ}	0	25	0	25	0	30	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	25	0	25	0	30	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	60	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t _{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to end of write	t _{BW}	60	-	70	-	80	-	ns

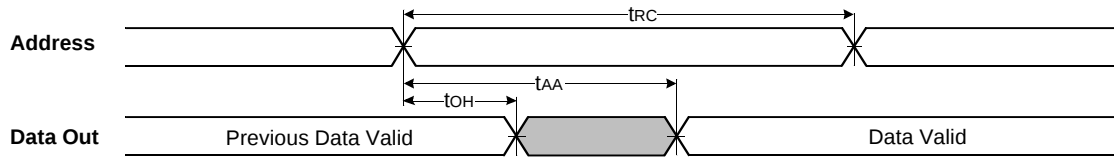
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	$\overline{CS}_1 \geq V_{CC}-0.2V^{1)}$	2.0	-	3.3	V
Data retention current	I_{DR}	$V_{CC}=3.0V$, $\overline{CS}_1 \geq V_{CC}-0.2V^{1)}$	-	0.5	20	μA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

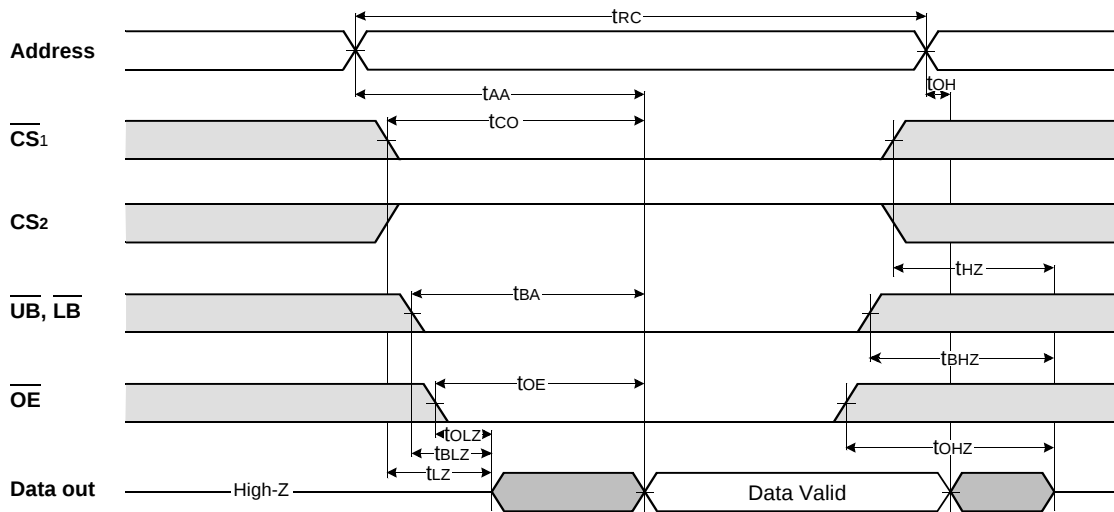
1. $\overline{CS}_1 \geq V_{CC}-0.2V$, $\overline{CS}_2 \geq V_{CC}-0.2V$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \geq V_{CC}-0.2V$ ($\overline{CS}_2$ controlled)

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{CS2}=\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)

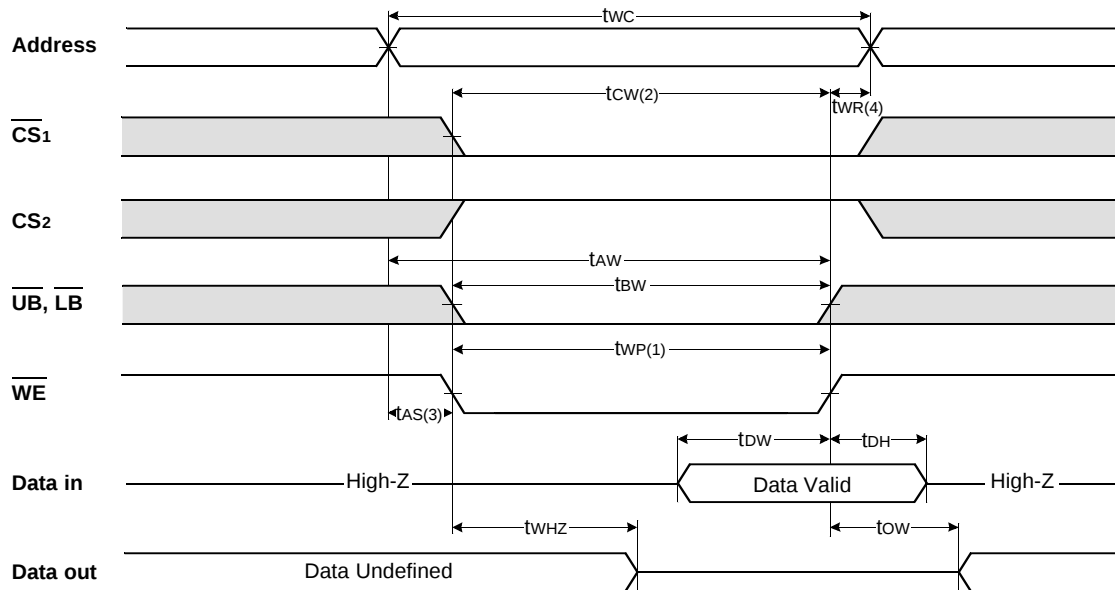
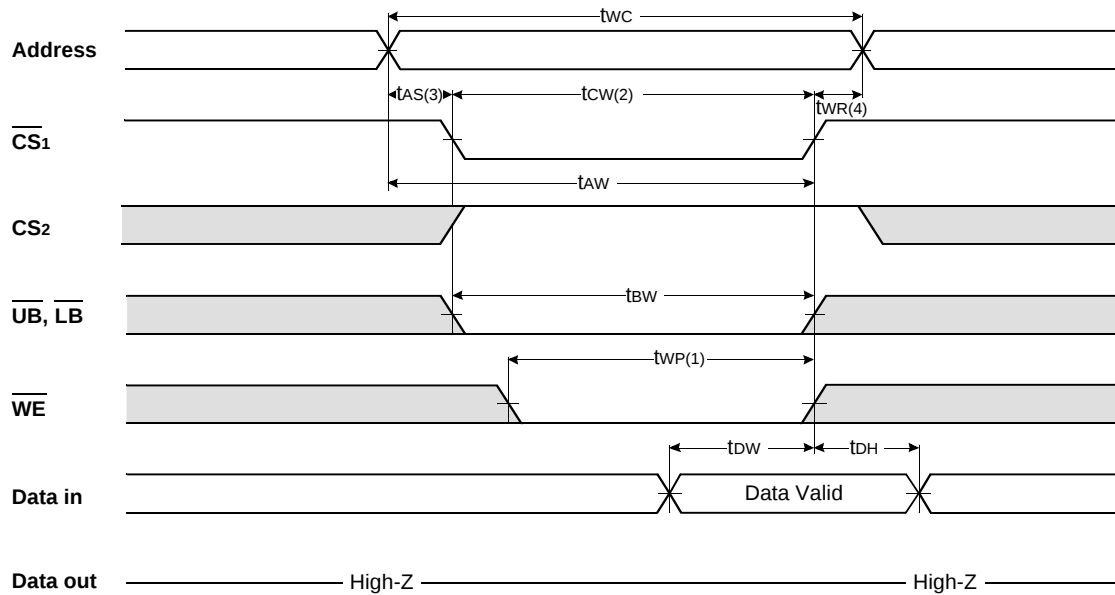


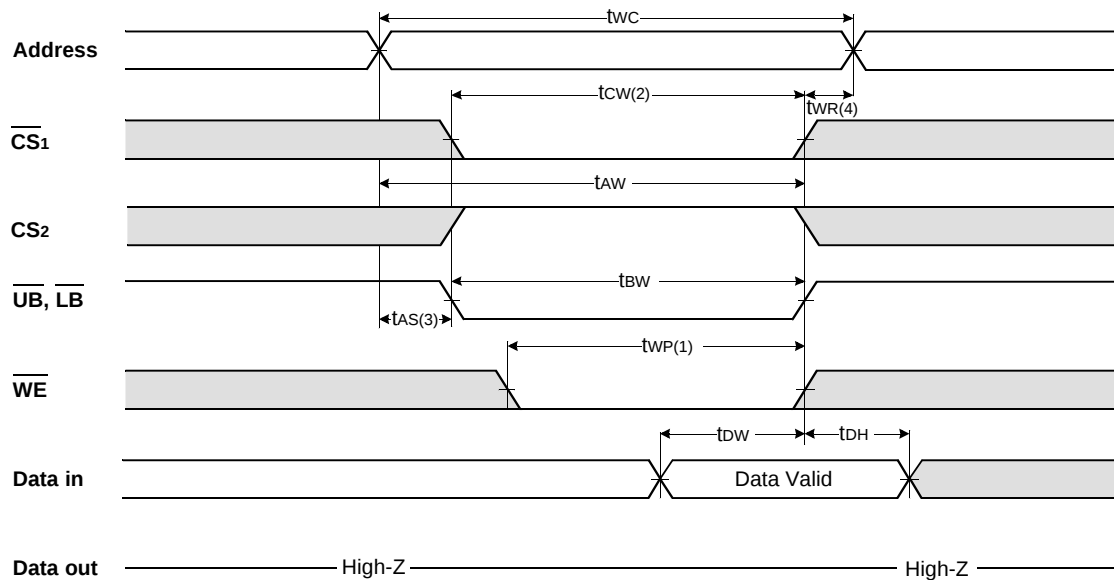
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

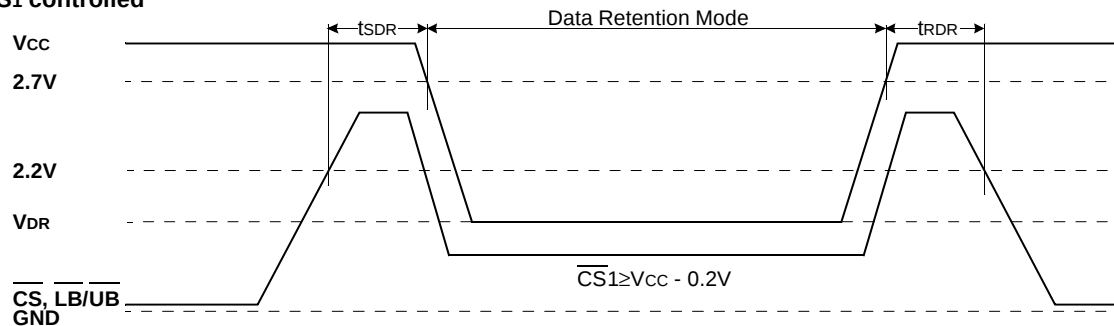
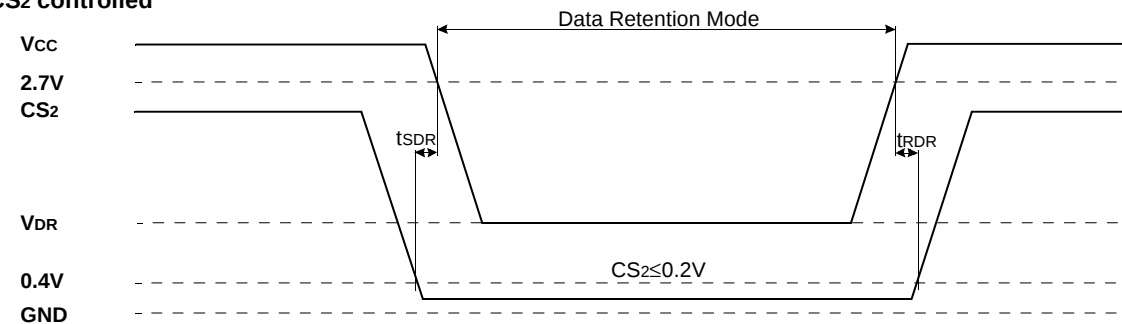
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{UB}}$, $\overline{\text{LB}}$ Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{\text{CS1}}$ and low $\overline{\text{WE}}$. A write begins when $\overline{\text{CS1}}$ goes low and $\overline{\text{WE}}$ goes low with asserting $\overline{\text{UB}}$ or $\overline{\text{LB}}$ for single byte operation or simultaneously asserting $\overline{\text{UB}}$ and $\overline{\text{LB}}$ for double byte operation. A write ends at the earliest transition when $\overline{\text{CS1}}$ goes high and $\overline{\text{WE}}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{\text{CS1}}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high.

DATA RETENTION WAVE FORM

 $\overline{\text{CS1}}$ controlled $\overline{\text{CS2}}$ controlled

PACKAGE DIMENSIONS

Units: millimeters

48 BALL MICRO BALL GRID ARRAY- 0.75mm ball pitch

