# 2M x 32 SDRAM

*512K x 32bit x 4 Banks*
*Synchronous DRAM*
*LVTTL(2.5V)*
*Extended Temperature*
*90-Ball FBGA*

Revision 1.8

April 2002

# Revision History

## Revision 1.8 (April 19, 2002) - *Final*
• Erased TSOP specification.

## Revision 1.7 (November 15, 2001) - *Final*
• Final specification for 2Mx32 SDRAM.

## Revision 1.6 (October 10, 2001) - *Preliminary*
• Changed VDD and VDDQ range from 2.3V~3.3V to 2.3V~2.7V.
• Deleted tCC 6ns part.
• Changed Vtt from 1.05V to 0.5 x VDDQ.
• Unification of tCH 3ns for -70 part and tCH 3ns for -80 part, tCH 3ns for -10 part.
• Unification of tCL 3ns for -70 part and tCL 3ns for -80 part, tCL 3ns for -10 part.
• Unification of tCL 1.75ns for -70 part and tCL 2ns for -80 part, tCL 2.5ns for -10 part.
• Changed tCDL form 2clk to 1clk and tRDL for CL1 from 1clk to 2clk.

## Revision 1.5 (August 7, 2001) - *Target*
• Addede CAS Latency 1

## Revision 1.4(July 13, 2001)
• Guaranteed 2.3V ~ 3.3V wide range $V_{DD}$.

## Revision 1.3 (April 6, 2001)
• Reduced ICC current value
-Changed ICC6 value from 450um to 350um
-Changed ICC2P from 3mA to 1.2mA and ICC2PS from 2mA to1.2mA
-Changed ICC3P from 20mA to 10mA and ICC3PS from 20mA to 10mA
-Changed ICC3N from 55mA to 45mA and ICC3NS from 40mA to 30mA
-Changed ICC4 of K4S643234E-70 from 155mA to 130mA
-Changed ICC5 of K4S643234E-70 from 160mA to 145mA

## Revision 1.2 (March 21, 2001)
• Specified the current value as super low power for K4S643234E-80/10
• Suppor ted 90Ball FBGA as well as 86-TSOP

## Revision 1.1 (March 06, 2000)
• Added K4S643234E-80/10 as a low curnent product.

## Revision 1.0 (January 12, 2000)
• Final spec

## Revision 0.0 (December 20, 2000) - *Preliminary Spec.*
• Initial draft

## *512K x 32Bit x 4 Banks Synchronous DRAM*

### FEATURES

- 2.5V power supply .
- LVCMOS compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (1 & 2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle).
- Extended temperature range : (-25°C to 85°C)

### GENERAL DESCRIPTION

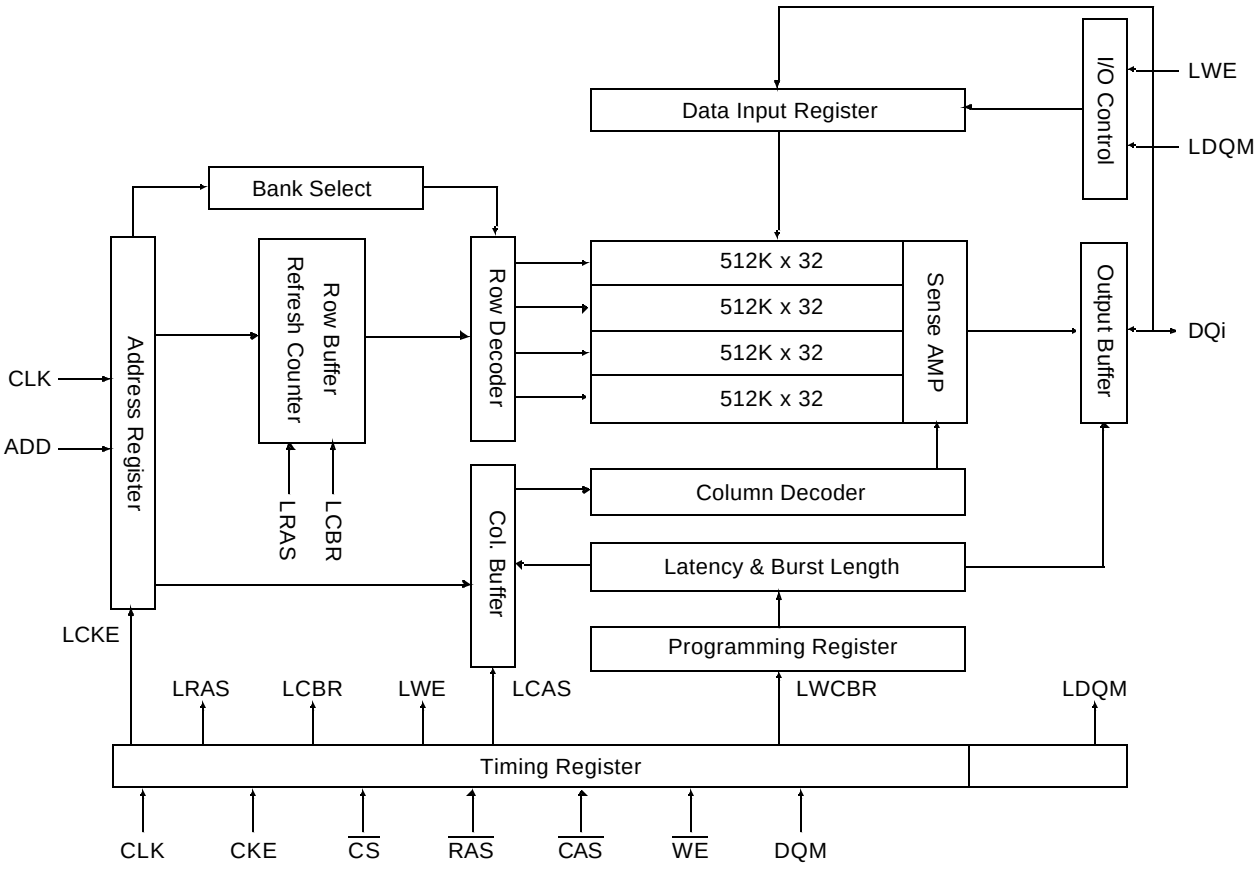
The K4S643234E is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### ORDERING INFORMATION

| Part NO. | Max Freq. | Interface | Package |
|---|---|---|---|
| K4S643234E-SE/N70 | 143MHz | LVCMOS | 90 FBGA |
| K4S643234E-SE/N80 | 125MHz | | |
| K4S643234E-SE/N10 | 100MHz | | |

- -SE/N : Extended temperature (-25°C to 85°C)

### FUNCTIONAL BLOCK DIAGRAM

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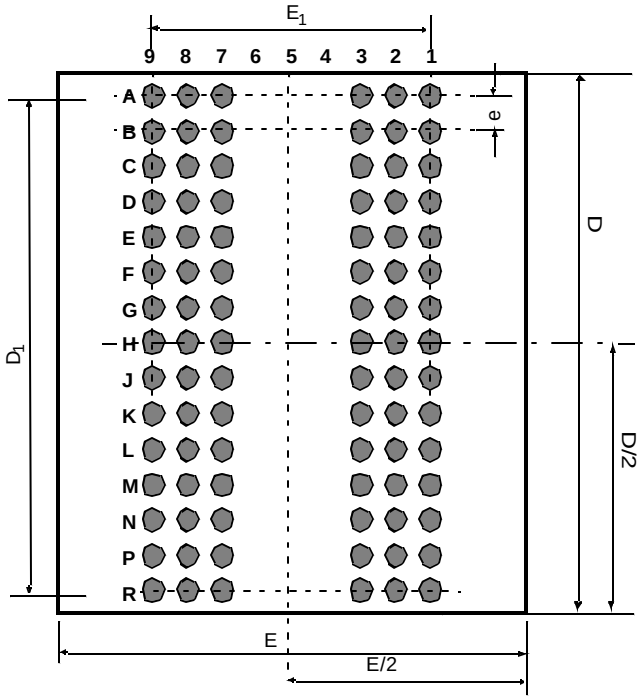
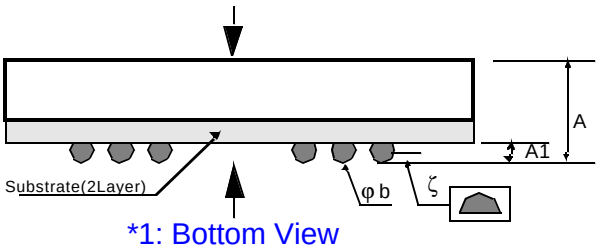
## 90-Ball FBGA Package Dimension and Pin Configuration

< Bottom View*1 >

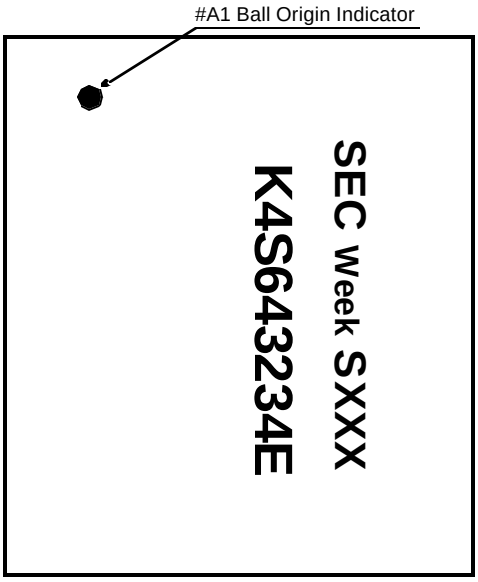



*2: Top View




*1: Bottom View

< Top View*2 >




< Top View*2 >

| 90Ball(6x15) CSP | | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 7 | 8 | 9 |
| A | DQ26 | DQ24 | VSS | VDD | DQ23 | DQ21 |
| B | DQ28 | VDDQ | VSSQ | VDDQ | VSSQ | DQ19 |
| C | VSSQ | DQ27 | DQ25 | DQ22 | DQ20 | VDDQ |
| D | VSSQ | DQ29 | DQ30 | DQ17 | DQ18 | VDDQ |
| E | VDDQ | DQ31 | NC | NC | DQ16 | VSSQ |
| F | VSS | DQM3 | A3 | A2 | DQM2 | VDD |
| G | A4 | A5 | A6 | A10 | A0 | A1 |
| H | A7 | A8 | NC | NC | BA1 | NC |
| J | CLK | CKE | A9 | BA0 | $\overline{CS}$ | $\overline{RAS}$ |
| K | DQM1 | NC | NC | $\overline{CAS}$ | $\overline{WE}$ | DQM0 |
| L | VDDQ | DQ8 | VSS | VDD | DQ7 | VSSQ |
| M | VSSQ | DQ10 | DQ9 | DQ6 | DQ5 | VDDQ |
| N | VSSQ | DQ12 | DQ14 | DQ1 | DQ3 | VDDQ |
| P | DQ11 | VDDQ | VSSQ | VDDQ | VSSQ | DQ4 |
| R | DQ13 | DQ15 | VSS | VDD | DQ0 | DQ2 |

| Pin Name | Pin Function |
|---|---|
| CLK | *System Clock* |
| $\overline{CS}$ | *Chip Select* |
| CKE | *Clock Enable* |
| $A_0$ ~ $A_{10}$ | *Address* |
| $BA_0$ ~ $BA_1$ | *Bank Select Address* |
| $\overline{RAS}$ | *Row Address Strobe* |
| $\overline{CAS}$ | *Column Address Strobe* |
| $\overline{WE}$ | *Write Enable* |
| $DQM_0$ ~ $DQM_3$ | *Data Input/Output Mask* |
| $DQ_{0 \sim 31}$ | *Data Input/Output* |
| VDD/VSS | *Power Supply/Ground* |
| VDDQ/VSSQ | *Data Output Power/Ground* |

[Unit:mm]

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | - | 1.40 | 1.45 |
| $A_1$ | 0.30 | 0.35 | 0.40 |
| E | - | 11.00 | - |
| $E_1$ | - | 6.40 | - |
| D | - | 13.00 | - |
| $D_1$ | - | 11.20 | - |
| e | - | 0.80 | - |
| φb | 0.40 | 0.45 | 0.50 |
| ζ | - | - | 0.10 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -0.5 ~ 3.6 | V |
| Voltage on $V_{DD}$ supply relative to Vss | $V_{DD}$, $V_{DDQ}$ | -0.5 ~ 3.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power dissipation | $P_D$ | 1 | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to $V_{SS}$ = 0V, $T_A$ = -25 to 85°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$, $V_{DDQ}$ | 2.3 | 2.5 | 2.7 | V | |
| Input logic high voltage | $V_{IH}$ | 0.8*$V_{DDQ}$ | 2.5 | $V_{DDQ}$+0.3 | V | 1 |
| Input logic low voltage | $V_{IL}$ | -0.3 | 0 | 0.7 | V | 2 |
| Output logic high voltage | $V_{OH}$ | 0.9*$V_{DDQ}$ | - | - | V | $I_{OH}$ = -1mA |
| Output logic low voltage | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 1mA |
| Input leakage current | $I_{LI}$ | -10 | - | 10 | uA | 3 |

**Notes :**
1. $V_{IH}$ (max) = 3.0V AC.The overshoot voltage duration is ≤ 3ns.
2. $V_{IL}$ (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ $V_{IN}$ ≤ $V_{DDQ}$,
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE ($V_{DD}$ = 2.5V, $T_A$ = 23°C, f = 1MHz, $V_{REF}$ = 1.4V ± 200mV)

| Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock | $C_{CLK}$ | - | 4 | pF |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM | $C_{IN}$ | - | 4.5 | pF |
| Address | $C_{ADD}$ | - | 4.5 | pF |
| $DQ_0$ ~ $DQ_{31}$ | $C_{OUT}$ | - | 6.5 | pF |

## DC CHARACTERISTICS

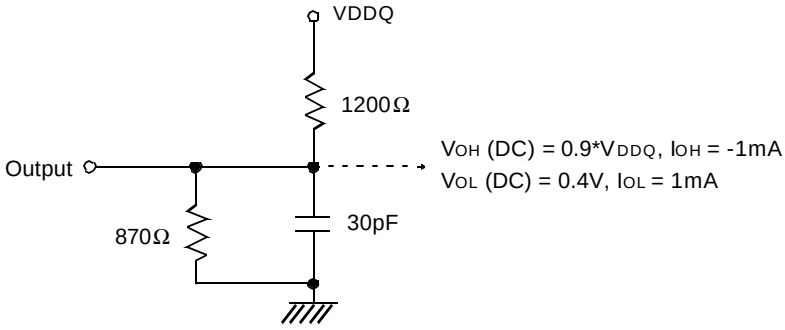
(Recommended operating condition unless otherwise noted, $T_A$ = -25 to +85°C)

| Parameter | Symbol | Test Condition | Speed | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | -70 | -80 | -10 | | |
| Operating Current (One Bank Active) | $I_{CC1}$ | Burst Length =1<br>$t_{RC} \geq t_{RC}$(min), $t_{CC} \geq t_{CC}$(min), Io = 0mA | 130 | 125 | 110 | mA | 2 |
| Precharge Standby Current in power-down mode | $I_{CC2}P$ | CKE ≤ $V_{IL}$(max), $t_{CC}$ = 15ns | 1.2 | | | mA | |
| | $I_{CC2}PS$ | CKE & CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | | | | | |
| Precharge Standby Current in non power-down mode | $I_{CC2}N$ | CKE ≥ $V_{IH(min)}$, $\overline{CS}$ ≥ $V_{IH(min)}$, $t_{CC}$ = 15ns<br>Input signals are changed one time during 30ns | 10 | | | mA | |
| | $I_{CC2}NS$ | CKE ≥ $V_{IH(min)}$, CLK ≤ $V_{IL(max)}$, tCC = ∞<br>Input signals are stable | 5 | | | | |
| Active Standby Current in power-down mode | $I_{CC3}P$ | CKE ≤ $V_{IL(max)}$, $t_{CC}$ = 15ns | 3.5 | | | mA | |
| | $I_{CC3}PS$ | CKE ≤ $V_{IL(max)}$, $t_{CC}$ = ∞ | 3 | | | | |
| Active Standby Current in non power-down mode (One Bank Active) | $I_{CC3}N$ | CKE ≥ $V_{IH(min)}$, $\overline{CS}$ ≥ $V_{IH(min)}$, $t_{CC}$ = 15ns<br>Input signals are changed one time during 30ns | 40 | | | mA | |
| | $I_{CC3}NS$ | CKE ≥ $V_{IH(min)}$, CLK ≤ $V_{IL(max)}$, $t_{CC}$ = ∞<br>Input signals are stable | 30 | | | | |
| Operating Current (Burst Mode) | $I_{CC4}$ | Io = 0 mA, Page Burst<br>All bank Activated, $t_{CCD}$ = $t_{CCD(min)}$ | 130 | 125 | 110 | mA | 2 |
| Refresh Current | $I_{CC5}$ | $t_{RC} \geq t_{RC(min)}$ | 145 | 135 | 125 | mA | 3 |
| Self Refresh Current | $I_{CC6}$ | CKE ≤ 0.2V | 350 | | | uA | |

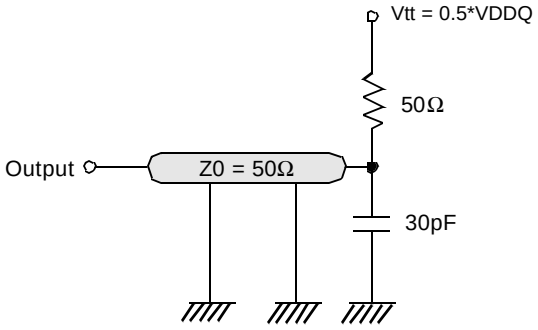
**Notes :** 1. Unless otherwise notes, Input level is CMOS(VIH/VIL=VDDQ/VSSQ)
2. Measured with outputs open.
3. Refresh period is 64ms.

## AC OPERATING TEST CONDITIONS ($V_{DD}$ = 2.5V ± 0.2V, $T_A$ = -25 to 85°C)

| Parameter | Value | Unit |
|---|---|---|
| AC input levels (Vih/Vil) | 0.9*$V_{DDQ}$/0.4 | V |
| Input timing measurement reference level | 0.5*$V_{DDQ}$ | V |
| Input rise and fall time | tr/tf = 1/1 | ns |
| Output timing measurement reference level | 0.5*$V_{DDQ}$ | V |
| Output load condition | See Fig. 2 | |




(Fig. 1) DC output load circuit




(Fig. 2) AC output load circuit

## OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter | | Symbol | Version | | | | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -70 | | | -80 | | | -10 | | | | |
| CAS Latency | | CL | 3 | 2 | 1 | 3 | 2 | 1 | 3 | 2 | 1 | CLK | |
| CLK cycle time | | $t_{CC(min)}$ | 7 | 10 | 20 | 8 | 12 | 20 | 10 | 12 | 20 | ns | |
| Row active to row active delay | | $t_{RRD(min)}$ | 2 | 2 | 1 | 2 | 2 | 1 | 2 | 2 | 1 | CLK | 1 |
| $\overline{RAS}$ to $\overline{CAS}$ delay | | $t_{RCD(min)}$ | 3 | 2 | 1 | 3 | 2 | 1 | 2 | 2 | 1 | CLK | 1 |
| Row precharge time | | $t_{RP(min)}$ | 3 | 2 | 1 | 3 | 2 | 1 | 2 | 2 | 1 | CLK | 1 |
| Row active time | | $t_{RAS(min)}$ | 7 | 5 | 2 | 6 | 4 | 2 | 5 | 4 | 2 | CLK | 1 |
| | | $t_{RAS(max)}$ | 100 | | | | | | | | | us | |
| Row cycle time | | $t_{RC(min)}$ | 10 | 7 | 3 | 10 | 7 | 3 | 10 | 9 | 3 | CLK | 1 |
| Last data in to row precharge | | $t_{RDL(min)}$ | 2 | | | | | | | | | CLK | 2 |
| Last data in to new col.address delay | | $t_{CDL(min)}$ | 1 | | | | | | | | | CLK | 2 |
| Last data in to burst stop | | $t_{BDL(min)}$ | 1 | | | | | | | | | CLK | 2 |
| Col. address to col. address delay | | $t_{CCD(min)}$ | 1 | | | | | | | | | CLK | 3 |
| Mode Register Set cycle time | | $t_{MRS(min)}$ | 2 | | | | | | | | | CLK | |
| Number of valid output data | CAS Latency=3 | | 2 | | | | | | | | | ea | 4 |
| | CAS Latency=2 | | 1 | | | | | | | | | | |
| | CAS Latency=1 | | 0 | | | | | | | | | | |

**Note :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer. Refer to the following ns-unit based AC table.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

## AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -70 | | -80 | | -10 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| CLK cycle time | CAS Latency=3 | $t_{CC}$ | 7 | 1000 | 8 | 1000 | 10 | 1000 | ns | 1 |
| | CAS Latency=2 | | 10 | | 12 | | 12 | | | |
| | CAS Latency=1 | | 20 | | 20 | | 20 | | | |
| CLK to valid output delay | CAS Latency=3 | $t_{SAC}$ | - | 5.5 | - | 6 | - | 6 | ns | 1, 2 |
| | CAS Latency=2 | | - | 6 | - | 8 | - | 8 | | |
| | CAS Latency=1 | | - | 18 | - | 18 | - | 18 | | |
| Output data hold time | CAS Latency=2,3 | $t_{OH}$ | 2 | - | 2 | - | 2 | - | ns | 2 |
| | CAS Latency=1 | | 3 | - | 3 | - | 3 | - | | |
| CLK high pulse width | | $t_{CH}$ | 3 | - | 3 | - | 3 | - | ns | 3 |
| CLK low | | $t_{CL}$ | 3 | - | 3 | - | 3 | - | ns | 3 |
| Input setup time | | $t_{SS}$ | 1.75 | - | 2 | - | 2.5 | - | ns | 3 |
| Input hold time | | $t_{SH}$ | 1 | - | 1 | - | 1 | - | ns | 3 |
| CLK to output in Low-Z | | $t_{SLZ}$ | 1 | - | 1 | - | 1 | - | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | $t_{SHZ}$ | - | 5.5 | - | 6 | - | 6 | ns | - |
| | CAS latency=2 | | - | 6 | - | 8 | - | 8 | | |
| | CAS Latency=1 | | - | 18 | - | 18 | - | 18 | | |

**Note :** 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

## SIMPLIFIED TRUTH TABLE

| Command | | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | $BA_{0,1}$ | $A_{10}$/AP | $A_9 \sim A_0$ | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Mode register set | | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self refresh | Entry | | L | | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank active & row addr. | | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column address ($A_0 \sim A_7$) | 4 |
| | Auto precharge enable | | | | | | | | | | H | | 4,5 |
| Write & column address | Auto precharge disable | | H | X | L | H | L | L | X | V | L | Column address ($A_0 \sim A_7$) | 4 |
| | Auto precharge enable | | | | | | | | | | H | | 4,5 |
| Burst Stop | | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank selection | | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | | X | H | | |
| Clock suspend or active power down | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | | Exit | L | H | X | X | X | X | X | | | | |
| Precharge power down mode | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | | Exit | L | H | H | X | X | X | X | | | | |
| | | | | | L | V | V | V | | | | | |
| DQM | | | H | X | | | | | V | X | | | 7 |
| No operation command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :** 1. OP Code : Operand code
$A_0 \sim A_{10}$ & $BA_0 \sim BA_1$ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$ : Bank select addresses.
If both $BA_0$ and $BA_1$ are "Low" at read, write, row active and precharge, bank A is selected.
If $BA_0$ is "Low" and $BA_1$ is "High" at read, write, row active and precharge, bank B is selected.
If $BA_0$ is "High" and $BA_1$ is "Low" at read, write, row active and precharge, bank C is selected.
If both $BA_0$ and $BA_1$ are "High" at read, write, row active and precharge, bank D is selected.
If $A_{10}$/AP is "High" at row precharge, $BA_0$ and $BA_1$ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at $t_{RP}$ after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

## MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

| Address | BA0 ~ BA1 | A10/AP | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | RFU | RFU | W.B.L | TM | | CAS Latency | | | BT | Burst Length | | |

| Test Mode | | | CAS Latency | | | | Burst Type | | Burst Length | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A8 | A7 | Type | A6 | A5 | A4 | Latency | A3 | Type | A2 | A1 | A0 | BT = 0 | BT = 1 |
| 0 | 0 | Mode Register Set | 0 | 0 | 0 | Reserved | 0 | Sequential | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | Reserved | 0 | 0 | 1 | 1 | 1 | Interleave | 0 | 0 | 1 | 2 | 2 |
| 1 | 0 | Reserved | 0 | 1 | 0 | 2 | | | 0 | 1 | 0 | 4 | 4 |
| 1 | 1 | Reserved | 0 | 1 | 1 | 3 | | | 0 | 1 | 1 | 8 | 8 |
| Write Burst Length | | | 1 | 0 | 0 | Reserved | | | 1 | 0 | 0 | Reserved | Reserved |
| A9 | Length | | 1 | 0 | 1 | Reserved | | | 1 | 0 | 1 | Reserved | Reserved |
| 0 | Burst | | 1 | 1 | 0 | Reserved | | | 1 | 1 | 0 | Reserved | Reserved |
| 1 | Single Bit | | 1 | 1 | 1 | Reserved | | | 1 | 1 | 1 | Full Page | Reserved |

Full Page Length : x32 (256)

## POWER UP SEQUENCE

**SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.**

1. Apply power and start clock. Must maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Power is applied to VDD and VDDQ (simultaneously).
3. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
4. Issue precharge commands for all banks of the devices.
5. Issue 2 or more auto-refresh commands.
6. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

**Note** : 1. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

## BURST SEQUENCE (BURST LENGTH = 4)

| Initial Address | | Sequential | | | | Interleave | | | |
|---|---|---|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | | | | | | | | |
| 0 | 0 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 0 | 1 | 1 | 2 | 3 | 0 | 1 | 0 | 3 | 2 |
| 1 | 0 | 2 | 3 | 0 | 1 | 2 | 3 | 0 | 1 |
| 1 | 1 | 3 | 0 | 1 | 2 | 3 | 2 | 1 | 0 |

## BURST SEQUENCE (BURST LENGTH = 8)

| Initial Address | | | Sequential | | | | | | | | Interleave | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |