Document Title

Multi-Chip Package MEMORY
64M Bit (4Mx16) Four Bank NOR Flash Memory *2 / 32M Bit (2Mx16) UtRAM / 8M Bit (512Kx16) SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	January 8, 2002	Preliminary
0.1	Revise - Added NOR Flash Boot Block Architecture 03: Flash 1 - Bottom Boot Block Flash 2 - Top Boot Block 04: Flash 1 - Top Boot Block Flash 2 - Bottom Boot Block	February 15, 2002	Preliminary

Multi-Chip Package MEMORY

64M Bit (4Mx16) Four Bank NOR Flash Memory *2 / 32M Bit (2Mx16) UtRAM / 8M Bit (512Kx16) SRAM

FEATURES

- Power Supply voltage
  - Flash : 2.7V to 3.3V
  - UtRAM, SRAM : 2.7V to 3.1V
- Organization
  - Flash : 4,194,304 x 16 bit *2
  - UtRAM : 2,097,152 x 16 bit
  - SRAM : 524,288 x 16 bit
- Access Time (@2.7V)
  - Flash : 85 ns, UtRAM : 85 ns, SRAM : 55ns
- Power Consumption (typical value)
  - Flash Read Current : 20 mA (@5MHz)
    Sequential Page Read Current : 5 mA (@5MHz)
    Program/Erase Current : 35 mA (Max.)
    Standby mode/Deep Power mode : 0.1 µA
  - UtRAM Operating Current : 30 mA
    Standby Current : 80 µA
    Deep Power Down : 5 µA
  - SRAM Standby Current : 0.5 µA
- SRAM Data Retention : 1.5 V (min.)
- Secode(Security Code) Block : Extra 32KW Block (Flash)
- Block Group Protection / Unprotection (Flash)
- 128 words Page Program (Flash)
- Flash Bank Size : 4Mb / 4Mb / 28Mb / 28Mb
- Flash Endurance : 100,000 Program/Erase Cycles
- Ambient Temperature : -25°C ~ 85°C
- Endurance : 100,000 Program/Erase Cycles
- Package : 80-ball TBGA Type - 11.0 x 10.0 mm, 0.8 mm pitch

GENERAL DESCRIPTION

The KBA0101A0M/KBA0201A0M featuring single 3.0V power supply is a Multi Chip Package Memory which combines two 64Mbit Four Bank Flash and 32Mbit UtRAM and 8Mbit SRAM.

The 64Mbit Flash memory is organized as 4M x16 bit and 32Mbit UtRAM is organized as 2M x16 bit and 8Mbit SRAM is organized as 512K x 16 bit.

The 64Mbit Flash memory is the high performance non-volatile memory fabricated by CMOS technology for peripheral circuit and DINOR IV(Diveded bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can be programmed or erased, when F-WP is low.

Using Software Lock Release function, program erase operation can be executed.

The 32Mbit UtRAM is fabricated by SAMSUNGś advanced CMOS technology using one transistor memory cell.

The device also supports deep power down mode for low standby current.

The 8Mbit SRAM is fabricated by SAMSUNG′s advanced full CMOS process technology. The device also supports low data retention voltage for battery back-up operation with low data retention current.

The KBA0101A0M/KBA0201A0M is suitable for use in program and data memory of mobile communication system to reduce mount area. This device is available in 80-ball TBGA Type package.

BALL CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	A6	F-RY/$\overline{BY}$	$\overline{UBs}$	NC	Vccs	F-$\overline{RP}$	NC	A12	DNU	DNU
B			A5	A18	A21	NC	Vccu	$\overline{WE}$	A9	A13		
C			A4	A17	$\overline{LBs}$	NC	Vss	A20	A10	A14		
D			A3	NC	A7	$\overline{LBu}$	$\overline{UBu}$	A19	A11	A15		
E			A1	A2	NC	F-$\overline{WP}$	$\overline{ZZ}$	CS2s	A8	NC		
F			A0	$\overline{CS1s}$	$\overline{CSu}$	NC	NC	F-$\overline{CE2}$	F-$\overline{CE1}$	A16		
G			$\overline{OE}$	DQ2	DQ11	Vccqu	Vss	DQ12	DQ5	DQ14		
H			DQ8	DQ9	DQ3	NC	Vccu	NC	DQ13	DQ7		
J	DNU	DNU	DQ0	DQ1	DQ10	F-Vcc	Vccs	DQ4	DQ6	DQ15	DNU	DNU

80 Ball TBGA , 0.8mm Pitch

Top View (Ball Down)

BALL DESCRIPTION

Ball Name	Description
A_0~A_{18}	Address Input (Flash Memory, UtRAM, SRAM)
A_{19}~A_{20}	Address Input (Flash Memory, UtRAM)
A_{21}	Address Input (Flash Memory)
DQ_0 to DQ_{15}	Data Input/Output Balls (Common)
F-$\overline{RP}$	Hardware Reset (Flash Memory)
F-$\overline{WP}$	Write Protection (Flash Memory)
F-Vcc	Power Supply (Flash Memory)
Vccs	Power Supply (SRAM)
Vccu	Power Supply (UtRAM)
Vccqu[1)]	Data Out Power (UtRAM)
Vss	Ground (Common)
$\overline{UBu}$	Upper Byte Enable (UtRAM)
$\overline{LBu}$	Lower Byte Enable (UtRAM)
$\overline{UBs}$	Upper Byte Enable (SRAM)
$\overline{LBs}$	Lower Byte Enable (SRAM)
F-RY/$\overline{BY}$	Ready/Busy (Flash Memory)
$\overline{ZZ}$	Deep Power Down (UtRAM)
F-$\overline{CE1}$	Chip Enable1 (Flash Memory)
F-$\overline{CE2}$	Chip Enable2 (Flash Memory)
$\overline{CS1s}$	Chip Select1 (SRAM)
CS2s	Chip Select2 (SRAM)
$\overline{CSu}$	Chip Enable (UtRAM)
$\overline{WE}$	Write Enable (Common)
$\overline{OE}$	Output Enable (Common)
NC	No Connection
DNU	Do Not Use

1) Vccqu=Vccu in this product.

ORDERING INFORMATION

K B A 01 0 1 A 0 M - T 401

Samsung
MCP(4 Stack) Memory

Device Type
Mitsubishi NOR Flash
+Mitsubishi NOR Flash
+UtRAM +SRAM

NOR Flash Density (Organization) (BankSize) , Block Architecture
01 : 64Mbit + 64Mbit (x16 Selectable)
(4Mb, 4Mb, 28Mb,28Mb)
Flash 1: Bottom Boot Block
Flash 2: Bottom Boot Block
02 : 64Mbit + 64Mbit (x16 Selectable)
(4Mb, 4Mb, 28Mb,28Mb)
Flash 1: Top Boot Block
Flash 2: Top Boot Block
03 : 64Mbit + 64Mbit (x16 Selectable)
(4Mb, 4Mb, 28Mb,28Mb)
Flash 1: Bottom Boot Block
Flash 2: Top Boot Block
04 : 64Mbit + 64Mbit (x16 Selectable)
(4Mb, 4Mb, 28Mb,28Mb)
Flash 1: Top Boot Block
Flash 2: Bottom Boot Block

NAND Density , Organization
0 = NONE

UtRAM Density , Organization
32Mbit , x16 Selectable

SRAM Density , Organization
8Mbit , x16 Selectable

SDRAM Density , Organization
0 = NONE

Version
M = 1st Generation

Package
T = 80 TBGA

Access Time
Mitsubishi NOR Flash: 85ns
Mitsubishi NOR Flash: 85ns
UtRAM: 85ns
SRAM: 55ns

FUNCTIONAL BLOCK DIAGRAM

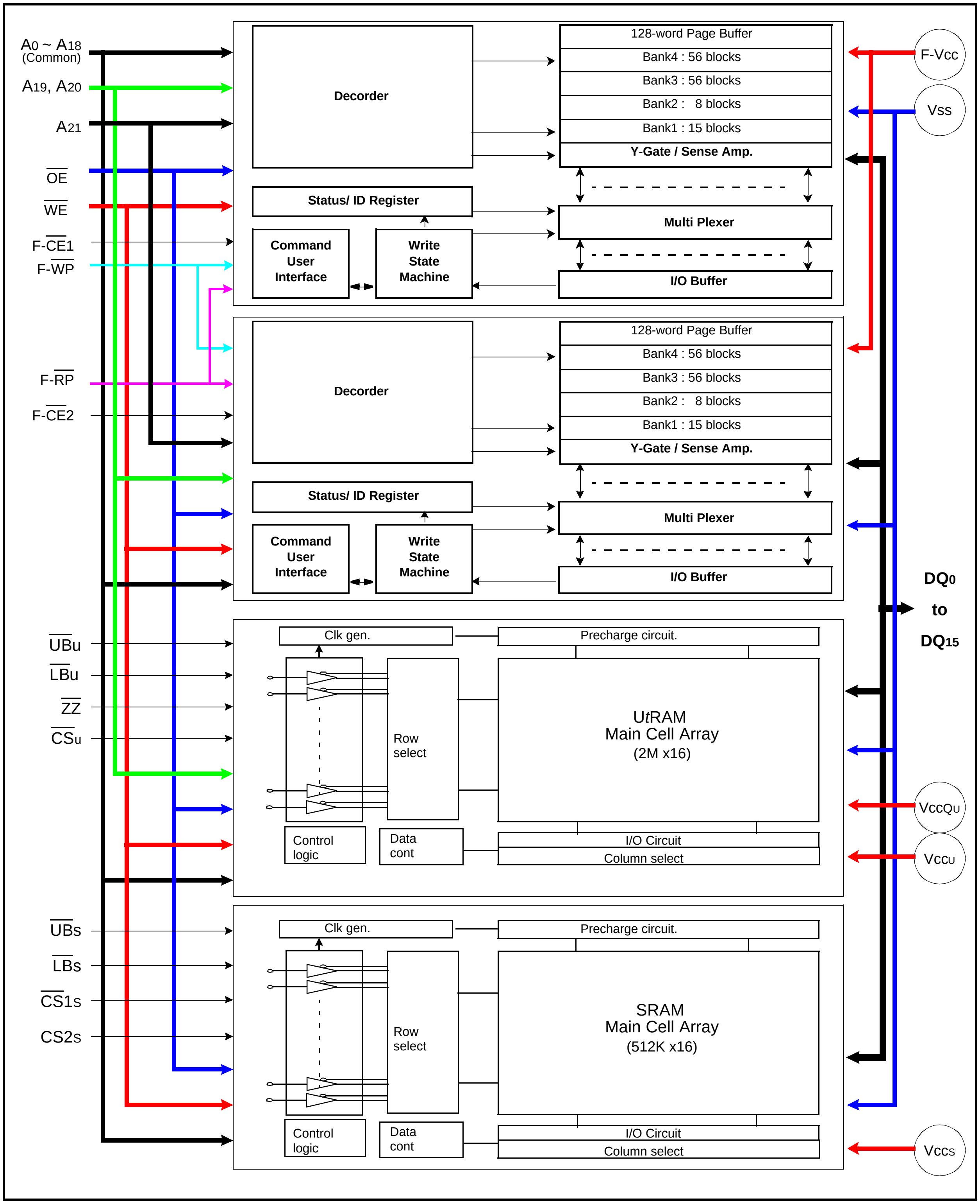


Table 1. Flash Memory Top Boot Block Address (KBA0201A0)

KBA0201A0	Block	Block Size	Address Range Word Mode (x16)
Bank4	BA134	4 Kwords	3FF000H-3FFFFFH
	BA133	4 Kwords	3FE000H-3FEFFFH
	BA132	4 Kwords	3FD000H-3FDFFFH
	BA131	4 Kwords	3FC000H-3FCFFFH
	BA130	4 Kwords	3FB000H-3FBFFFH
	BA129	4 Kwords	3FA000H-3FAFFFH
	BA128	4 Kwords	3F9000H-3F9FFFH
	BA127	4 Kwords	3F8000H-3F8FFFH
	BA126	32 Kwords	3F0000H-3F7FFFH
	BA125	32 Kwords	3E8000H-3EFFFFH
	BA124	32 Kwords	3E0000H-3E7FFFH
	BA123	32 Kwords	3D8000H-3DFFFFH
	BA122	32 Kwords	3D0000H-3D7FFFH
	BA121	32 Kwords	3C8000H-3CFFFFH
	BA120	32 Kwords	3C0000H-3C7FFFH
Bank3	BA119	32 Kwords	3B8000H-3BFFFFH
	BA118	32 Kwords	3B0000H-3B7FFFH
	BA117	32 Kwords	3A8000H-3AFFFFH
	BA116	32 Kwords	3A0000H-3A7FFFH
	BA115	32 Kwords	398000H-39FFFFH
	BA114	32 Kwords	390000H-397FFFH
	BA113	32 Kwords	388000H-38FFFFH
	BA112	32 Kwords	380000H-387FFFH
Bank2	BA111	32 Kwords	378000H-37FFFFH
	BA110	32 Kwords	370000H-377FFFH
	BA109	32 Kwords	368000H-36FFFFH
	BA108	32 Kwords	360000H-367FFFH
	BA107	32 Kwords	358000H-35FFFFH
	BA106	32 Kwords	350000H-357FFFH
	BA105	32 Kwords	348000H-34FFFFH
	BA104	32 Kwords	340000H-347FFFH
	BA103	32 Kwords	338000H-33FFFFH
	BA102	32 Kwords	330000H-337FFFH
	BA101	32 Kwords	328000H-32FFFFH
	BA100	32 Kwords	320000H-327FFFH
	BA99	32 Kwords	318000H-31FFFFH
	BA98	32 Kwords	310000H-317FFFH
	BA97	32 Kwords	208000H-20FFFFH
	BA96	32 Kwords	300000H-307FFFH
	BA95	32 Kwords	2F8000H-2FFFFFH
	BA94	32 Kwords	2F0000H-2F7FFFH
	BA93	32 Kwords	2E8000H-2EFFFFH
	BA92	32 Kwords	2E0000H-2E7FFFH
	BA91	32 Kwords	2D8000H-2DFFFFH
	BA90	32 Kwords	2D0000H-2D7FFFH

Table 1. Flash Memory Top Boot Block Address (KBA0201A0)

KBA0201A0	Block	Block Size	Address Range
			Word Mode (x16)
Bank2	BA89	32 Kwords	2C8000H-2CFFFFH
	BA88	32 Kwords	2C0000H-2C7FFFH
	BA87	32 Kwords	2B8000H-2BFFFFH
	BA86	32 Kwords	2B0000H-2B7FFFH
	BA85	32 Kwords	2A8000H-2AFFFFH
	BA84	32 Kwords	2A0000H-2A7FFFH
	BA83	32 Kwords	298000H-29FFFFH
	BA82	32 Kwords	290000H-297FFFH
	BA81	32 Kwords	288000H-28FFFFH
	BA80	32 Kwords	280000H-287FFFH
	BA79	32 Kwords	278000H-27FFFFH
	BA78	32 Kwords	270000H-277FFFH
	BA77	32 Kwords	268000H-26FFFFH
	BA76	32 Kwords	260000H-267FFFH
	BA75	32 Kwords	258000H-25FFFFH
	BA74	32 Kwords	250000H-257FFFH
	BA73	32 Kwords	248000H-24FFFFH
	BA72	32 Kwords	240000H-247FFFH
	BA71	32 Kwords	238000H-23FFFFH
	BA70	32 Kwords	230000H-237FFFH
	BA69	32 Kwords	228000H-22FFFFH
	BA68	32 Kwords	220000H-227FFFH
	BA67	32 Kwords	218000H-21FFFFH
	BA66	32 Kwords	210000H-217FFFH
	BA65	32 Kwords	208000H-20FFFFH
	BA64	32 Kwords	200000H-207FFFH
	BA63	32 Kwords	1F8000H-1FFFFFH
	BA62	32 Kwords	1F0000H-1F7FFFH
	BA61	32 Kwords	1E8000H-1EFFFFH
	BA60	32 Kwords	1E0000H-1E7FFFH
	BA59	32 Kwords	1D8000H-1DFFFFH
	BA58	32 Kwords	1D0000H-1D7FFFH
	BA57	32 Kwords	1C8000H-1CFFFFH
	BA56	32 Kwords	1C0000H-1C7FFFH
Bank1	BA55	32 Kwords	1B8000H-1BFFFFH
	BA54	32 Kwords	1B0000H-1B7FFFH
	BA53	32 Kwords	1A8000H-1AFFFFH
	BA52	32 Kwords	1A0000H-1A7FFFH
	BA51	32 Kwords	198000H-19FFFFH
	BA50	32 Kwords	190000H-197FFFH
	BA49	32 Kwords	188000H-18FFFFH
	BA48	32 Kwords	180000H-187FFFH
	BA47	32 Kwords	178000H-17FFFFH
	BA46	32 Kwords	170000H-177FFFH
	BA45	32 Kwords	168000H-16FFFFH

Table 1. Flash Memory Top Boot Block Address (KBA0201A0)

KBA0201A0	Block	Block Size	Address Range
			Word Mode (x16)
Bank1	BA44	32 Kwords	160000H-167FFFH
	BA43	32 Kwords	158000H-15FFFFH
	BA42	32 Kwords	150000H-157FFFH
	BA41	32 Kwords	148000H-14FFFFH
	BA40	32 Kwords	140000H-147FFFH
	BA39	32 Kwords	138000H-13FFFFH
	BA38	32 Kwords	130000H-137FFFH
	BA37	32 Kwords	128000H-12FFFFH
	BA36	32 Kwords	120000H-127FFFH
	BA35	32 Kwords	118000H-11FFFFH
	BA34	32 Kwords	110000H-117FFFH
	BA33	32 Kwords	108000H-10FFFFH
	BA32	32 Kwords	100000H-107FFFH
	BA31	32 Kwords	F8000H-FFFFFH
	BA30	32 Kwords	F0000H-F7FFFH
	BA29	32 Kwords	E8000H-EFFFFH
	BA28	32 Kwords	E0000H-E7FFFH
	BA27	32 Kwords	D8000H-DFFFFH
	BA26	32 Kwords	D0000H-D7FFFH
	BA25	32 Kwords	C8000H-CFFFFH
	BA24	32 Kwords	C0000H-C7FFFH
	BA23	32 Kwords	B8000H-BFFFFH
	BA22	32 Kwords	B0000H-B7FFFH
	BA21	32 Kwords	A8000H-AFFFFH
	BA20	32 Kwords	A0000H-A7FFFH
	BA19	32 Kwords	98000H-9FFFFH
	BA18	32 Kwords	90000H-97FFFH
	BA17	32 Kwords	88000H-8FFFFH
	BA16	32 Kwords	80000H-87FFFH
	BA15	32 Kwords	78000H-7FFFFH
	BA14	32 Kwords	70000H-77FFFH
	BA13	32 Kwords	68000H-6FFFFH
	BA12	32 Kwords	60000H-67FFFH
	BA11	32 Kwords	58000H-5FFFFH
	BA10	32 Kwords	50000H-57FFFH
	BA9	32 Kwords	48000H-4FFFFH
	BA8	32 Kwords	40000H-47FFFH
	BA7	32 Kwords	38000H-3FFFFH
	BA6	32 Kwords	30000H-37FFFH
	BA5	32 Kwords	28000H-2FFFFH
	BA4	32 Kwords	20000H-27FFFH
	BA3	32 Kwords	18000H-1FFFFH
	BA2	32 Kwords	10000H-17FFFH
	BA1	32 Kwords	08000H-0FFFFH
	BA0	32 Kwords	00000H-07FFFH

Table 2. Flash Memory Bottom Boot Block Address (KBA0101A0)

KBA0101A0	Block	Block Size	Address Range
			Word Mode (x16)
Bank4	BA134	32 Kwords	3F8000H-3FFFFFH
	BA133	32 Kwords	3F0000H-3F7FFFH
	BA132	32 Kwords	3E8000H-3EFFFFH
	BA131	32 Kwords	3E0000H-3E7FFFH
	BA130	32 Kwords	3D8000H-3DFFFFH
	BA129	32 Kwords	3D0000H-3D7FFFH
	BA128	32 Kwords	3C8000H-3CFFFFH
	BA127	32 Kwords	3C0000H-3C7FFFH
	BA126	32 Kwords	3B8000H-3BFFFFH
	BA125	32 Kwords	3B0000H-3B7FFFH
	BA124	32 Kwords	3A8000H-3AFFFFH
	BA123	32 Kwords	3A0000H-3A7FFFH
	BA122	32 Kwords	398000H-39FFFFH
	BA121	32 Kwords	390000H-397FFFH
	BA120	32 Kwords	388000H-38FFFFH
	BA119	32 Kwords	380000H-387FFFH
	BA118	32 Kwords	378000H-37FFFFH
	BA117	32 Kwords	370000H-377FFFH
	BA116	32 Kwords	368000H-36FFFFH
	BA115	32 Kwords	360000H-367FFFH
	BA114	32 Kwords	358000H-35FFFFH
	BA113	32 Kwords	350000H-357FFFH
	BA112	32 Kwords	348000H-34FFFFH
	BA111	32 Kwords	340000H-347FFFH
	BA110	32 Kwords	338000H-33FFFFH
	BA109	32 Kwords	330000H-337FFFH
	BA108	32 Kwords	328000H-32FFFFH
	BA107	32 Kwords	320000H-327FFFH
	BA106	32 Kwords	318000H-31FFFFH
	BA105	32 Kwords	310000H-317FFFH
	BA104	32 Kwords	208000H-20FFFFH
	BA103	32 Kwords	300000H-307FFFH
	BA102	32 Kwords	2F8000H-2FFFFFH
	BA101	32 Kwords	2F0000H-2F7FFFH
	BA100	32 Kwords	2E8000H-2EFFFFH
	BA99	32 Kwords	2E0000H-2E7FFFH
	BA98	32 Kwords	2D8000H-2DFFFFH
	BA97	32 Kwords	2D0000H-2D7FFFH
	BA96	32 Kwords	2C8000H-2CFFFFH
	BA95	32 Kwords	2C0000H-2C7FFFH
	BA94	32 Kwords	2B8000H-2BFFFFH
	BA93	32 Kwords	2B0000H-2B7FFFH
	BA92	32 Kwords	2A8000H-2AFFFFH
	BA91	32 Kwords	2A0000H-2A7FFFH
	BA90	32 Kwords	298000H-29FFFFH

Table 2. Flash Memory Bottom Boot Block Address (KBA0101A0)

KBA0101A0	Block	Block Size	Address Range Word Mode (x16)
Bank4	BA89	32 Kwords	290000H-297FFFH
	BA88	32 Kwords	288000H-28FFFFH
	BA87	32 Kwords	280000H-287FFFH
	BA86	32 Kwords	278000H-27FFFFH
	BA85	32 Kwords	270000H-277FFFH
	BA84	32 Kwords	268000H-26FFFFH
	BA83	32 Kwords	260000H-267FFFH
	BA82	32 Kwords	258000H-25FFFFH
	BA81	32 Kwords	250000H-257FFFH
	BA80	32 Kwords	248000H-24FFFFH
	BA79	32 Kwords	240000H-247FFFH
Bank3	BA78	32 Kwords	238000H-23FFFFH
	BA77	32 Kwords	230000H-237FFFH
	BA76	32 Kwords	228000H-22FFFFH
	BA75	32 Kwords	220000H-227FFFH
	BA74	32 Kwords	218000H-21FFFFH
	BA73	32 Kwords	210000H-217FFFH
	BA72	32 Kwords	208000H-20FFFFH
	BA71	32 Kwords	200000H-207FFFH
	BA70	32 Kwords	1F8000H-1FFFFFH
	BA69	32 Kwords	1F0000H-1F7FFFH
	BA68	32 Kwords	1E8000H-1EFFFFH
	BA67	32 Kwords	1E0000H-1E7FFFH
	BA66	32 Kwords	1D8000H-1DFFFFH
	BA65	32 Kwords	1D0000H-1D7FFFH
	BA64	32 Kwords	1C8000H-1CFFFFH
	BA63	32 Kwords	1C0000H-1C7FFFH
	BA62	32 Kwords	1B8000H-1BFFFFH
	BA61	32 Kwords	1B0000H-1B7FFFH
	BA60	32 Kwords	1A8000H-1AFFFFH
	BA59	32 Kwords	1A0000H-1A7FFFH
	BA58	32 Kwords	198000H-19FFFFH
	BA57	32 Kwords	190000H-197FFFH
	BA56	32 Kwords	188000H-18FFFFH
	BA55	32 Kwords	180000H-187FFFH
	BA54	32 Kwords	178000H-17FFFFH
	BA53	32 Kwords	170000H-177FFFH
	BA52	32 Kwords	168000H-16FFFFH
	BA51	32 Kwords	160000H-167FFFH
	BA50	32 Kwords	158000H-15FFFFH
	BA49	32 Kwords	150000H-157FFFH
	BA48	32 Kwords	148000H-14FFFFH
	BA47	32 Kwords	140000H-147FFFH
	BA46	32 Kwords	138000H-13FFFFH
	BA45	32 Kwords	130000H-137FFFH

Table 2. Flash Memory Bottom Boot Block Address (KBA0101A0)

KBA0101A0	Block	Block Size	Address Range Word Mode (x16)
Bank3	BA44	32 Kwords	128000H-12FFFFH
	BA43	32 Kwords	120000H-127FFFH
	BA42	32 Kwords	118000H-11FFFFH
	BA41	32 Kwords	110000H-117FFFH
	BA40	32 Kwords	108000H-10FFFFH
	BA39	32 Kwords	100000H-107FFFH
	BA38	32 Kwords	F8000H-FFFFFH
	BA37	32 Kwords	F0000H-F7FFFH
	BA36	32 Kwords	E8000H-EFFFFH
	BA35	32 Kwords	E0000H-E7FFFH
	BA34	32 Kwords	D8000H-DFFFFH
	BA33	32 Kwords	D0000H-D7FFFH
	BA32	32 Kwords	C8000H-CFFFFH
	BA31	32 Kwords	C0000H-C7FFFH
	BA30	32 Kwords	B8000H-BFFFFH
	BA29	32 Kwords	B0000H-B7FFFH
	BA28	32 Kwords	A8000H-AFFFFH
	BA27	32 Kwords	A0000H-A7FFFH
	BA26	32 Kwords	98000H-9FFFFH
	BA25	32 Kwords	90000H-97FFFH
	BA24	32 Kwords	88000H-8FFFFH
	BA23	32 Kwords	80000H-87FFFH
Bank2	BA22	32 Kwords	78000H-7FFFFH
	BA21	32 Kwords	70000H-77FFFH
	BA20	32 Kwords	68000H-6FFFFH
	BA19	32 Kwords	60000H-67FFFH
	BA18	32 Kwords	58000H-5FFFFH
	BA17	32 Kwords	50000H-57FFFH
	BA16	32 Kwords	48000H-4FFFFH
	BA15	32 Kwords	40000H-47FFFH
Bank1	BA14	32 Kwords	38000H-3FFFFH
	BA13	32 Kwords	30000H-37FFFH
	BA12	32 Kwords	28000H-2FFFFH
	BA11	32 Kwords	20000H-27FFFH
	BA10	32 Kwords	18000H-1FFFFH
	BA9	32 Kwords	10000H-17FFFH
	BA8	32 Kwords	08000H-0FFFFH
	BA7	4 Kwords	07000H-07FFFH
	BA6	4 Kwords	06000H-06FFFH
	BA5	4 Kwords	05000H-05FFFH
	BA4	4 Kwords	04000H-04FFFH
	BA3	4 Kwords	03000H-03FFFH
	BA2	4 Kwords	02000H-02FFFH
	BA1	4 Kwords	01000H-01FFFH
	BA0	4 Kwords	00000H-00FFFH

Flash MEMORY COMMAND DEFINITION

Table 3. Command List (F-$\overline{WP}$ = V_{IH} or V_{IL})

Command	1st Cycle			2nd Cycle				3rd Cycle		
	Mode	Address	Data[1] (DQ0-15)	Mode	Address A21-A18	Address A0	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)
Read Array	Write	X	FFH							
Sequential Page Read	Write	X	F3H	Read	SA[5]		RD0	Read	SA+i[6]	RDi
Device Identifier	Write	Bank[2]	90H	Read	Bank[2]	IA[3]	ID			
Read Status Register	Write	Bank[2]	70H	Read	Bank[2]		SRD[4]			
Clear Status Register	Write	X	50H							
Suspend	Write	Bank[2]	B0H							
Resume	Write	Bank[2]	D0H							

Notes : 1. Upper byte data (DQ15-DQ8) is ignored.
2. Bank=Bank address (bank1-Bank4:A21-18)
3. IA=ID code address:A0=V_{IL} (Manufacture's code):A0=V_{IH} (Device code), ID=ID code
4. SRD=Status Register Data
5. SA=Sequential page Address:A21-A3, A2-A0:0h
6. SA+i;A21-A3 must be flxed and A2-A0 must be incremented from 0h to 7h.

Table 4. Command List (F-$\overline{WP}$ = V_{IH})

Command	1st Cycle			2nd Cycle			3rd Cycle		
	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)
Word Program	Write	Bank	40H	Write	WA[2]	WD[2]			
Page Program	Write	Bank	41H	Write	WA0[3]	WD0[3]	Write	WAn[3]	WDn[3]
Page Buffer to Flash	Write	Bank	0EH	Write	WA[4]	D0[1]			
Block Erase / Confirm	Write	Bank	20H	Write	BA[5]	D0[1]			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0[1]			
Clear Page Buffer	Write	X	55H	Write	X	D0[1]			
Single Date Load to Page Buffer	Write	Bank	74H	Write	WA	WD			
Flash to Page Buffer	Write	Bank	F1H	Write	RA[6]	D0[1]			

Notes : 1. Upper byte data (DQ15-DQ8) is ignored.
2. WA=Write Address, WD=Write Data
3. WA0, WAn=Write Address, WD0, WDn=Write Data, Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128-word x 16-bit), and also A21-A7(block address, page address) must be valid.
4. WA=Write Address:A21-A7 (block address, page address) must be valid.
5. BA=Block Address:A21-A12(Bank1), A21-A15(Bank2, Bank3, Bank4)
6. RA=Read Address:A21-A7 (block address, page address) must be valid.

Flash MEMORY COMMAND DEFINITION

Software lock release operation needs following consecutive 7bus cycles. Moreover, additional 127 bus cycles are needed for page program operation.

Table 5. Command List (F-$\overline{WP}$ = V_{IH} or V_{IL})

Setup Command for Software Lock Release	1st Cycle			2nd Cycle			3rd Cycle		
	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)
Word Program	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Page Program[3]	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Page Buffer to Flash	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Block Erase / Confirm	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Erase All Unlocked Blocks	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Clear Page Buffer	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Single Data Load to Page Buffer	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH
Flash to Page Buffer	Write	Bank	60H	Write	Bank	Block[6]	Write	Bank	ACH

Setup Command for Software Lock Release	4th Cycle			5th Cycle		
	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)
Word Program	Write	Bank	Block[6]	Write	Bank	78H
Page Program[3]	Write	Bank	Block[6]	Write	Bank	78H
Page Buffer to Flash	Write	Bank	Block[6]	Write	Bank	78H
Block Erase / Confirm	Write	Bank	Block[6]	Write	Bank	78H
Erase All Unlocked Blocks	Write	Bank	Block[6]	Write	Bank	78H
Clear Page Buffer	Write	Bank	Block[6]	Write	Bank	78H
Single Data Load to Page Buffer	Write	Bank	Block[6]	Write	Bank	78H
Flash to Page Buffer	Write	Bank	Block[6]	Write	Bank	78H

Setup Command for Software Lock Release	6th Cycle			7th Cycle			8th-134th Cycle		
	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)	Mode	Address	Data[1] (DQ0-15)
Word Program	Write	Bank	40h	Write	WA[2]	WD[2]			
Page Program[3]	Write	Bank	41h	Write	WA0[3]	WD0[3]	Write	WAn[3]	WDn[3]
Page Buffer to Flash	Write	Bank	0Eh	Write	WA[4]	D0[1]			
Block Erase / Confirm	Write	Bank	20H	Write	BA[5]	D0[1]			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0[1]			
Clear Page Buffer	Write	X	55H	Write	X	D0[1]			
Single Data Load to Page Buffer	Write	Bank	74H	Write	WA	WD			
Flash to Page Buffer	Write	Bank	F1H	Write	RA[7]	D0[1]			

Notes :
1. Upper byte data (DQ15-DQ8) is ignored.
2. WA=Write Address, WD=Write Data
3. WA0, WAn=Write Address, WD0, WDn=Write Data, Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128 word x 16 bit), and also A21-A7(block address, page address) must be valid.
4. WA=Write Address:A21-A7 (block address, page address) must be valid.
5. BA=Block Address:A21-A12(Bank1), A21-A15(Bank2, Bank3, Bank4)
6. Block=Block Address:A21-A15, $\overline{\text{Block}}$=$\overline{\text{A21-A15}}$

Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Block	Fixed0	A21	A20	A19	A18	A17	A16	A15
$\overline{\text{Block}}$	Fixed0	$\overline{\text{A21}}$	$\overline{\text{A20}}$	$\overline{\text{A19}}$	$\overline{\text{A18}}$	$\overline{\text{A17}}$	$\overline{\text{A16}}$	$\overline{\text{A15}}$

7. RA=Read Address: A21-A7 (block address, page address) must be valid.

Table 6. Device ID Code

Code \ Pins	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Date
Manufacturer Code	V_{IL}	"0"	"0"	"0"	"1"	"1"	"1"	"0"	"0"	1CH
Devide Code (Bottom Boot)	V_{IH}	"0"	"0"	"1"	"0"	"1"	"0"	"1"	"0"	2AH
Devide Code (Top Boot)	V_{IH}	"0"	"0"	"1"	"0"	"1"	"0"	"1"	"1"	2BH

The output of upper byte data (DQ15-DQ7) is "0".

Table 7. Block Locking

F-$\overline{RP}$	F-$\overline{WP}$	Write Protection Provided					Notes
		Bank1		Bank2	Bank3	Bank4	
		Boot	Parameter/Main	Main	Main	Main	
V_{IL}	x	Locked	Locked	Locked	Locked	Locked	Deep Power Down Mode
V_{IH}	V_{IL}	Locked	Locked	Locked	Locked	Locked	All Blocks Locked (Valid to operate Software Lock Release)
	V_{IH}	Unlocked	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

F-$\overline{WP}$ pin must not be switched during performing Read / Write operations or WSM busy (WSMS=0).

Table 8. Status Register

Symbol (I/O Pin)	Status	Definition	
		"1"	"0"
S.R.7 (AQ7)	Write State Machine Status	Ready	Busy
S.R.6 (DQ6)	Suspend Status	Suspended	Operation in Progress/Completed
S.R.5 (DQ5)	Erase Status	Error	Successful
S.R.4 (DQ4)	Program Status	Error	Successful
S.R.3 (DQ3)	Block Status after Program	Error	Successful
S.R.2 (DQ2)	Reserved	-	-
S.R.1 (DQ1)	Reserved	-	-
S.R.0 (DQ0)	Reserved	-	-

Table 9. Flash Memory Operation Table

Mode \ Pins		F-$\overline{\text{CE1}}$	F-$\overline{\text{CE2}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	F-$\overline{\text{RP}}$	DQ0-15	
							Flash 1	Flash 2
Read	Array	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data-Output	High-Z
		V_{IH}	V_{IL}				High-Z	Data-Output
	Sequential	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data-Output	High-Z
		V_{IH}	V_{IL}				High-Z	Data-Output
	Status Register	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	High-Z
		V_{IH}	V_{IL}				High-Z	Status Register Data
	Identifier Code	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	High-Z
		V_{IH}	V_{IL}				High-Z	Identifier Code
Output Disable		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	High-Z	High-Z
Write	Program	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	Command / Data-In	High-Z
		V_{IH}	V_{IL}				High-Z	Command / Data-In
	Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	Command	High-Z
		V_{IH}	V_{IL}				High-Z	Command
	Others	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	Command	High-Z
		V_{IH}	V_{IL}				High-Z	Command
Standby		V_{IH}	V_{IH}	X[1)]	X	V_{IH}	High-Z	High-Z
Deep Power Down		X	X	X	X	V_{IL}	High-Z	High-Z

Notes : 1. X can be V_{IH} or V_{IL} for control pins

Flash DEVICE OPERATION

The 64Mbit DINOR IV Flash Memory includes on-chip program/erase control circuitry. The Write State Machine(WSM) control block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.
A Deep Power Down mode is enabled when the F-$\overline{RP}$ pin is at Vss, minimizing power consumption.

Read Mode

The 64Mbit DINOR IV Flash Memory has four read modes, which accesses to the memory array, the Sequential Page Read, the Device Identifier and the Status Register. The appropriate read commands are required to be written to the CUI. Upon initial device power up or after exit from deep power down, the 64Mbit DINOR IV Flash Memory automatically resets to read array mode. In the read array mode and in the conditions are low level input to $\overline{OE}$, high level input to $\overline{WE}$ and F-$\overline{RP}$, low level input to F-$\overline{CE}$ and address signals to the address inputs (A21 - A0) the data of the addressed location to the data input/output (DQ15-DQ0) is output.

Standby Mode

When F-$\overline{CE}$ is at V_{IH}, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

Output Disable

When $\overline{OE}$ is at V_{IH}, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

Automatic Power Down (APD)

The Automatic Power Down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or F-$\overline{CE}$ isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. During this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

Deep Power Down

When F-$\overline{RP}$ is at V_{IL}, the device is in the deep power down mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance (High-Z) state. After return from power down, the CUI is reset to Read Array, and the Status Register is cleared to value 80H. During block erase or program modes, F-$\overline{RP}$ low will abort either operation. Memory array data of the block being altered become invalid.

Write Mode

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing $\overline{WE}$ to low level and $\overline{OE}$ is at high level, while F-$\overline{CE}$ is at low level. Address and data are latched on the earlier rising edge of $\overline{WE}$ and F-$\overline{CE}$. Standard micro processor write timings are used.

Alternating Background Operation (BGO)

The 64Mbit DINOR IV Flash Memory allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Array Read operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation. BGO must be between Bank1, Bank2, Bank3, and Bank4.

Back Bank array Read (BBR)

In the 64Mbit DINOR IV Flash Memory , when one memory address is read according to a Read Mode in the case of the same as an access when a Read Mode command is input, an another Bank memory data can be read out (Random or Sequential Mode) by changing an another Bank address.

Software Command Definitions

The device operations are selected by writing specific software command into the Commnad User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

Sequential Page Read Command (F3H)

The Sequential Page Read command (F3H) timing can be used by writing the first command. This command is fast sequential 8 words read. During the read it is necessary to fix F-$\overline{CE}$ low and increase the addresses sequentially from 0h to 7h. The mode is kept until Read Array command is input. The first read of Seq. Page Read timing is the same as normal read (ta(CE)). F-$\overline{CE}$ should be fallen 'L". The read timing after the first is fast read (ta(PAD)). When an another sequential page (A21-A3) is accessed before one sequential page (one 8-word) read is not finished, once F-$\overline{CE}$ is at V_{IH} and A2-A0 data are 0h, after that F-$\overline{CE}$ is at V_{IL} we can use the first read of Seq. Page Read or normal read (ta(CE)).

Read Device Identifier Command (90H)

We can normally read device identifier codes when Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically. The contents of Status Register are latched on the later falling edge of $\overline{OE}$ must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicate various failure conditions. status read.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Program Commands

1) Word Program (40H)

Word program is executed by a two-command sequence. The Word program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation.

2) Page Program for Data Blocks (41H)

Page Program allows fast programming of 128words of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle, write data must be serially inputted. Address A6-A0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

3) Single Data Load to Page Buffer (74H) / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programmed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programming the data on the page buffer is cleared automatically.

Flash to Page Buffer Command (F1H/D0H)

Array data load to the page buffer is performed by writing the Flash to Page Buffer command of F1H followed by the Confirm command of D0H. An address within the page to be loaded is required. Then the array data can be copied into the other pages within the same bank by using the Page Buffer to Flash command.

Clear Page Buffer Command (55H/D0H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

Data Protection

The 64M-bit DINOR(IV) Flash Memory has a master Write Protect pin (F-$\overline{WP}$). When F-$\overline{WP}$ is at V_{IH}, all blocks can be programmed or erased. When F-$\overline{WP}$ is low, all blocks are in locked mode which prevents any modifications to memory blocks. Software Lock Release function is only command which allows to program or erase. See the BLOCK LOCKING table on 13 page for details.

Power Supply Voltage

When the power supply voltage is less than V_{LKO}, Low Vcc Lock-Out voltage, the device is set to the Read-only mode. Regarding DC electrical characteristics of V_{LKO}, see 18 page. A delay time of 2us is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin (2.7V). During power up, F-$\overline{RP}$ = Vss is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

Memory Organization

The 64Mbit DINOR IV Flash Memory is constructed by 2 boot blocks of 4K words, 6 parameter blocks of 4K words and 7 main blocks of 32K words in Bank1, by 8 main blocks of 32K words in Bank2 and by 56 main blocks of 32K words in Bank3 and Bank4.

CAPACITANCE

Item		Symbol	Test Condition	Min	Max	Unit
Input Capacitance	A21-A0, $\overline{OE}$, $\overline{WE}$, F-$\overline{CE}$, F-$\overline{WP}$, F-$\overline{RP}$	C_{IN}	TA=25°C, f=1MHz, Vin=Vout=0V		35	pF
Output Capacitance	DQ15-DQ0, F-RY/$\overline{BY}$	C_{OUT}			45	pF

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
F-Vcc Voltage	F-Vcc	With Respect to Vss	-0.2 to +4.6	V
All input or Output Voltage[1)]	VI1		-0.6 to +4.6	
Ambient Temperature	Ta		-40 to +85	°C
Temperature under Bias	Tbs		-50 to +95	
Storage Temperature	Tstg		-65 to +125	
Outputs Short Circuit Current	Iout		100 (Max.)	mA

Notes : 1. Minimum DC voltage is -0.5V on input / output pins. During transitions, the level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input / output pins is F-Vcc+0.5V which, during transitions, may overshoot to F-Vcc+1.5V for periods <20ns.

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ[1)]	Max	Unit
Input Leakage Current	I_{LI}	0V<V_{IN}<F-Vcc				±1.0	µA
Output Leackage Current	I_{LO}	0V<V_{OUT}<F-Vcc				±1.0	µA
Vcc Standby Current	$I_{SB}1$	F-Vcc=3.3V, V_{IN}=V_{IL}/V_{IH}, F-$\overline{CE}$=F-$\overline{RP}$=F-$\overline{WP}$=V_{IH}			50	200	µA
	$I_{SB}2$	F-Vcc=3.3V, V_{IN}=Vss/F-Vcc, F-$\overline{CE}$=F-$\overline{RP}$=F-$\overline{WP}$=F-Vcc±0.3V			0.1	5	µA
Vcc Deep Power Down Current	$I_{SB}3$	F-Vcc=3.3V, V_{IN}/V_{IH}, F-$\overline{RP}$=V_{IL}			5	15	µA
	$I_{SB}4$	F-Vcc=3.3V, V_{IN}=Vss or F-Vcc, F-$\overline{RP}$=F-Vss±0.3V			0.1	5	µA
Vcc Read Current for Word	$I_{CC}1$	F-Vcc=3.3V, V_{IN}=V_{IL}/V_{IH}, F-$\overline{RP}$=$\overline{WE}$=V_{IH}, F-$\overline{CE}$=$\overline{OE}$=V_{IL}, Iout=0mA	5MHz		20	30	mA
			1MHz		4	8	mA
Vcc Sequential Page Read Current	$I_{CC}1P$		5MHz		5	10	mA
Vcc Write Current for Word	$I_{CC}2$	F-Vcc=3.3V, V_{IN}=V_{IL}/V_{IH}, F-$\overline{RP}$=$\overline{OE}$=V_{IH}, F-$\overline{CE}$=$\overline{WE}$=V_{IL}				15	mA
Vcc Program Current	$I_{CC}3$	F-Vcc=3.3V, V_{IN}=V_{IL}/V_{IH}, F-$\overline{CE}$=F-$\overline{RP}$=F-$\overline{WP}$=V_{IH}				35	mA
Vcc Erase Current	$I_{CC}4$	F-Vcc=3.3V, V_{IN}=V_{IL}/V_{IH}, F-$\overline{CE}$=F-$\overline{RP}$=F-$\overline{WP}$=V_{IH}				35	mA
Vcc Suspend Current	$I_{CC}5$	F-Vcc=3.3V, V_{IN}=V_{IL}/V_{IH}, F-$\overline{CE}$=F-$\overline{RP}$=F-$\overline{WP}$=V_{IH}				200	mA
Input Low Voltage	V_{IL}			-0.5		0.8	V
Input High Voltage	V_{IH}			2.0		F-Vcc +0.5	V
Output Low Voltage	V_{OL}	I_{OL}=4.0mA				0.45	V
Output High Voltage	$V_{OH}1$	I_{OH}=-2.0mA		0.85x F-Vcc			V
	$V_{OH}2$	I_{OL}=4-100µA		F-Vcc -0.4			V
Low F-Vcc Lock Out Voltage[2)]	V_{LKO}			1.5		2.2	V

Notes : All currents are in RMS unless otherwise noted
1. Typical values at F-Vcc=3.0V, Ta=25°C.
2. To protect initiation of write cycle during F-Vcc power up / down, a write cycle is locked out for F-Vcc less than V_{LKO}, Write State Machine is in Busy state, if F-Vcc is less than V_{LKO}, the alteration of memory contents may occur.

AC CHARACTERISTICS

Read Only Mode

Parameter	Symbol		Vcc=2.7V~3.3V			Unit
			Min	Typ	Max	
Read Cycle Time	tRC	tAVAV	85			ns
Address Access Time	ta(AD)	tAVQV			85	ns
Chip Enable Access Time	ta(CE)	tELQV			85	ns
Output Enable Access Time	ta(OE)	tGLQV			30	ns
Sequential Page Access Time (After 2nd Cycle)	ta(PAD)				45	ns
Sequential Page Setup Time	tASPR		-20			ns
Sequential Page Read F-$\overline{CE}$ "H" Time	tCEHRR		15			ns
Maximum Valid Time of Sequential Page Read	tRPCRR				20	ns
Chip Enable to Output in Low-Z	tCLZ	tELQX	0			ns
Chip Enable High to Output in High-Z	tDF(CE)	tEHQZ			25	ns
Output Enablr to Output in Low-Z	tOLZ	tGLQX	0			ns
Output Enable to High to Output in High-Z	tDF(OE)	tGHQZ			25	ns
F-$\overline{RP}$ Low to Output High-Z	tPHZ	tPLQZ			150	ns
Output Hold from F-$\overline{CE}$, $\overline{OE}$ and Address	tOH	tOH	0			ns
OE hold from $\overline{WE}$ High	tOEH	tWHGL	10			ns
F-RP Recovery to $\overline{CE}$ Low	tPS	tPHEL	150			ns

Notes : 1. Timing measurements are made under AC waveforms for read operation.

Read / Write Mode ($\overline{WE}$ Control)

Parameter	Symbol		Vcc=2.7V~3.3V			Unit
			Min	Typ	Max	
Wrie Cycle Time	tWC	tAVAV	85			ns
Address Setup Time	tAS	tAVWH	35			ns
Address Hold Time	tAH	tWHAX	0			ns
Data Setup time	tDS	tDVWH	35			ns
Data Hold time	tDH	tWHDX	0			ns
$\overline{OE}$ Holf from $\overline{WE}$ High	tOEH	tWHGL	10			ns
Chip Enable Setup Time	tCS	tELWL	0			ns
Chip Enable Hold Time	tCH	tWHEH	0			ns
Write Pulse Width	tWP	tWLWH	35			ns
Write Pulse Width High	tWPH	tWHWL	30			ns
$\overline{OE}$ Hold to $\overline{WE}$ Low	tGHWL	tGHWL	0			ns
Block Lock Setup to Write Enable High	tBLS	tPHHWH	85			ns
Block Lock Hold from Valid SRD	tBLH	tQVPH	0			ns
Duration of Auto Program Operation (Word Mode)	tDAP	tWHRH1		30	300	µs
Duration of Auto Program Operation (Page Mode)	tDAP	tWHRH1		4	80	ms
Duration of Auto Block Erase Operation	tDAE	tWHRH2		150	600	ms
Delay Time to Begin Internal Operation	tWHRL	tWHRL			85	ns
F-$\overline{RP}$ Recovery to F-$\overline{CE}$ Low	tPS	tPHWL	150			ns

Notes : 1. Read timing parameters during command write operations mode are the same as during read only operation mode.
2. Typical values at F-Vcc=3.0V and Ta=25°C.

AC CHARACTERISTICS

Read / Write Mode ($\overline{CE}$ Control)

Parameter	Symbol		Vcc=2.7V~3.3V			Unit
			Min	Typ	Max	
Write Cycle Time	tWC	tAVAV	85			ns
Address Setup Time	tAS	tAVWH	35			ns
Address Hold Time	tAH	tWHAX	0			ns
Data Setup Time	tDS	tDVWH	35			ns
Data Hold Time	tDH	tWHDX	0			ns
$\overline{OE}$ Hold from $\overline{WE}$ High	tOEH	tWHGL	10			ns
Write Enable Setup Time	tWS	tWLEL	0			ns
Write Enable Hold Time	tWH	tEHWH	0			ns
F-$\overline{CE}$ Pulse Width	tCEP	tELEH	35			ns
F-$\overline{CE}$ "H" Pulse Width	tCEPH	tEHEL	30			ns
$\overline{OE}$ Hold to $\overline{WE}$ Low	tGHEL	tGHEL	85			ns
Block Lock Setup to Write Enable High	tBLS	tPHHWH	85			ns
Block Lock Hold from Valid SRD	tBLH	tQVPH	0			ns
Duration of Auto Program Operation (Word Mode)	tDAP	tWHRH1		30	300	µs
Duration of Auto Program Operation (Page Mode)	tDAP	tWHRH1		4	80	ms
Duration of Auto Block Erase Operation	tDAE	tWHRH2		150	600	ms
Delay Time to Begin Internal Operation	tEHRL	tEHRL			90	ns
F-$\overline{RP}$ Recovery to F-$\overline{CE}$ Low	tPS	tPHWL	150			ns

Notes : 1. Timing measurements are made under AC waveforms for read operations
2. Typical values at F-Vcc=3.0V and Ta=25°C.

Program / Erase Time

Parameter	Min	Typ	Max	Unit
Block Erase Time		150	600	ms
Main Block Write Time		1	4	sec
Page Write Time		4	80	ms
Flash to Page Buffer Time		100	150	µs

Program Suspend / Erase Suspend Time

Parameter	Min	Typ	Max	Unit
Program Suspend Time			15	µs
Erase Suspend Time			15	µs

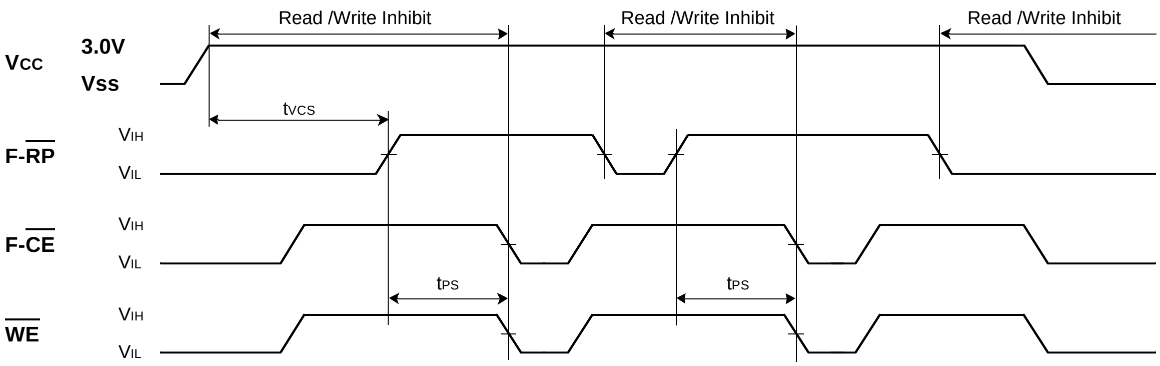
F-Vcc Power up / Down timing

Parameter		Min	Typ	Max	Unit
tVCS	F-RP=V_{IH} Setup Time from F-Vcc min.	2		15	µs

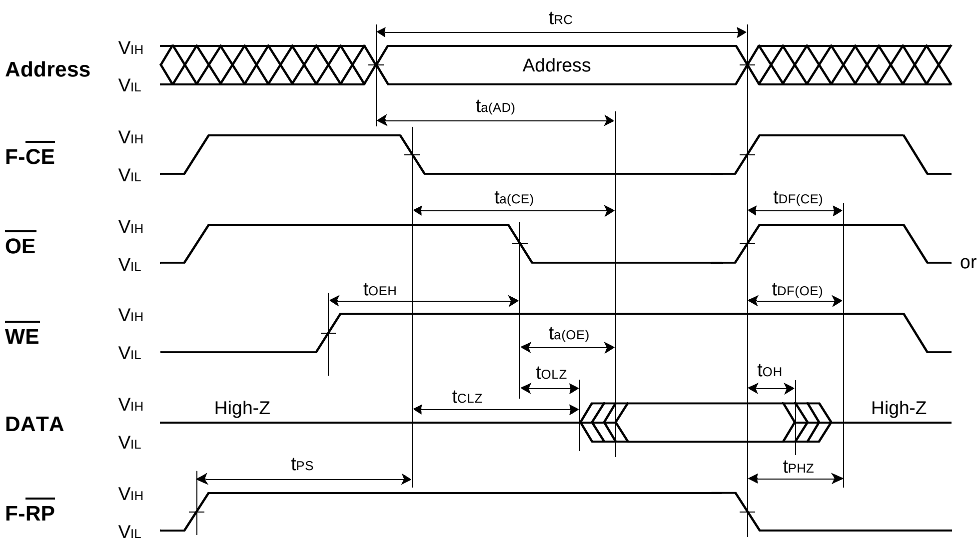
Please see 21 page.

During power up / down, by the noise pulses on control pins, the device has possibility of accidental erase of programming. The device must be protected against initiation of write cycle for memory contents during power up / down. The delay time of min. 2 micro sec is always required before read operation or write operation is initiated from the time F-Vcc reaches F-Vcc min. during power up /down. By holding F-$\overline{RP}$=V_{IL}, the contents of memory is protected during F-Vcc power up / down. During power up, F-$\overline{RP}$ must be held V_{IL} for min. 2us form the time F-Vcc reaches F-Vcc min.. During power down, F-$\overline{RP}$ must be held V_{IL} until F-Vcc reaches Vss. F-$\overline{RP}$ doesnt have latch mode, therefore F- $\overline{RP}$ must be held V_{IH} during read operation or erase / program operation.

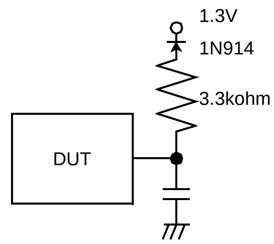
F-Vcc Power up / dowm Timing



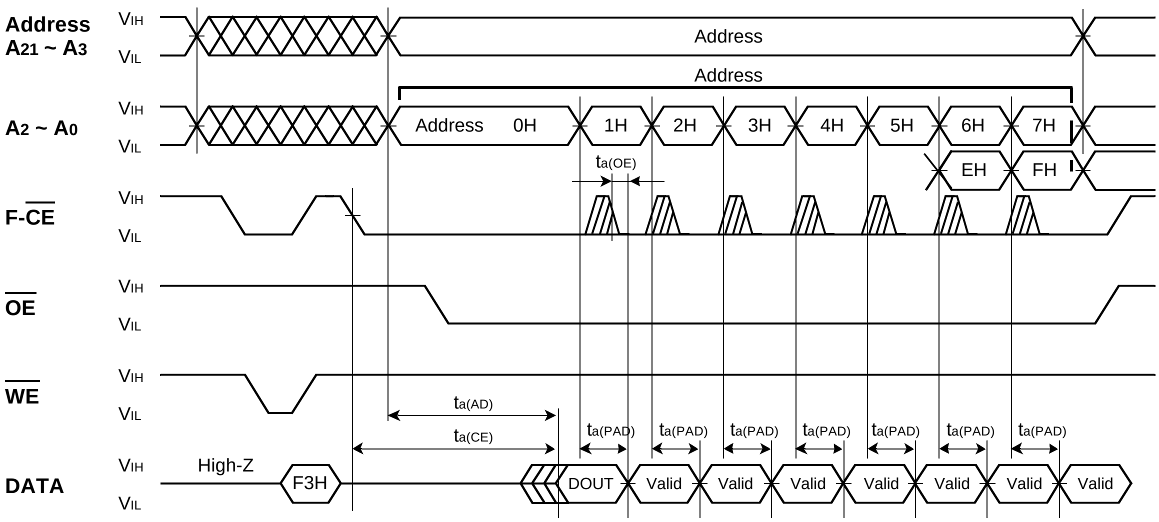
AC Waveforms for Read Operation and Test Conditions



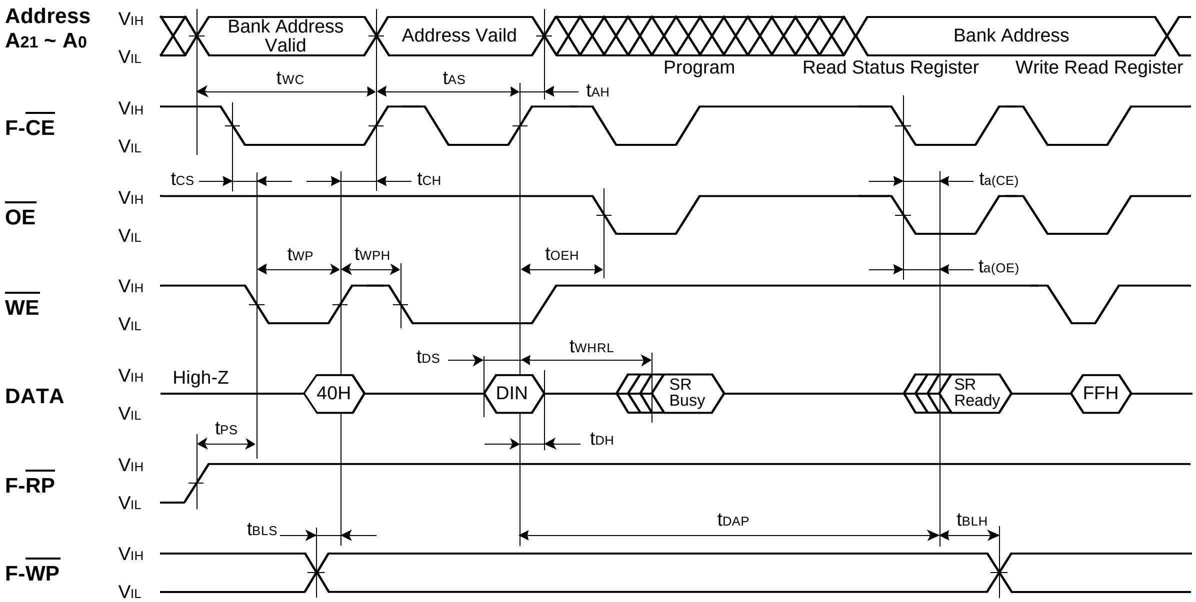
TEST CONDITIONS
FOR AC CHARACTERISTICS
Input Voltage: V_{IL}=0V, V_{IH}=Flash V_{CC}
Input Rise and Fall Times: ≤5ns
Reference Voltage
at timing measurement: (Flash V_{CC})/2
Output Load: 1TTL gate + CL(30pF)



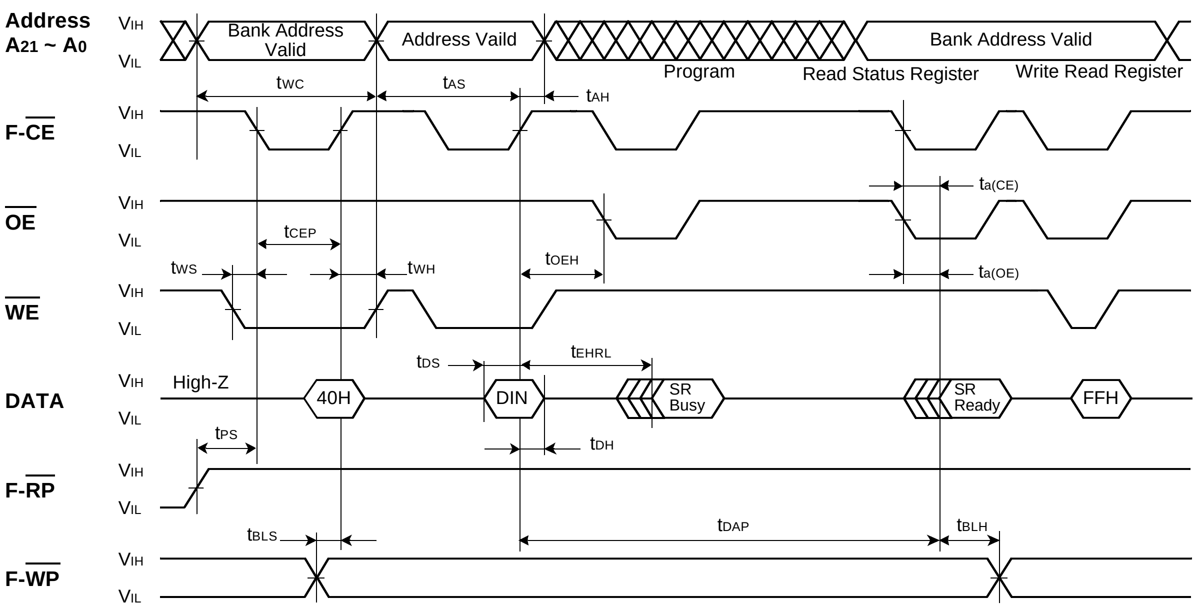
AC Waveforms for Sequential Page Read Operation



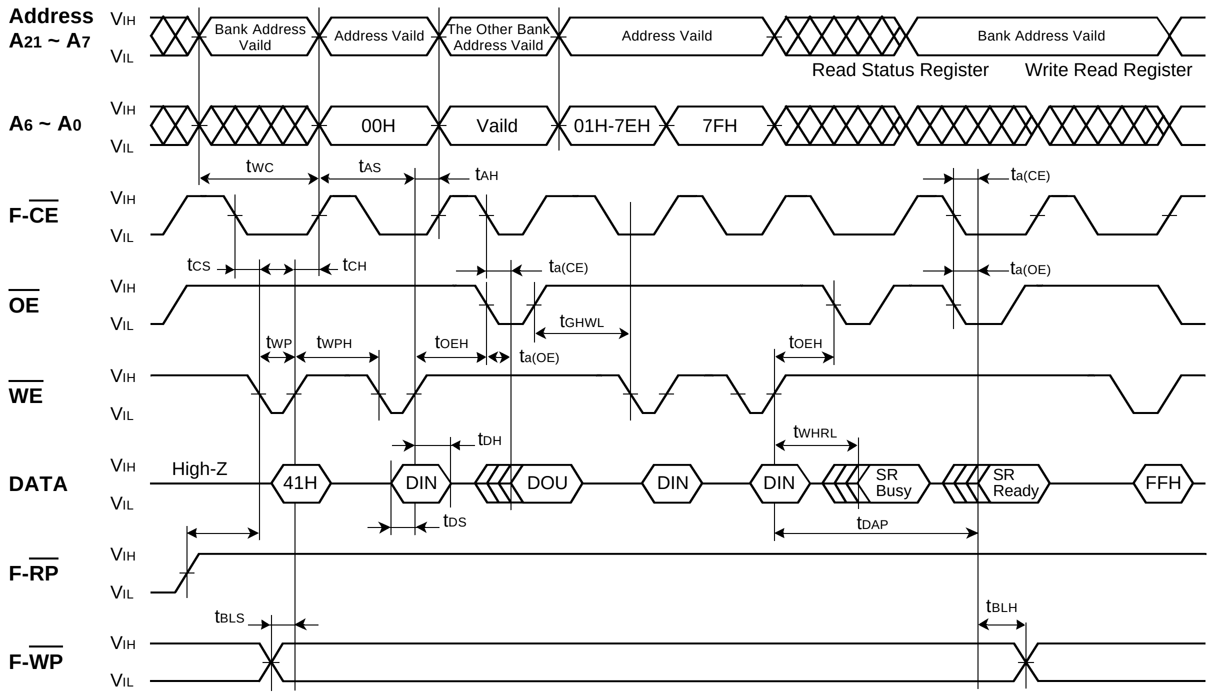
AC Waveforms for Word Program Operation($\overline{WE}$ Control)



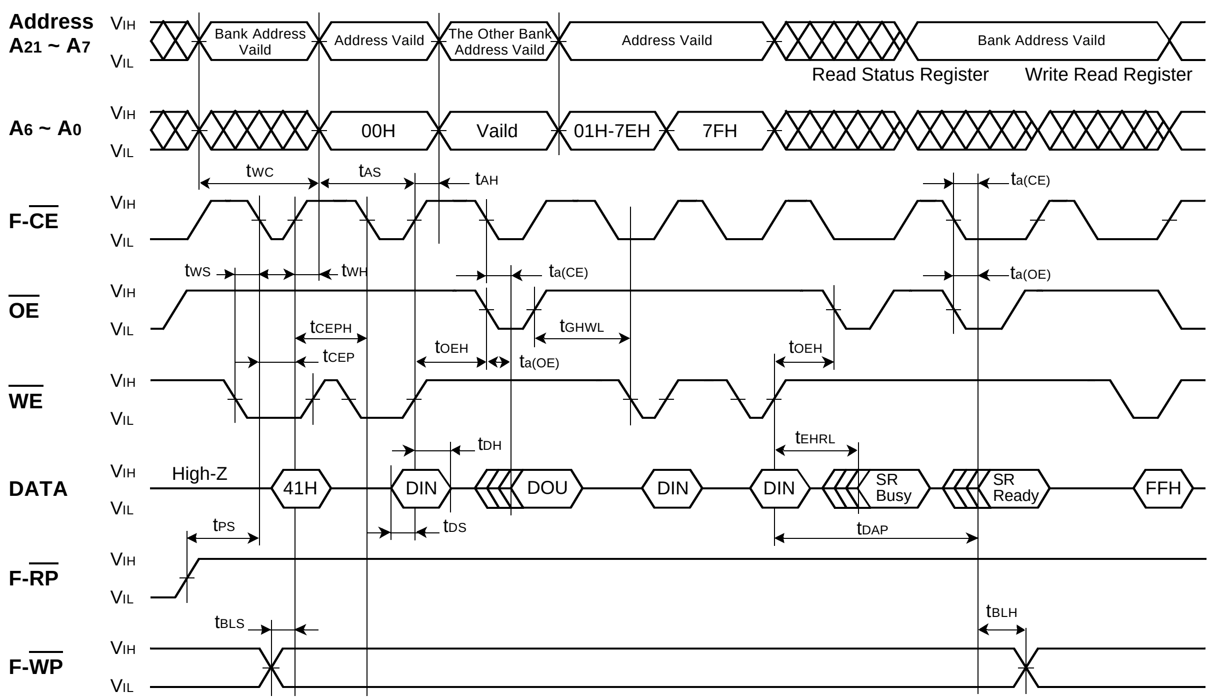
AC Waveforms for Word Program Operation($\overline{CE}$ Control)



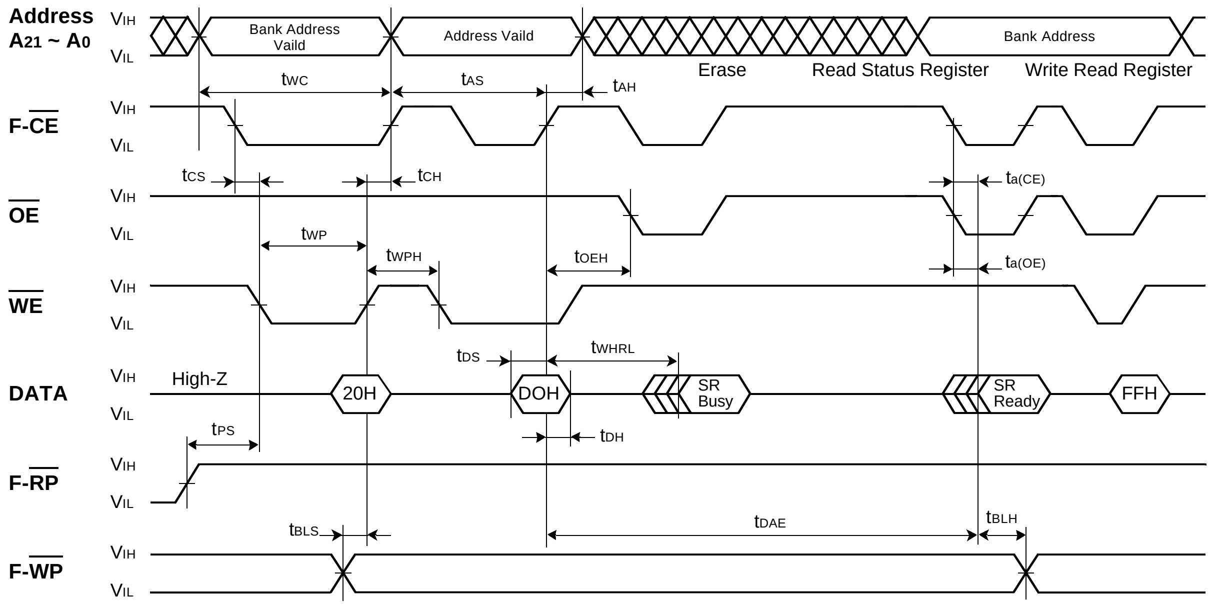
AC Waveforms for Page Program Operation($\overline{WE}$ Control)



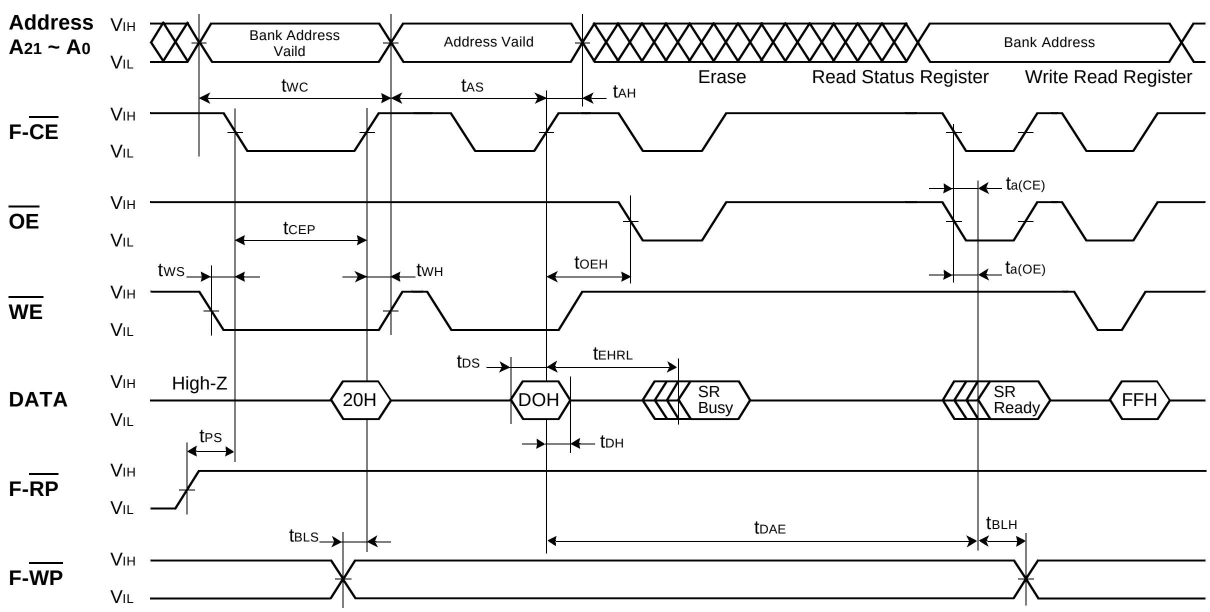
AC Waveforms for Page Program Operation($\overline{CE}$ Control)



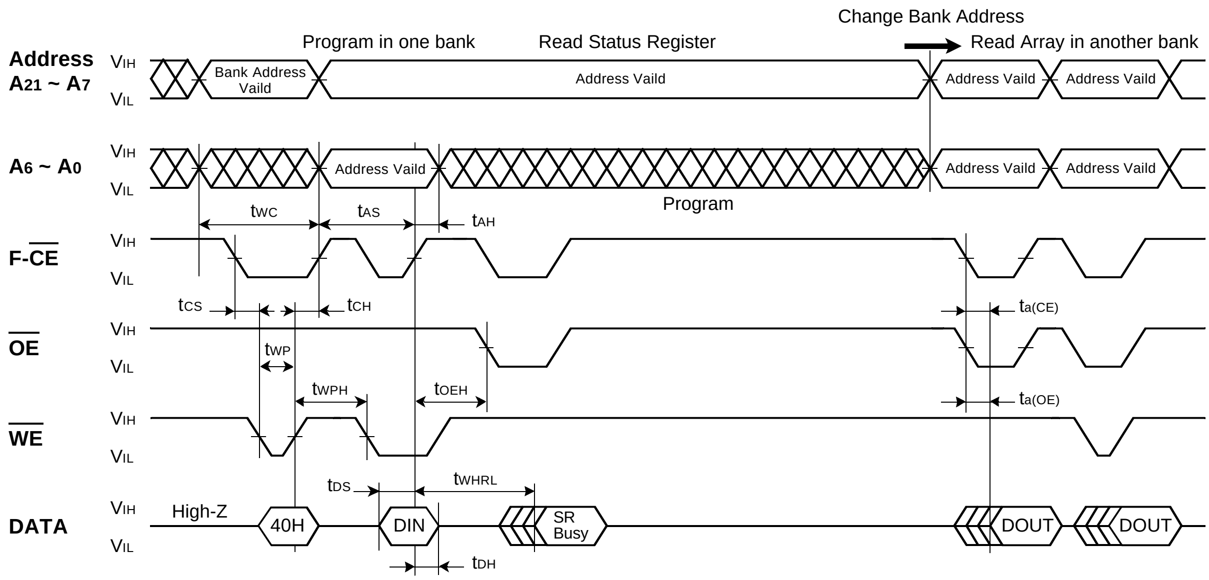
AC Waveforms for Erase Operation($\overline{WE}$ Control)



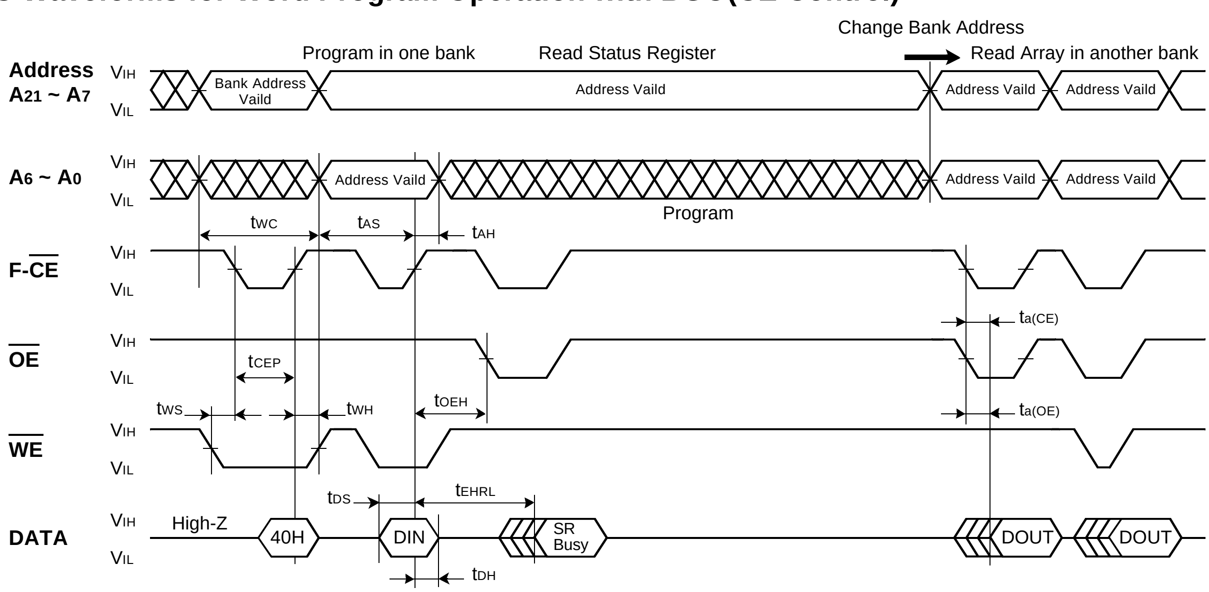
AC Waveforms for Erase Operation($\overline{CE}$ Control)



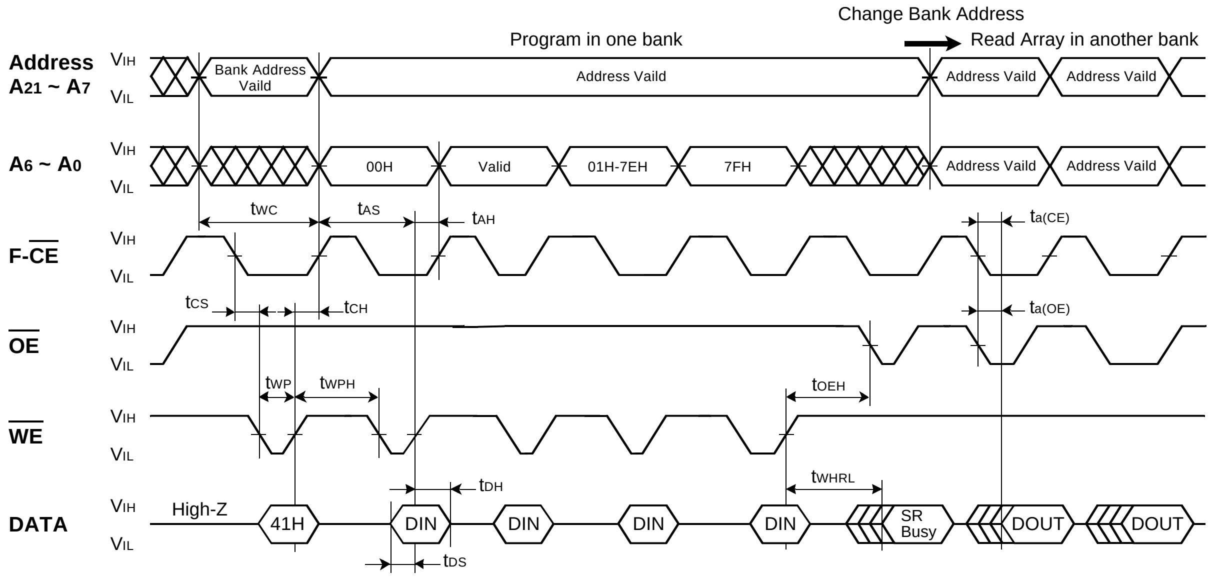
AC Waveforms for Word Program Operation with BGO($\overline{WE}$ Control)



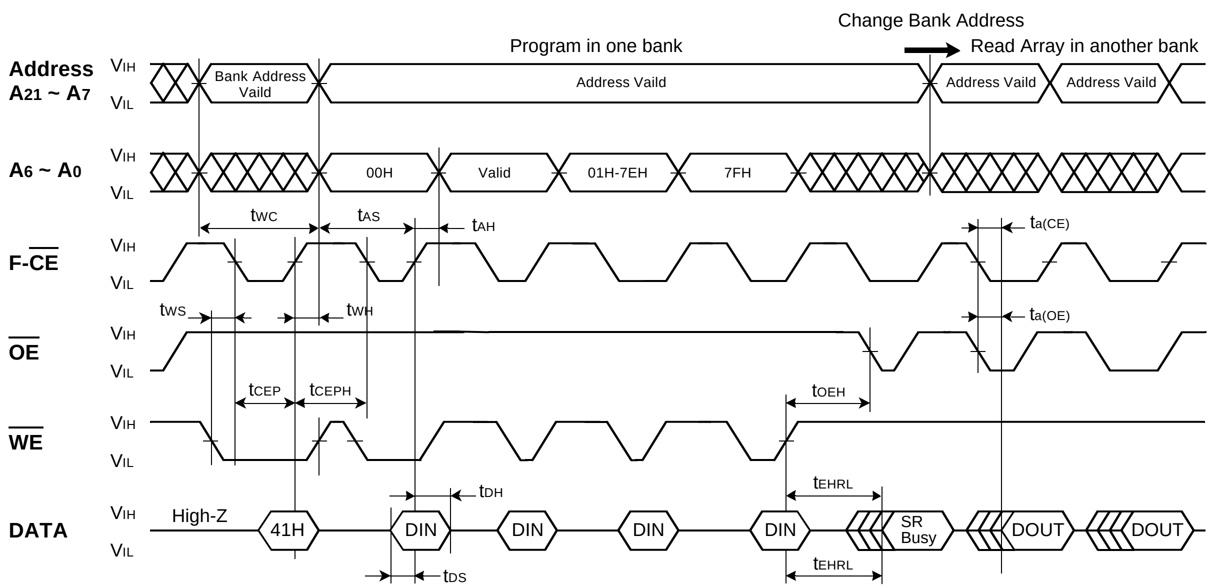
AC Waveforms for Word Program Operation with BGO($\overline{CE}$ Control)



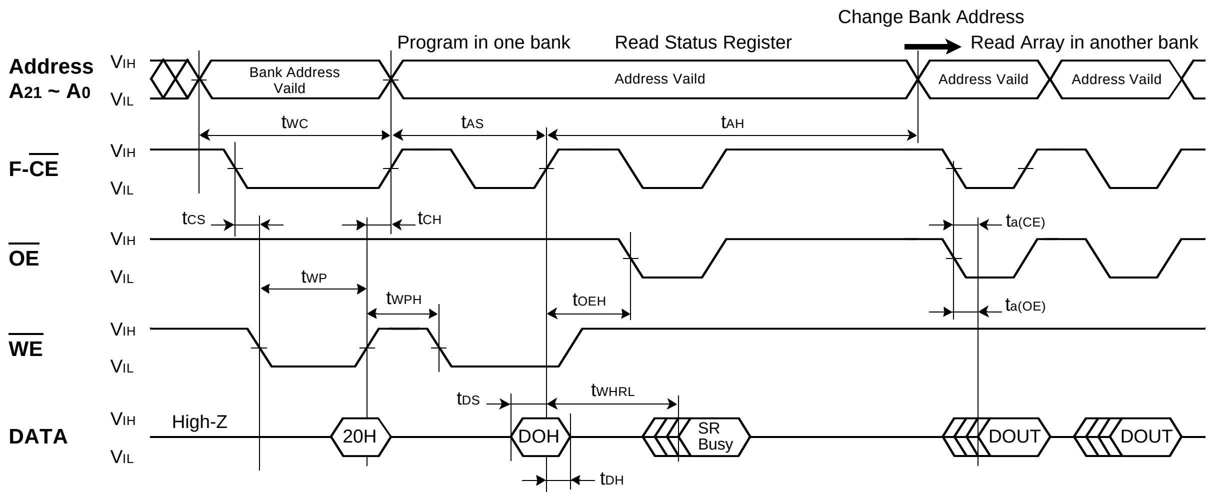
AC Waveforms for Page Program Operation with BGO($\overline{WE}$ Control)



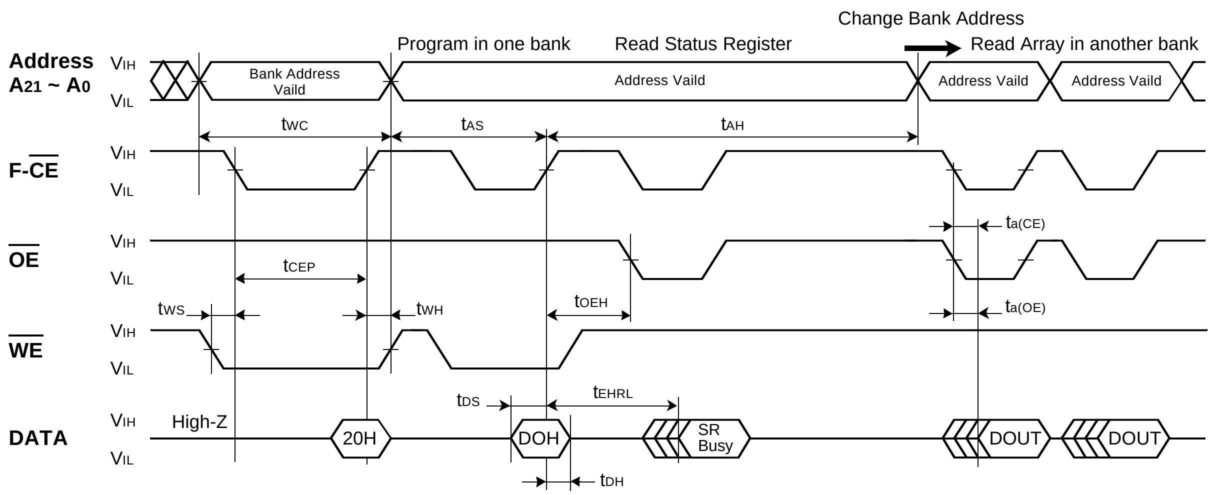
AC Waveforms for Page Program Operation with BGO($\overline{CE}$ Control)



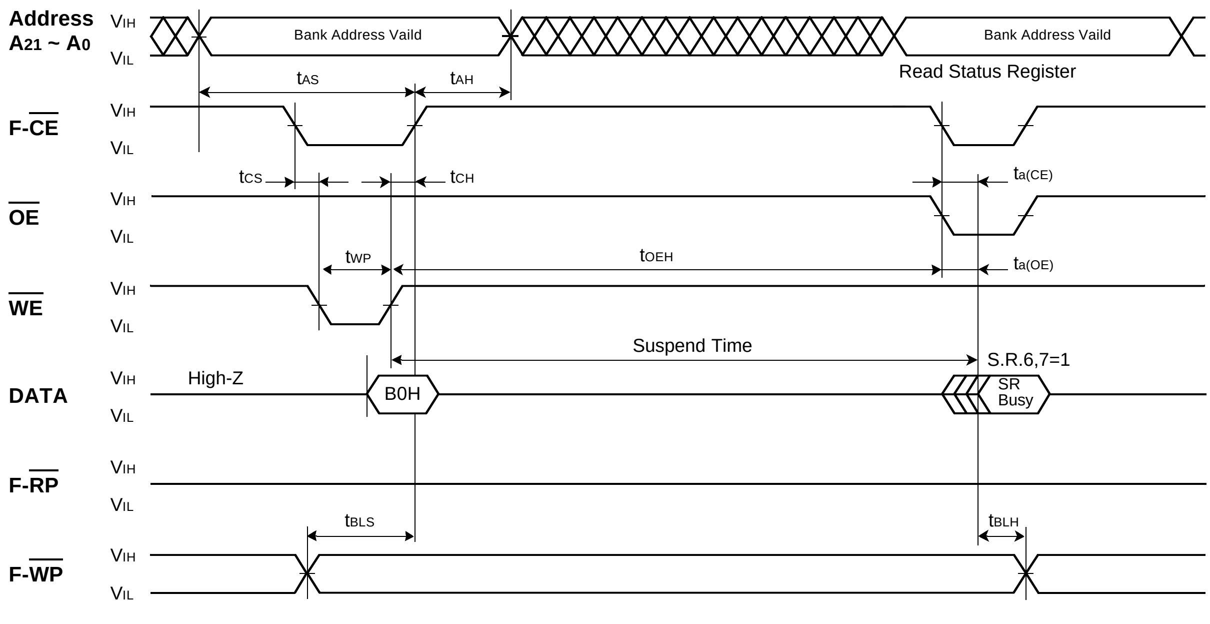
AC Waveforms for Erase Operation with BGO($\overline{WE}$ Control)



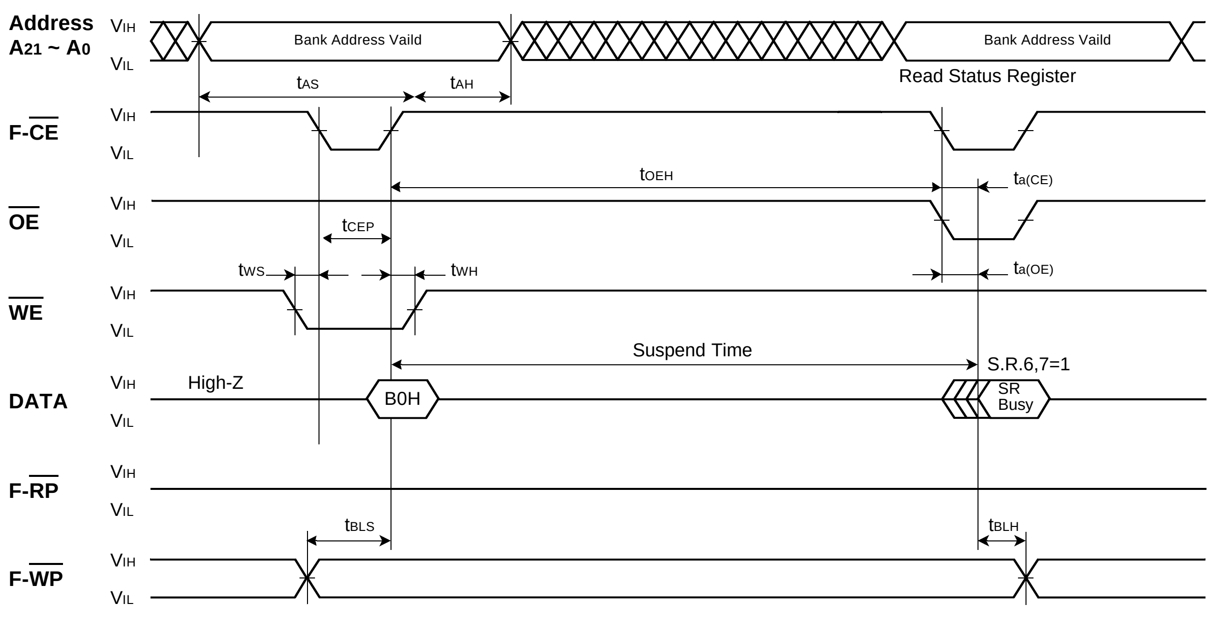
AC Waveforms for Erase Operation with BGO($\overline{CE}$ Control)



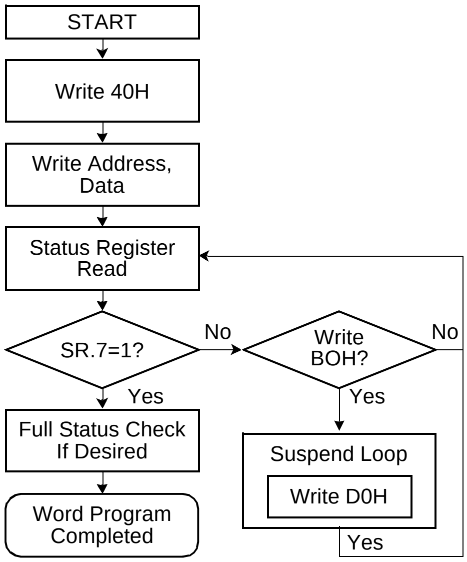
AC Waveforms for Suspend Operation($\overline{WE}$ Control)



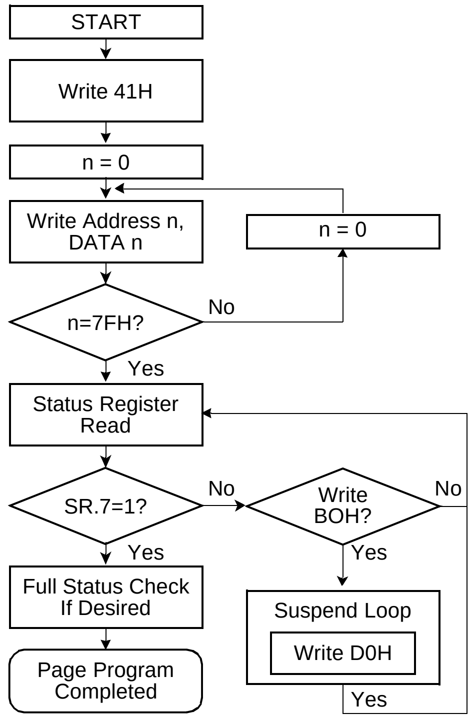
AC Waveforms for Suspend Operation($\overline{CE}$ Control)



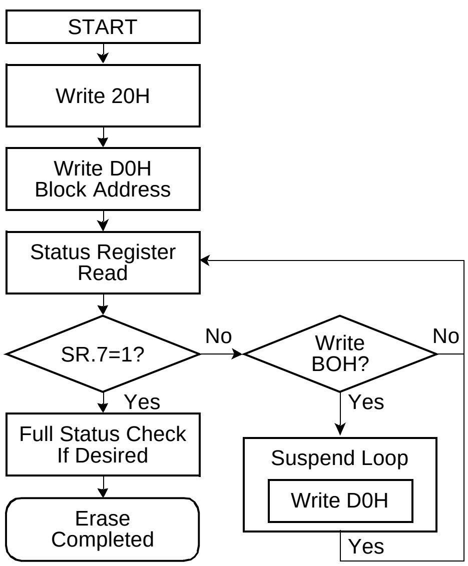
Word Program Flow Chart



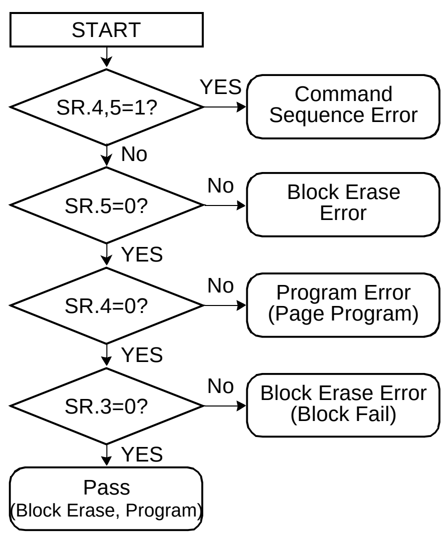
Page Program Flow Chart



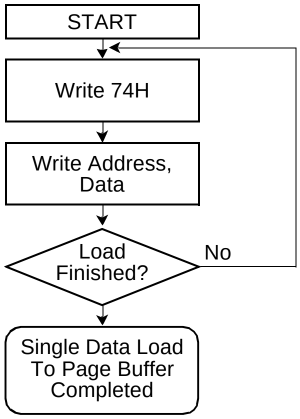
Block Erase Flow Chart



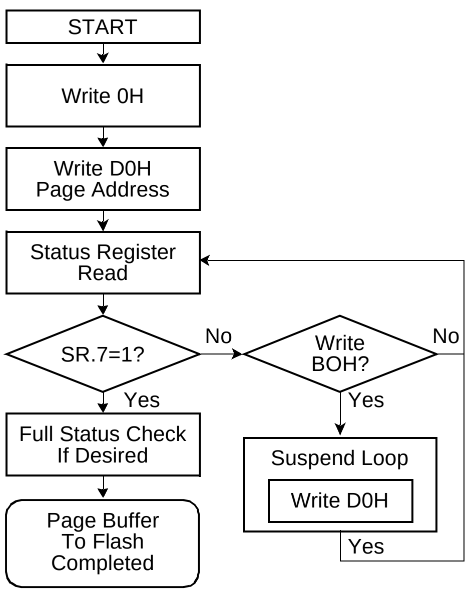
Status Register Check Flow Chart



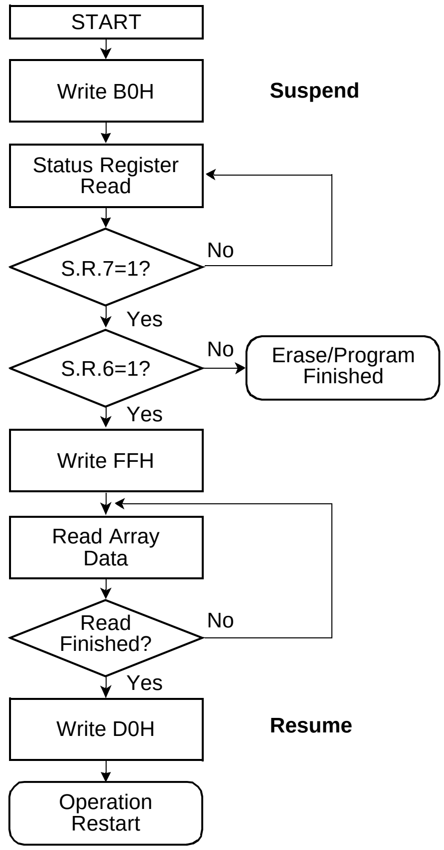
Single Data Load to Page Buffer Flow Chart



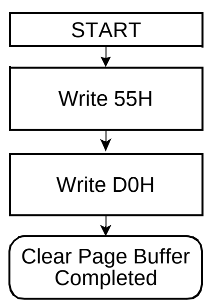
Page Buffer to Flash Flow Chart



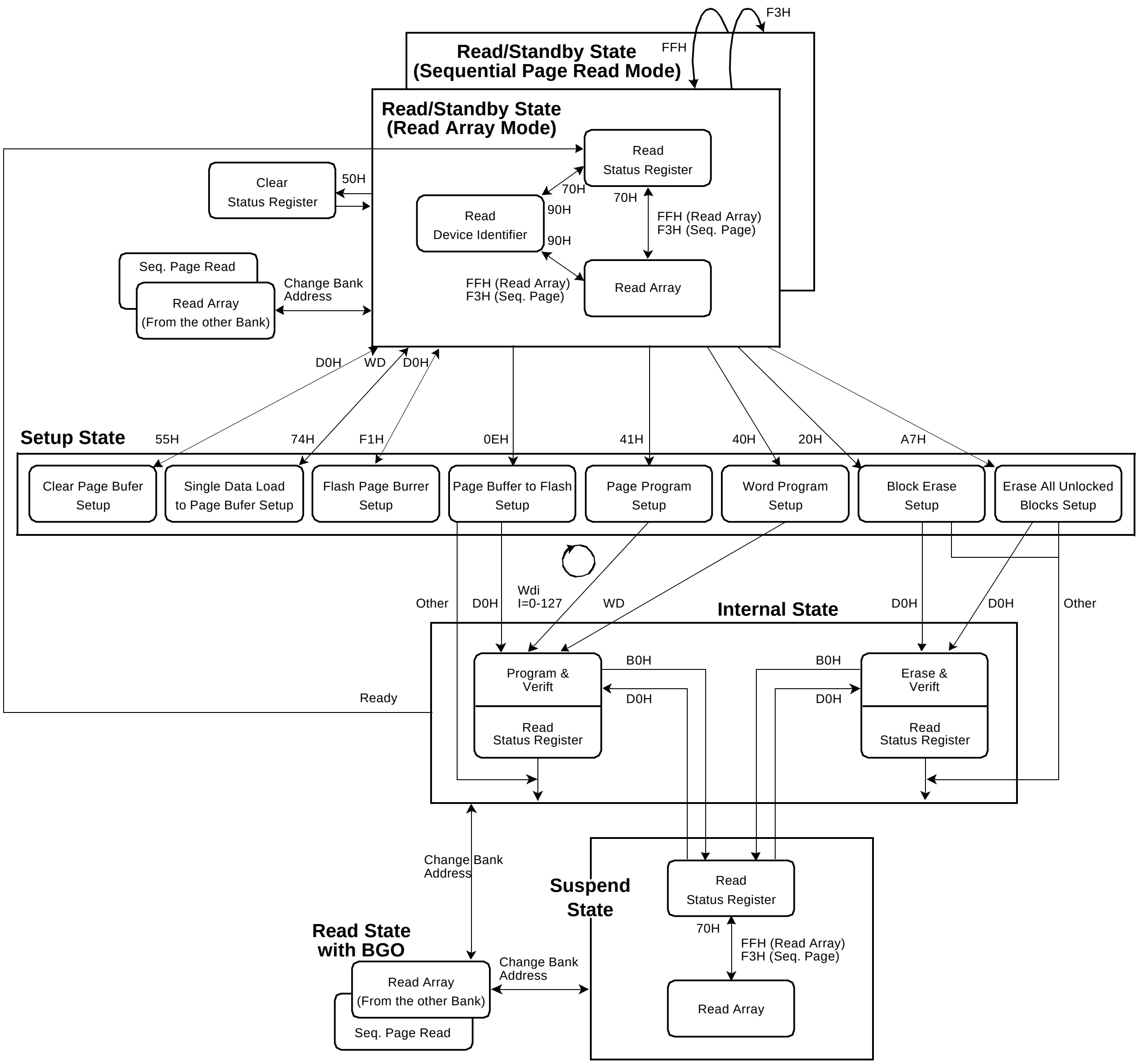
Suspend / Resume Flow Chart



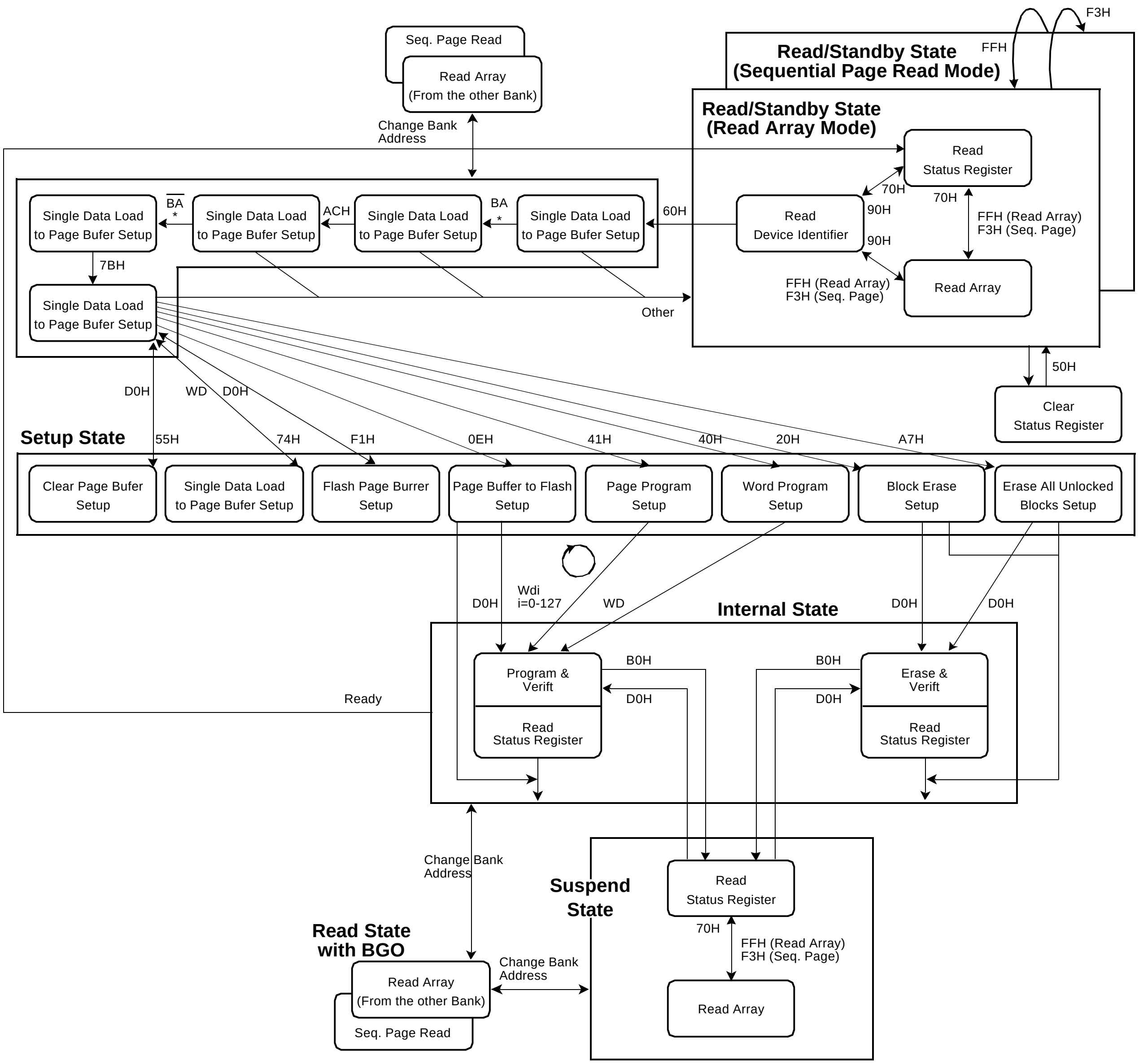
Clear Page Buffer Flow Chart



Operation Status ($\overline{WP}$=VIH)



Operation Status ($\overline{WP}$=VIL)



U*t*RAM & SRAM Part

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions longer than 1seconds may affect reliability.

FUNCTIONAL DESCRIPTION for U*t*RAM

$\overline{\text{CS}}$u	$\overline{\text{ZZ}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$u	$\overline{\text{UB}}$u	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected[2)]	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected[2)]	Deep Power Down
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselected[2)]	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled[2)]	Active
L	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled[2)]	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read[3)]	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read[3)]	Active
L	H	L	H	L	L	Dout	Dout	Word Read[3)]	Active
L	H	X[1)]	L	L	H	Din	High-Z	Lower Byte Write[3)]	Active
L	H	X[1)]	L	H	L	High-Z	Din	Upper Byte Write[3)]	Active
L	H	X[1)]	L	L	L	Din	Din	Word Write[3)]	Active

1. X means dont care.(Must be low or high state)
2. SRAM or one of Flash memories is allowable.
3. Others must be in High-Z.

FUNCTIONAL DESCRIPTION for SRAM

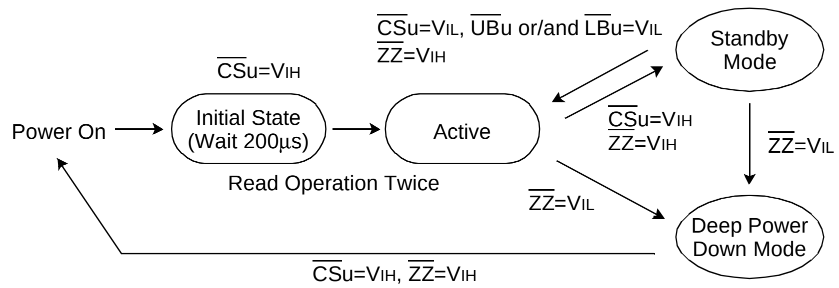
$\overline{\text{CS}}_{1s}$	CS_{2s}	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$s	$\overline{\text{UB}}$s	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected[2)]	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected[2)]	Standby
X[1)]	X[1)]	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselected[2)]	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled[2)]	Active
L	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled[2)]	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read[3)]	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read[3)]	Active
L	H	L	H	L	L	Dout	Dout	Word Read[3)]	Active
L	H	X[1)]	L	L	H	Din	High-Z	Lower Byte Write[3)]	Active
L	H	X[1)]	L	H	L	High-Z	Din	Upper Byte Write[3)]	Active
L	H	X[1)]	L	L	L	Din	Din	Word Write[3)]	Active

1. X means don't care. (Must be low or high state)
2. UtRAM or one of Flash memories is allowable.
3. Others must be in High-Z.

POWER UP SEQUENCE for U*t*RAM

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minium 200µs with $\overline{CS}$u=high.
3. Issue read operation at least twice.

STANDBY MODE STATE MACHINES for U*t*RAM



STANDBY MODE CHARACTERISTIC for U*t*RAM

Power Mode	Memory Cell Data	Standby Current(µA)	Wait Time(µs)
Standby	Valid	100	0
Deep Power Down	Invaild	10	200

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	2.9	3.1	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.3[3)]	-	0.6	V

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	35	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	45	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Item	Symbol	Test Conditions	Min	Typ[1)]	Max	Unit
Common	Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-2	-	2	µA
	Output leakage current	I_{LO}	$\overline{CS}=V_{IH}$, $\overline{ZZ}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V_{IO}=Vss to Vcc	-2	-	2	µA
	Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	Output high voltage	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V
U*t*RAM	Average operating current	I_{CC1u}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}\leq$0.2V, $\overline{ZZ}\geq$Vcc-0.2V, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$-0.2V	-	4	7	mA
		I_{CC2u}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}=V_{IL}$, $\overline{ZZ}=V_{IH}$, $V_{IN}=V_{IL}$ or V_{IH}	-	30	35	mA
	Standby Current(CMOS)	I_{SB1u}	$\overline{CS}\geq$Vcc-0.2V, $\overline{ZZ}\geq$Vcc-0.2V, Other inputs=Vss to Vcc	-	80	100	µA
	Deep Power Down	I_{SBDu}	$\overline{ZZ}\leq$0.2V, Other inputs=Vss to Vcc	-	5	10	µA
SRAM	Average operating current	I_{CC1S}	Cycle time=1µs, 100%duty, I_{IO}=0mA, $\overline{CS}_1\leq$0.2V, $\overline{LB}\leq$0.2V or/and $\overline{UB}\leq$0.2V, $CS_2\geq$Vcc-0.2V, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$-0.2V	-	-	2	mA
		I_{CC2S}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH}	-	-	30	mA
	Standby Current (CMOS)	I_{SB1S}	Other input =0~Vcc 1) $\overline{CS}_1\geq$Vcc-0.2V, $CS_2\geq$Vcc-0.2V ($\overline{CS}_1$ controlled) or 2) 0V$\leq CS_2\leq$0.2V(CS_2 controlled)	-	0.5	15	µA

1. Typical values are tested at V_{CC}=2.9V, T_A=25°C and not guaranteed.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load: C_L=50pF

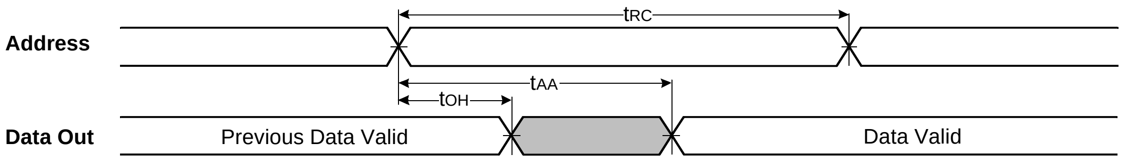
AC CHARACTERISTICS(V_{CC}=2.7~3.1V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			UtRAM 85ns[1]		SRAM 55ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	85	-	55	-	ns
	Address Access Time	t_{AA}	-	85	-	55	ns
	Chip Select to Output	t_{CO}	-	85	-	55	ns
	Output Enable to Valid Output	t_{OE}	-	40	-	25	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	85	-	55	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	20	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	20	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	20	ns
	Output Hold from Address Change	t_{OH}	5	-	10	-	ns
Write	Write Cycle Time	t_{WC}	85	-	55	-	ns
	Chip Select to End of Write	t_{CW}	70	-	45	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	70	-	45	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	70	-	45	-	ns
	Write Pulse Width	t_{WP}	60	-	40	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	0	20	ns
	Data to Write Time Overlap	t_{DW}	35	-	25	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

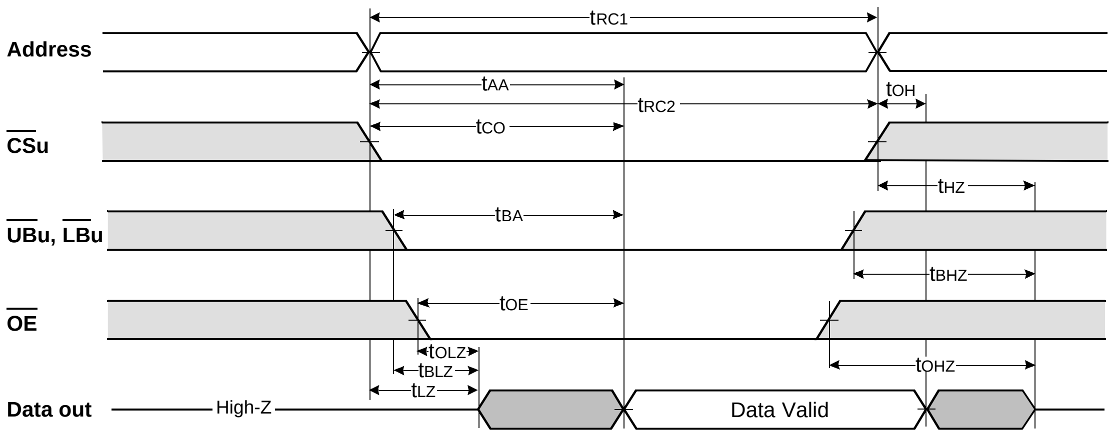
1. The limitation in continuous write operation is up to 50 times. If you want to write continuously over 50 times, please refer to the technical note.

TIMING DIAGRAMS for U*t*RAM

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CSu}=\overline{OE}=V_{IL}$, $\overline{ZZ}=\overline{WE}=V_{IH}$, $\overline{UBu}$ or/and $\overline{LBu}=V_{IL}$)



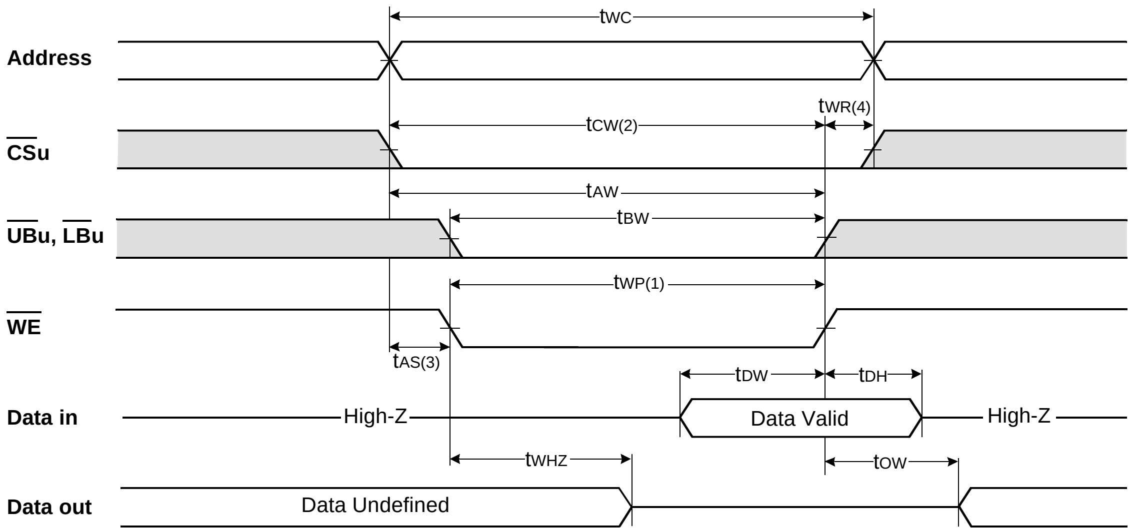
TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}=\overline{WE}=V_{IH}$)



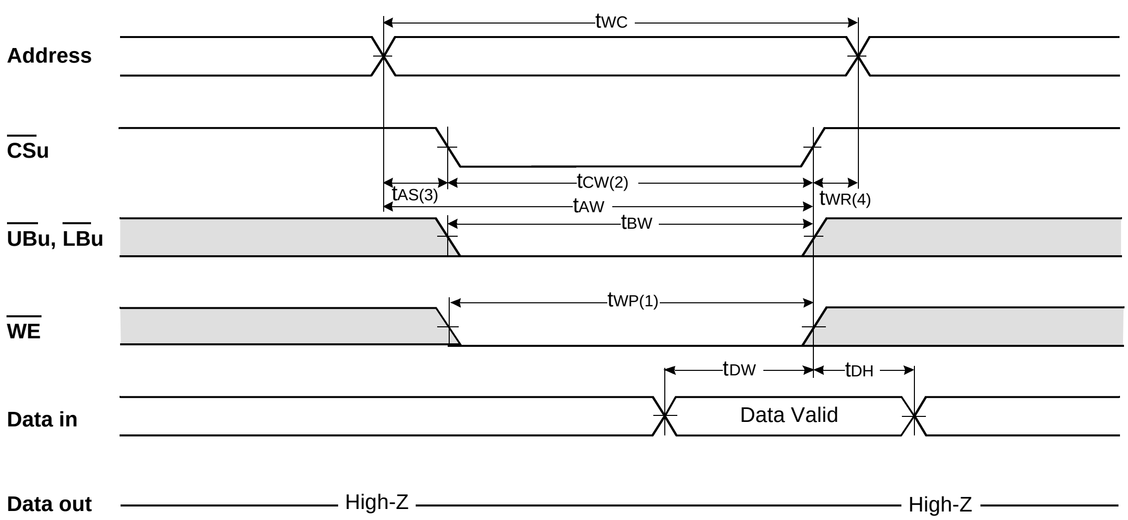
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined by longer one of t_{RC1} and t_{RC2}.
4. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).

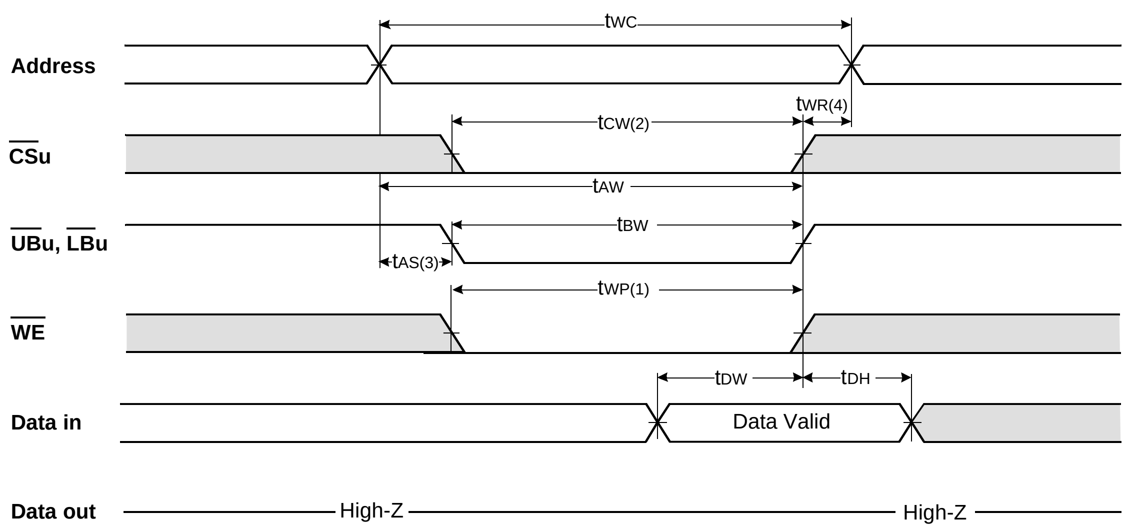
TIMING WAVEFORM OF WRITE CYCLE(1)(WE Controlled, ZZ=VIH)



TIMING WAVEFORM OF WRITE CYCLE(2)(CSu Controlled, ZZ=VIH)



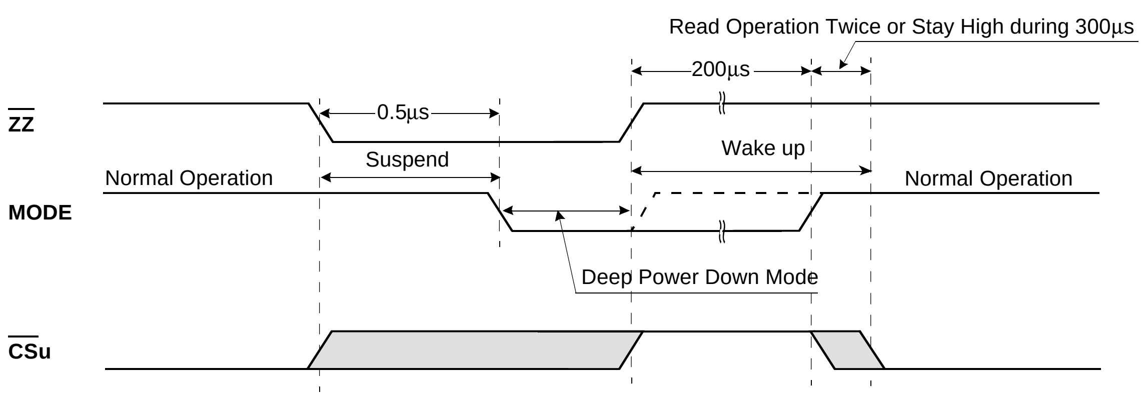
TIMING WAVEFORM OF WRITE CYCLE(3)(UBu, LBu Controlled, ZZ=V_{IH})



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low CSu and low WE. A write begins when CSu goes low and WE goes low with asserting UBu or LBu for single byte operation or simultaneously asserting UBu and LBu for double byte operation. A write ends at the earliest transition when CSu goes high and WE goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CSu going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with CSu or WE going high.

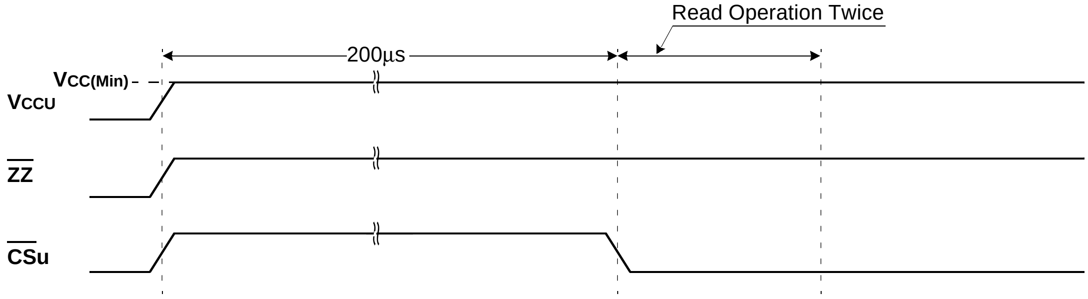
TIMING WAVEFORM OF DEEP POWER DOWN MODE for U*t*RAM



(DEEP POWER DOWN MODE)

1. When you toggle ZZ pin low, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power Up sequence shown in next page.

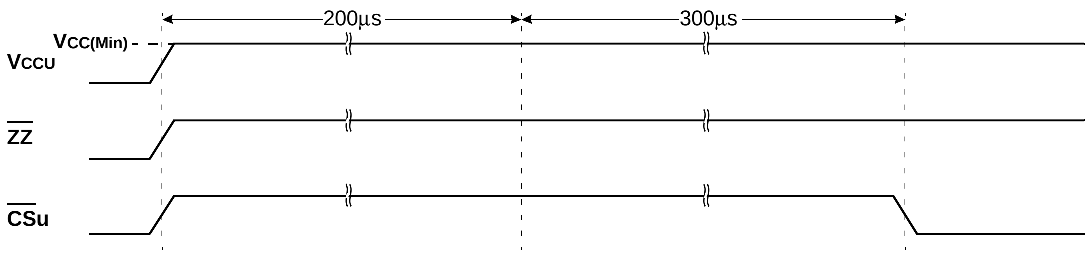
TIMING WAVEFORM OF POWER UP(1) for U*t*RAM



(POWER UP(1))

1. After VCCU reaches VCC(Min.) following power application, wait 200µs with CSu high and then toggle CSu low and commit Read Operation at least twice. Then you get into the normal operation.
2. Read operation should be executed by toggling CSu pin low.
3. The read operation must satisfy the specified tRC.
4. ZZ pin should be kept high during whole power up sequence.

TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle) for U*t*RAM

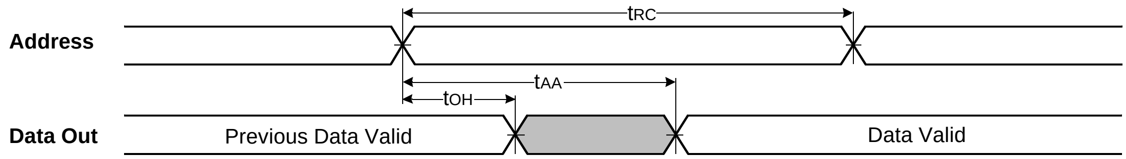


(POWER UP(2))

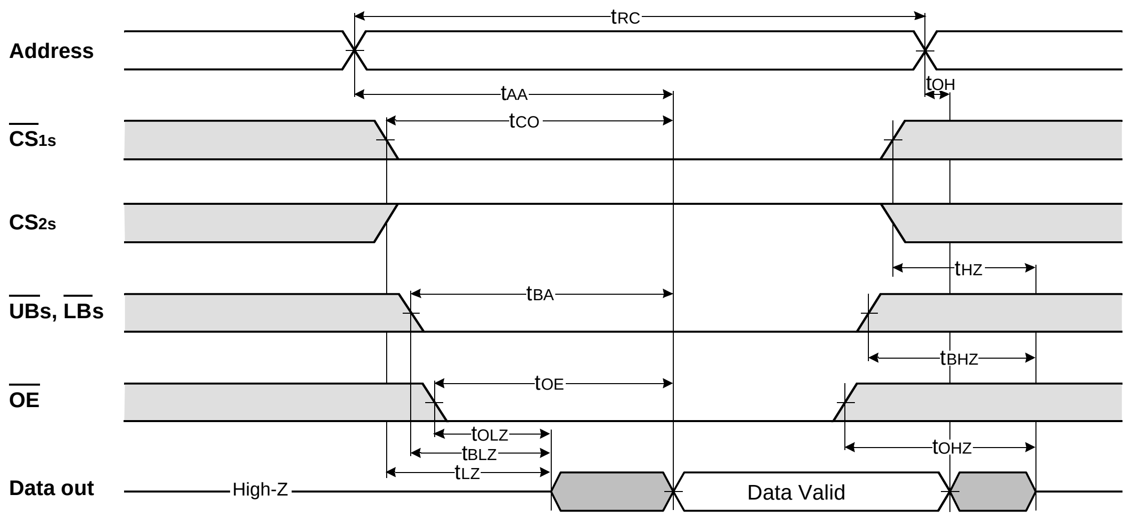
1. After VCCU reaches VCC(Min.) following power application, wait 200µs and wait another 300µs with CSu high if you dont want to commit dummy read cycle. After total 500µs wait, toggle CSu low, then you get into the normal mode.
2. ZZ pin should be kept high during whole power up sequence.

TIMING DIAGRAMS for SRAM

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}_{1s}$=$\overline{OE}$=V_{IL}, CS_{2s}=$\overline{WE}$=V_{IH}, $\overline{UB}$s or/and $\overline{LB}$s=V_{IL})



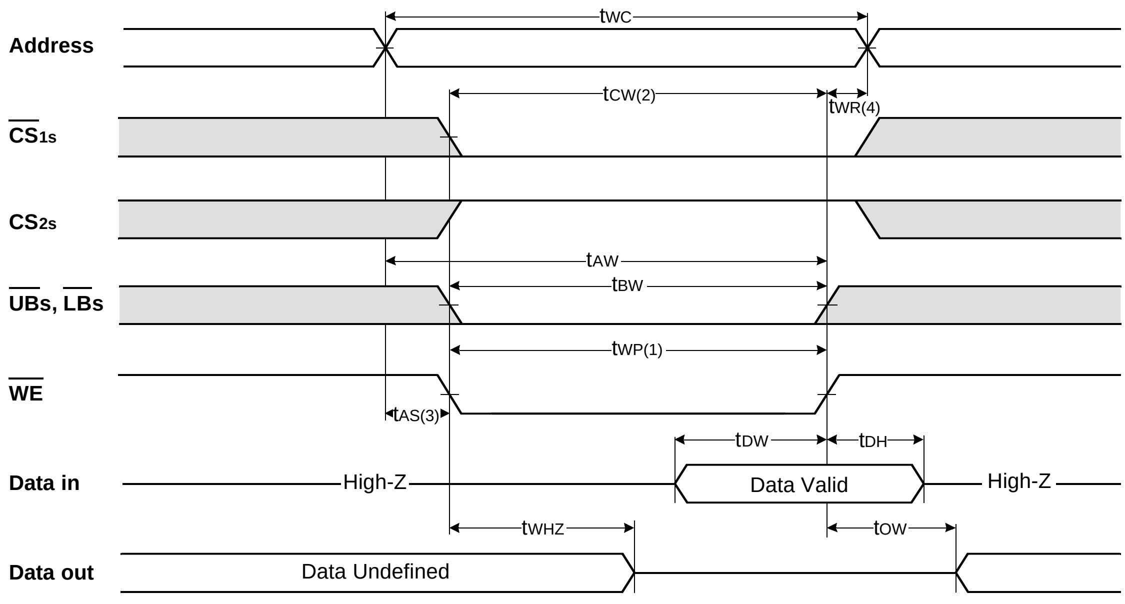
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



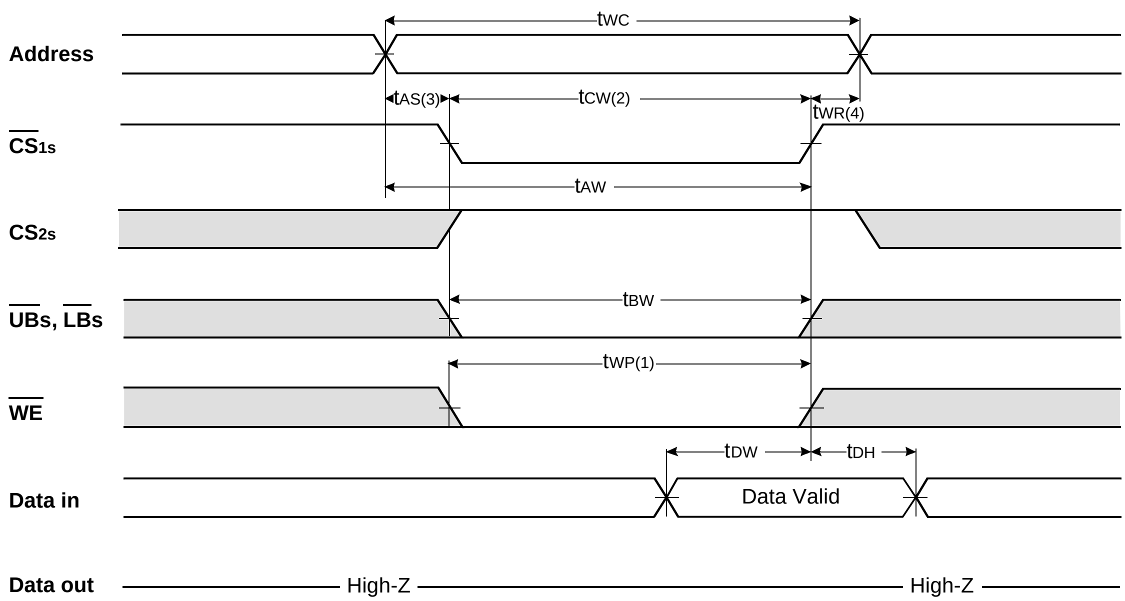
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

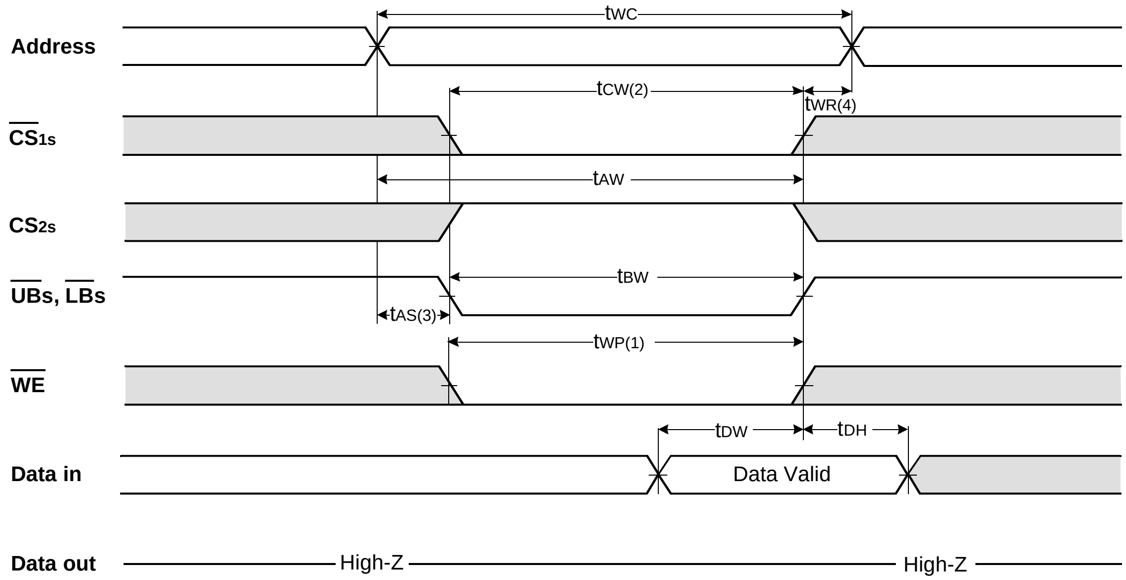
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$1s Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UBs}$, $\overline{LBs}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1s}$ and low $\overline{WE}$. A write begins when $\overline{CS1s}$ goes low and $\overline{WE}$ goes low with asserting UBs or LBs for single byte operation or simultaneously asserting UBs and LBs for double byte operation. A write ends at the earliest transition when $\overline{CS1s}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1s}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS1s}$ or $\overline{WE}$ going high.

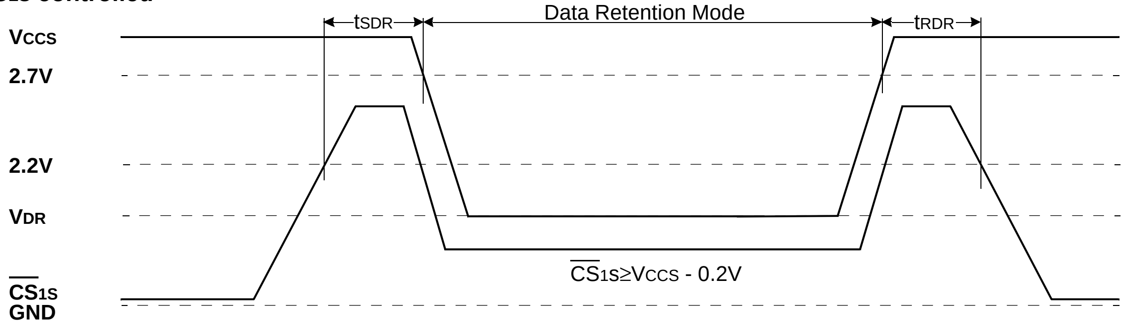
DATA RETENTION CHARACTERISTICS for SRAM

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}_{1S} \geq Vcc-0.2V$[1)], $V_{IN} \geq 0V$	1.5	-	3.1	V
Data retention current	I_{DR}	$Vcc=1.5V$, $\overline{CS}_{1S} \geq Vcc-0.2V$[1)], $V_{IN} \geq 0V$	-	0.5[2)]	6	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		tRC	-	-	

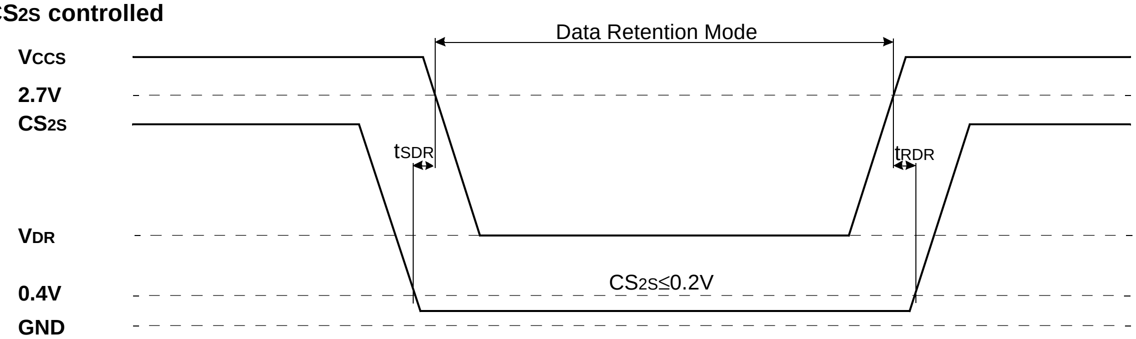
1. 1) $\overline{CS}_{1S} \geq Vcc-0.2V$, $CS_{2S} \geq Vcc-0.2V$($\overline{CS}_{1S}$ controlled) or
   2) $0 \leq CS_{2S} \leq 0.2V$(CS_{2S} controlled)
2. Typical values are measured at $T_A=25°C$ and not 100% tested.

DATA RETENTION WAVE FORM for SRAM

$\overline{CS}_{1S}$ controlled



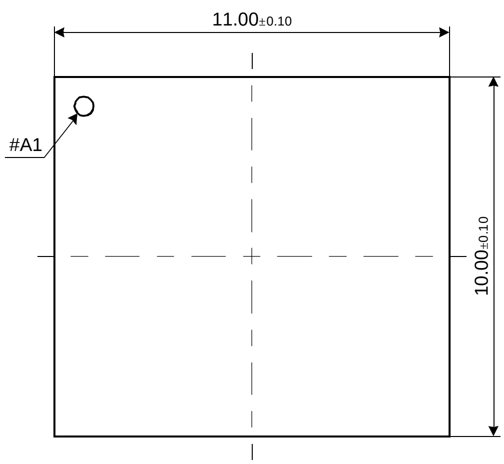
CS_{2S} controlled



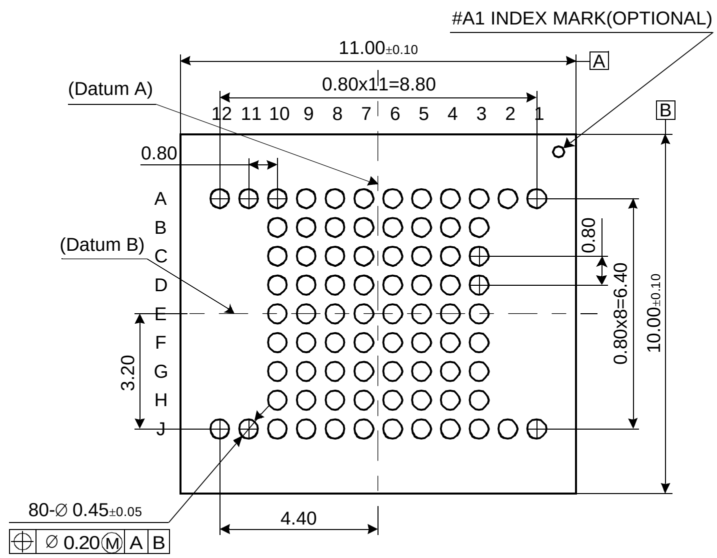
PACKAGE DIMENSION

80-Ball Tape Ball Grid Array Package (measured in millimeters)

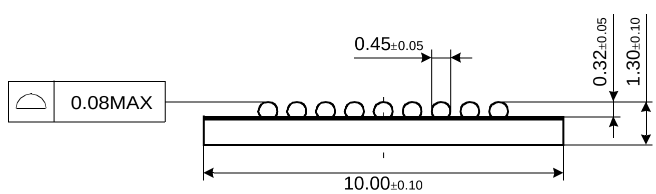
Top View



Bottom View



Side View



TECHNICAL NOTE

UtRAM USAGE AND TIMING

INTRODUCTION

UtRAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the UtRAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

START WITH A DRAM TECHNOLOGY

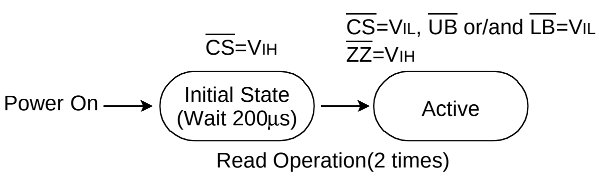
The key point of UtRAM is its high speed and low power. This high speed comes from the use of many small blocks such as 32Kbits each to create UtRAM arrays. The small blocks have short word lines thus with little capacitance eliminating a major factor of operating current dissipation in conventional DRAM blocks.

Each independent macro-cell on a UtRAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. UtRAM performs a complete read operation in every tRC, but UtRAM needs power up sequence like DRAM.

Power Up Sequence and Diagram

1. Apply power.
2. Maintain stable power for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least 2 times.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The UtRAM was designed to work just like an SRAM - without any waits or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations inside with advanced design technology - those are not to be seen from outside. Precharging takes place during every access, overlapped between the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult. Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides an internal refresh controller for devices. When all accesses within refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM is sometimes used on these applications, which requires a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG's unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the UtRAM never need to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

AVOID TIMING

Following figures show you an abnormal timing which is not supported on UtRAM and its solution.

If your system has a timing which sustains invalid states over 4µs at read mode like Figure 1, there are some guide lines for proper operation of UtRAM.

When your system has multiple invalid address signals shorter than tRC on the timing shown in Figure 1, UtRAM needs a normal read timing(tRC) during that cycle(Figure 2) or needs to toggle $\overline{CS}$ once to 'high' for about tRC(Figure 3).

Figure 1.

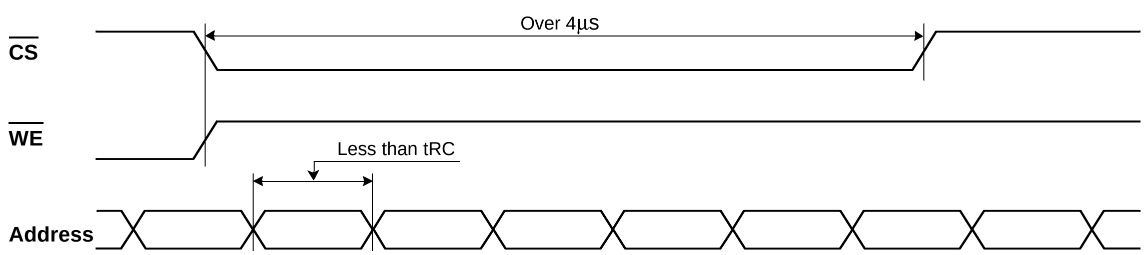


Figure 2.

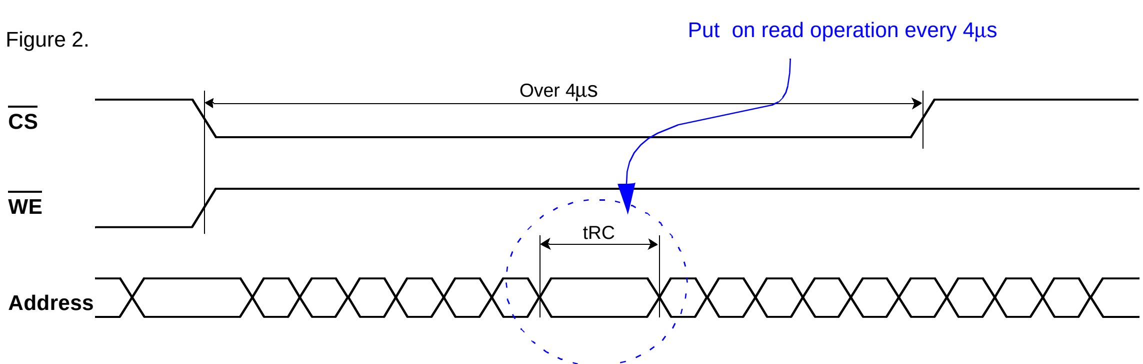
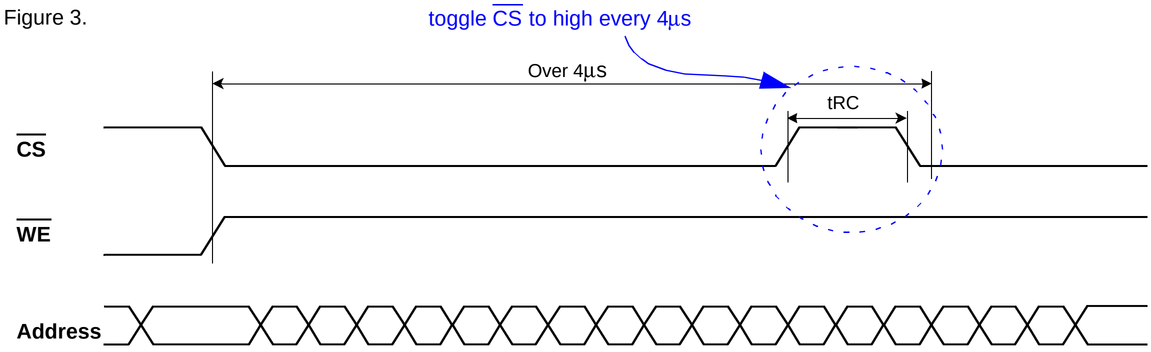


Figure 3.



Write operation has similar restriction to Read operation. If your system has a timing which sustains invalid states over 4µs at write mode and has continuous write signals with length of Min. tWC over 4µs like Figure 4, you must toggle WE once to high and make it stay high at least for tRC every 4µs or toggle CS once to high for about tRC.

Figure 4.

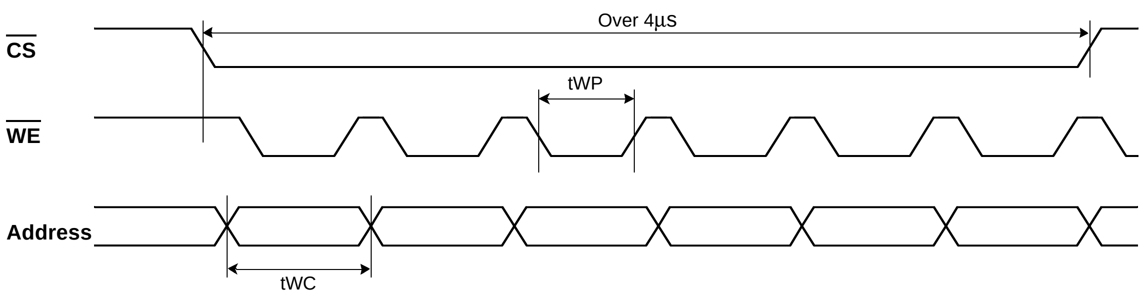


Figure 5.

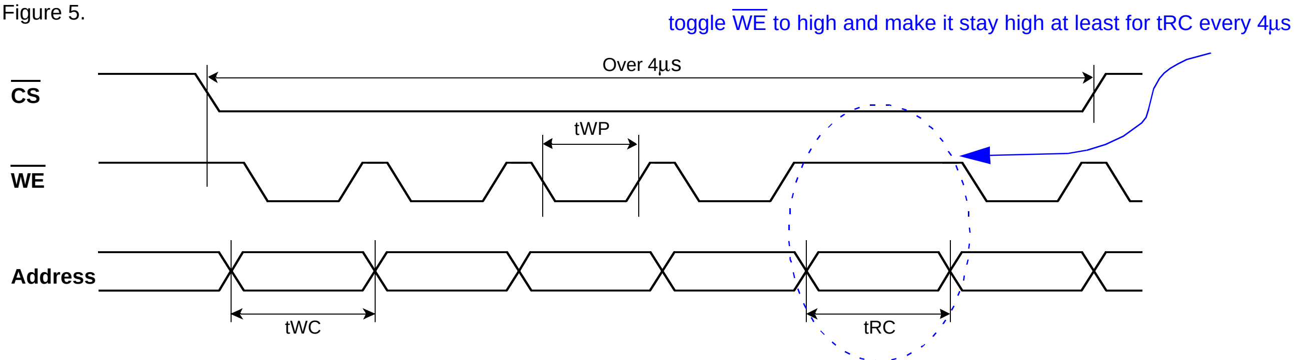


Figure 6.