512Mb M-die DDR-II SDRAM Specification

Version 0.11

Contents

Revision History

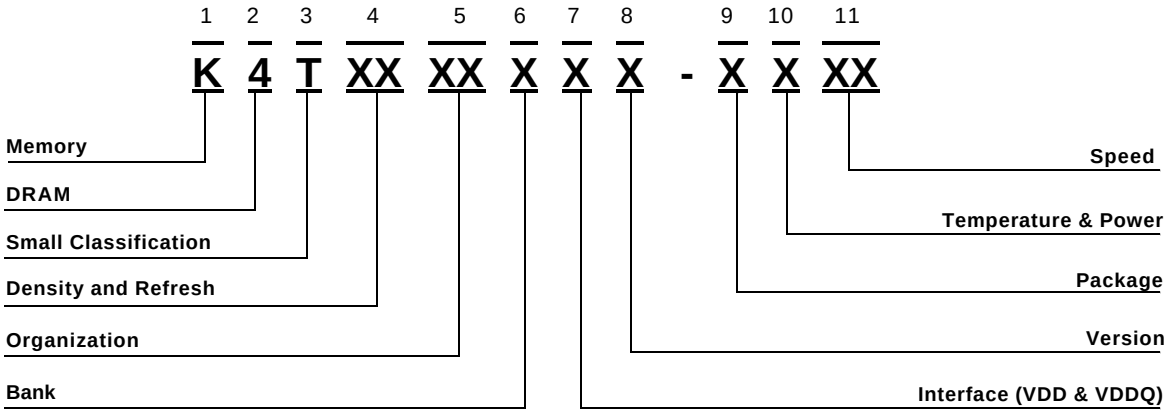
Version 0.0 (Feb, 2002)
- Initial Release

Version 0.1 (Mar, 2002)
- Corrected the typo
- Add FBGA package dimension
- Delete SS800 AC parameter table
- Changed the CAS Latency & Additive Latency
  CAS Latency : removed CL=2(Optional) and changed CL=5(Optional) to CL=5 & Added CL=6(Optional)
  Additive Latency : Changed AL=4(Optional) to AL=4 & Added AL=5
- Delete tHZ min
- tIH/tIS for DDR533 : min 500ps(from TBD)
- tRRD : differentiate 1KB & 2KB page size as 7.5ns & 10ns each
- tWTR : Changed to analog value(400Mbps : 10ns, 533Mbps + : 7.5ns)

Version 0.11 (April, 2002)
- Corrected the typo
- Changed Additive Latency definition as below
  Old : AL=0(Default), 1,2,3,4 and 5
  New : AL=0,1,2,3 and 4
- Added Comment of Max. Package dimension
  Maximum Package Height : 21mm
  Maximum Package Center to Center spacing : 12.8mm

General Information

Organization	DDR400 w/ CL=4	DDR400 w/ CL=3	DDR533 w/ CL=5	DDR533 w/ CL=4
128Mx4	K4T51043QM-GCD4	K4T51043QM-GCC4	K4T51043QM-GCE5	K4T51043QM-GCD5
	K4T51043QM-GLD4	K4T51043QM-GLC4	K4T51043QM-GLE5	K4T51043QM-GLD5
64Mx8	K4T51083QM-GCD4	K4T51083QM-GCC4	K4T51083QM-GCE5	K4T51083QM-GCD5
	K4T51083QM-GLD4	K4T51083QM-GLC4	K4T51083QM-GLE5	K4T51083QM-GLD5
32Mx16	K4T51163QM-GCD4	K4T51163QM-GCC4	K4T51163QM-GCE5	K4T51163QM-GCD5
	K4T51163QM-GLD4	K4T51163QM-GLC4	K4T51163QM-GLE5	K4T51163QM-GLD5



1. SAMSUNG Memory : K

2. DRAM : 4

3. Small Classification

T : DDR-II SDRAM

4. Density & Refresh

51 : 512M 8K/64ms

5. Organization

04 : x4
08 : x8
16 : x16

6. Bank

3 : 4 Bank

7. Interface (VDD & VDDQ)

Q: SSTL-18(1.8V, 1.8V)

8. Version

M : 1st Generation
A : 2nd Generation
B : 3rd Generation
C : 4th Generation
D : 5th Generation
E : 6th Generation

9. Package

G : FBGA

10. Temperature & Power

C : (Commercial, Normal)
L : (Commercial, Low)

11. Speed

C4 : 5ns@CL3
D4 : 5ns@CL4
E4 : 5ns@CL5

C5 : 3.75ns@CL3
D5 : 3.75ns@CL4
E5 : 3.75ns@CL5

D6 : 3ns@CL4
E6 : 3ns@CL5
F6 : 3ns@CL6

1.Key Features

		DDR400 CL=4	DDR400 CL=3	DDR533 CL=5	DDR533 CL=4	Units
f_{CK}	Clock Frequency	200	200	267	267	MHz
	Data Rate	400	400	533	533	Mb/s/pin

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8V ± 0.1V
- 200 MHz f_{CK} for 400Mb/sec/pin & 267MHz f_{CK} for 533Mb/sec/pin
- 4 Bank
- Posted CAS
- Programmable CAS Latency: 3, 4, 5 and 6(Optional)
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 (Read/Write Interrupt Prohibited but only Read interrupted by Read & Write interrupted by Write are allowed), 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Data-Strobes: Bidirectional, (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- Auto Refresh (CBR) and Self Refresh
  Refesh Period 7.8us (8192 refresh cycles/64ms)
- Package: 60ball FBGA - 128Mx4/64Mx8 , 84ball FBGA - 32Mx16

Description

The 512Mb Double-Data-Rate-II (DDR-II) SDRAMs are high-speed CMOS 512Mb Double Data Rate II Synchronous DRAM devices. The 512Mb chip is organized as either 32Mbit x 4 I/O x 4 banks or 16Mbit x 8 I/O x 4banks or 8Mbit x 16I/O x 4 banks device. This synchronous device achieve high speed double-data-rate transfer rates of up to 533Mb/sec/pin (DDR533) for general applications.

The chip is designed to comply with the following key DDR-II DRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) Off-Chip Driver(OCD) impedance adjustment, (4) On Die Termination.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with DQS in a source synchronous fashion. A fourteen bit address bus is used to convey row, column, and bank address information in a $\overline{RAS}$/$\overline{CAS}$ multiplexing style. For example, 512Mb(x4) device receive 14/11/2 addressing.

The 512Mb DDR-II devices operate with a single 1.8V±0.1V power supply and 1.8V ± 0.1V VDDQ.

The 512Mb DDR-II devices are available in 60ball FBGAs(x4/8) and available in 84ball FBGAs(x16). Auto Refresh (CBR) and Self Refresh operations of 8192refresh cycles per 64ms are supported. (Refresh Period 7.8us)

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

2. Package Pinout & Addressing

2.1 Package Pinout

x4 package pinout (Top View) : 60ball FBGA Package

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{DQS}$	VDDQ
NC	VSSQ	DM	B	DQS	VSSQ	NC
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
NC	VSSQ	DQ3	D	DQ2	VSSQ	NC
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	$\overline{WE}$	F	$\overline{RAS}$	$\overline{CK}$	ODT
BA2	BA0	BA1	G	$\overline{CAS}$	$\overline{CS}$	
	A10	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

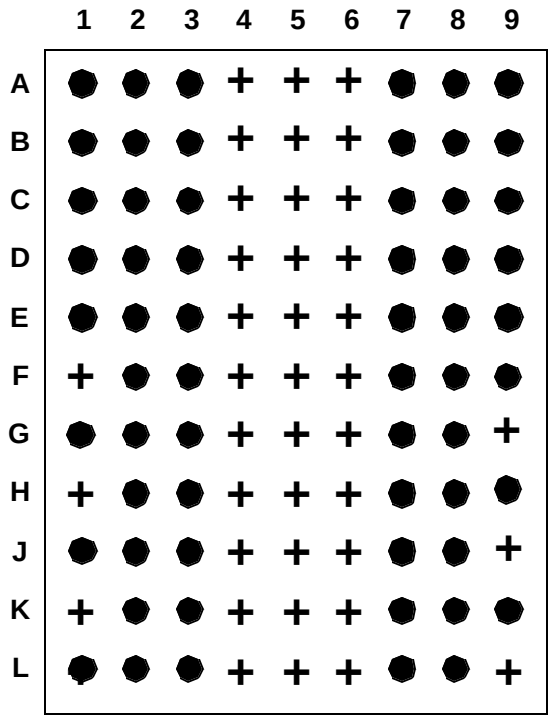
Notes:
B1, B9, D1, D9 = NC for x4 organization.
Pins B3 has identical capacitance as pins B7.
VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Ball Locations (x4)

● : Populated Ball

+ : Depopulated Ball

Top View (See the balls through the Package)



x8 package pinout (Top View) : 60ball FBGA Package

1	2	3		7	8	9
VDD	NU/ RDQS	VSS	A	VSSQ	$\overline{DQS}$	VDDQ
DQ6	VSSQ	DM/ RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	$\overline{WE}$	F	$\overline{RAS}$	$\overline{CK}$	ODT
BA2	BA0	BA1	G	$\overline{CAS}$	$\overline{CS}$	
	A10	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

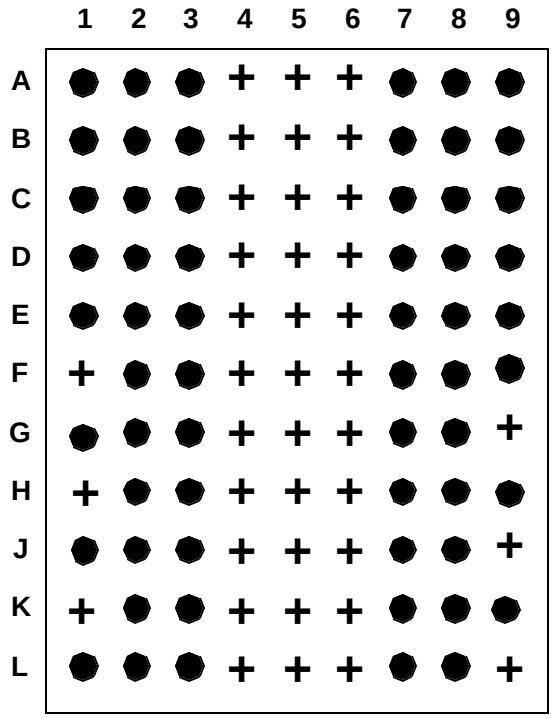
Notes:
Pins B3 and A2 have identical capacitance as pins B7 and A8.
For a read, when enabled, strobe pair RDQS & $\overline{RDQS}$ are identical in function and timing to strobe pair DQS & $\overline{DQS}$.
The function of DM or RDQS/$\overline{RDQS}$ are enabled by EMRS command.
VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Ball Locations (x8)

● : Populated Ball

+ : Depopulated Ball

Top View (See the balls through the Package)



x16 package pinout (Top View) : 84ball FBGA Package

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
UDQ6	VSSQ	UDM	B	UDQS	VSSQ	UDQ7
VDDQ	UDQ1	VDDQ	C	VDDQ	UDQ0	VDDQ
UDQ4	VSSQ	UDQ3	D	UDQ2	VSSQ	UDQ5
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
LDQ6	VSSQ	LDM	F	LDQS	VSSQ	LDQ7
VDDQ	LDQ1	VDDQ	G	VDDQ	LDQ0	VDDQ
LDQ4	VSSQ	LDQ3	H	LDQ2	VSSQ	LDQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

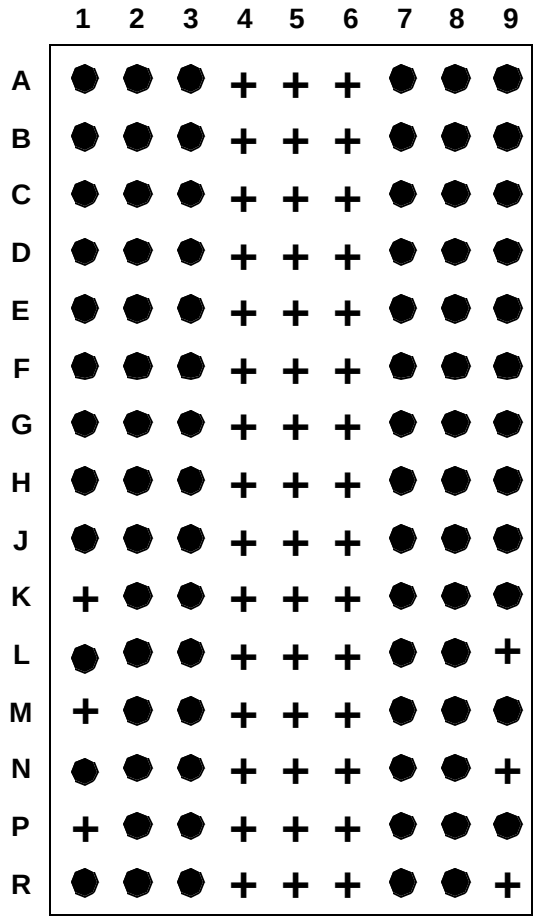
Notes:
VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Ball Locations (x16)

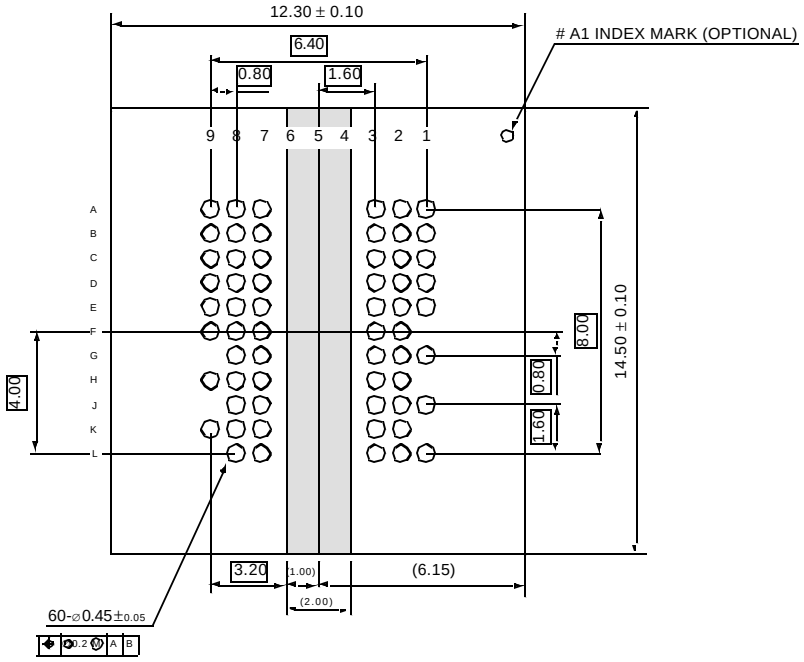
● : Populated Ball

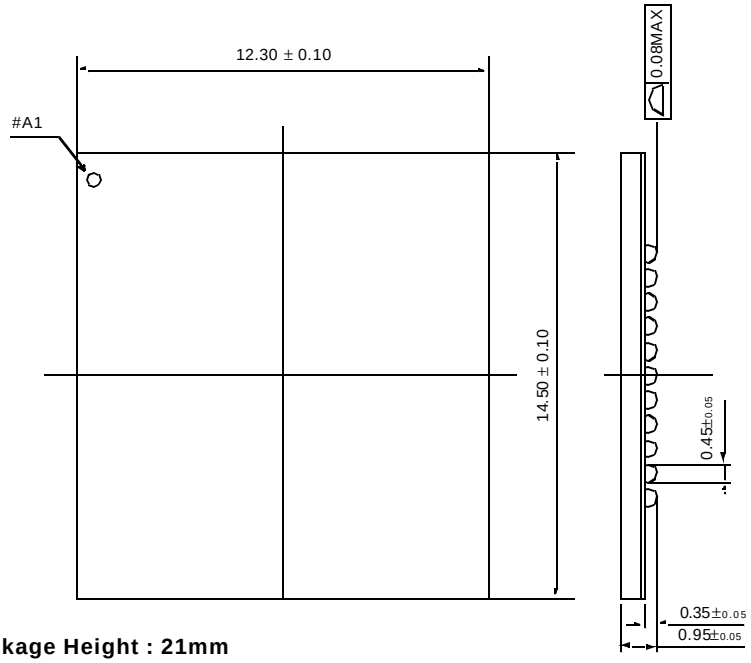
+ : Depopulated Ball

Top View (See the balls through the Package)



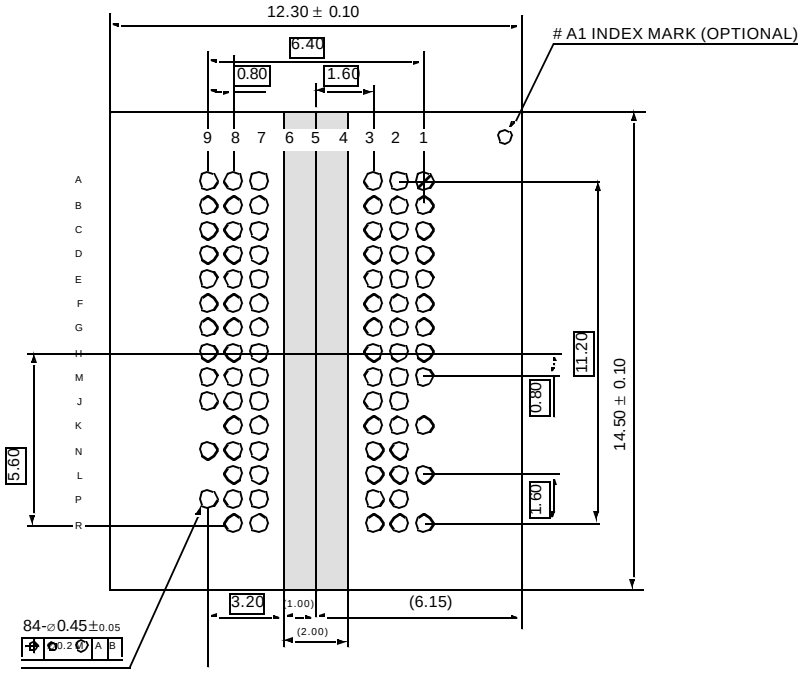
FBGA Package Dimension(x4/x8)

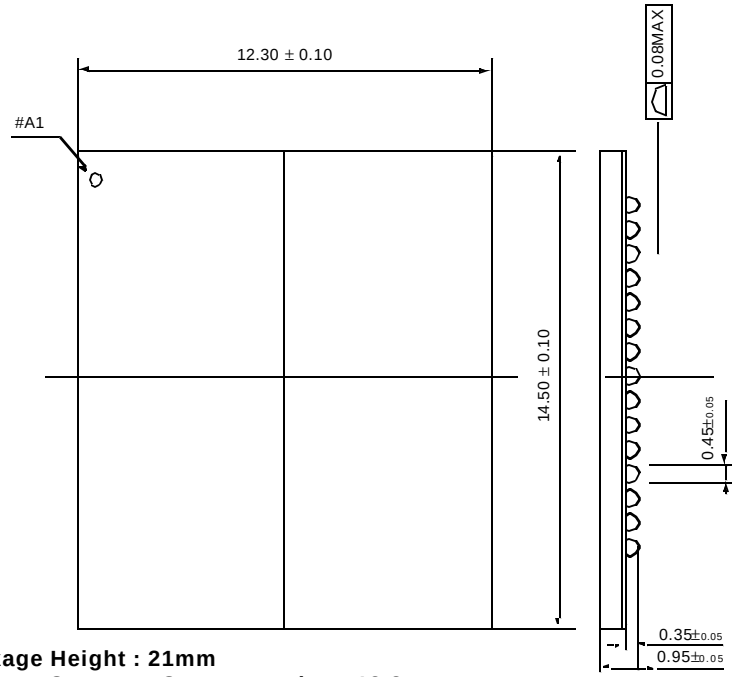




Maximum Package Height : 21mm
Maximum Package Center to Center spacing : 12.8mm

FBGA Package Dimension(x16)





Maximum Package Height : 21mm
Maximum Package Center to Center spacing : 12.8mm

2.2 Input/Output Functional Description

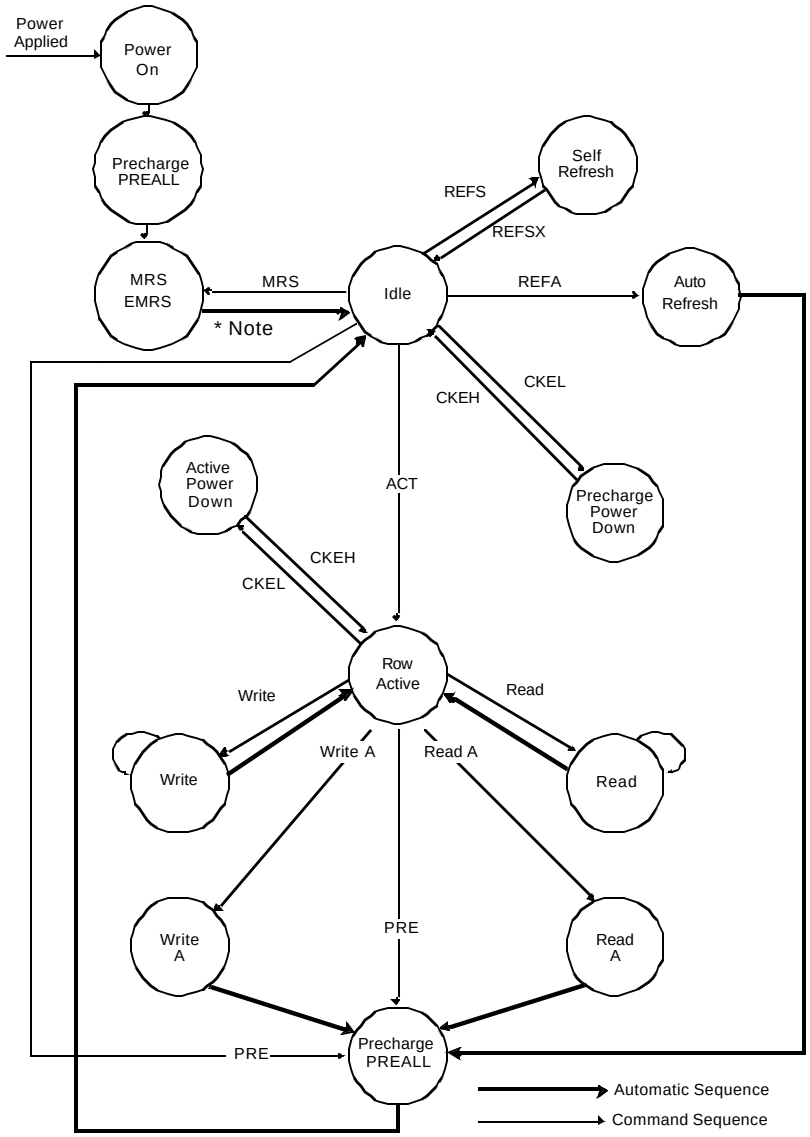
Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A13	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data for source synchronous operation. Edge-aligned with read data, centered in write data. Used to capture write data. Differential strobe is optional feature
RDQS, ($\overline{RDQS}$)	Output	**Data Strobe for Read:** Edge-aligned with read data, for the x8, an RDQS/$\overline{RDQS}$ can be enabled via EMRS to simplify read timing
ODT	Input	**On Die Termination :** Active Termination Control: ODT (registered HIGH) enables active termination resistance internal to the DDR II SDRAM. When enabled, active termination is only applied to DQ, DQS, DQS#, RDQS, RDQS#, and DM.
NC		**No Connect:** No internal electrical connection is present.
NU		No Usage
RFU		Reserved for Future Use
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage:** min. 0.49*V_{DDQ} , typ. 0.5*V_{DDQ} , max.. 0.51*V_{DDQ}

2.3 DDR-II Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A_{10}/AP	A_{10}/AP	A_{10}/AP
Row Address	A_0 ~ A_{13}	A_0 ~ A_{13}	A_0 ~ A_{12}
Column Address	A_0 ~ A_9,A_{11}	A_0 ~ A_9	A_0 ~ A_9

3 Functional Description

3.1 Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

*Note : Except Align drive(1)/drive(0) states activated by EMRS, Align mode should be deactivated by EMRS to move to an idle state.
Read interrupted by Read & Write Interrupted by Write are acceptable only @ Burst length 4 boundary

3.2 Basic Functionality

Read and write accesses to the DDR-II SDRAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR-II SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

3.2.1 Power On and Initialization

DDR-II SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

No Power sequencing is specified during power up or power down given the following criteria.

- VDD and VDDQ are driven from a single power converter output, and
- VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation), and
- VREF < VDDQ + 0.3V, and
- A minimum resistance of 42ohms(22ohms series resistor + 22ohm parallel resistor - 5% tolerance)

If the above criteria cannot be met by the system design, then the following table must be adheres to during power up:

Voltage Description	Sequencing	Voltage Relationship to avoid latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

The DQ and DQS outputs are in the High-Z state, where they remain until driven active in normal operation (by a read access). After all power supply, reference voltages, and the clocks are stable, the DDR-II SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought HIGH. Following the NOP command, a Precharge ALL command must be applied. Next a Mode Register Set command must be issued for the Extended Mode Register, to enable the DLL. Then a Mode Register Set command must be issued for the Mode Register, to reset the DLL and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. A Precharge ALL command should be applied, placing the device in the “all banks idle” state.

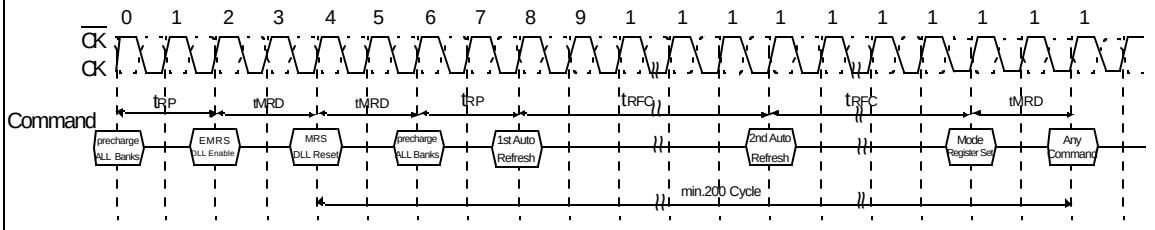
Once in the idle state, two Auto Refresh cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR-II SDRAM is ready for normal operation. Failure to follow these steps may lead to unpredictable start-up modes.

Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE at a low state(all other inputs may be undefined.)
   - Apply VDD before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock(CK, $\overline{CK}$), apply NOP & take CKE high.
4. Issue precharge commands for all banks of the device.
5. Issue EMRS to enable DLL.(To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL.
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command with low to A8 to initialize device operation.

Power up & Initialization Sequence



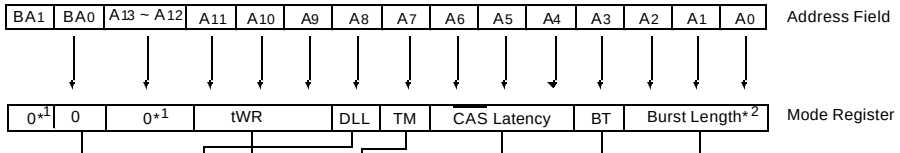
3.2.2 Programming the Mode Register

For application flexibility, burst type, burst length, $\overline{CAS}$ latency, DLL reset function are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive CAS latency, ODT(On Die Termination) and Off-Chip Driver impedance adjustment are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the MRS and EMRS can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

After initial power up, the both MRS and EMRS Commands must be issued before read or write cycles may begin. All four banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Either MRS or EMRS Commands are activated by the low signals of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ at the positive edge of the clock. When the bank address 0 (BA0) is low, the DDR-II SDRAM enables the MRS command. When the bank address 0 (BA0) is high, the DDR-II SDRAM enables the EMRS command. The address input data during this cycle defines the parameters to be set as shown in the MRS and EMRS table. A new command may be issued after the mode register set command cycle time (tMRD). MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

3.2.2.1 DDR-II SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR-II SDRAM. It controls CAS latency, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR-II SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0, while controlling the state of address pins A0 ~ A13. The DDR-II SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, and, $\overline{CAS}$ latency is defined by A4 ~ A6. The DDR-II doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes. A9~A11 are used for tWR definition.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

BA0	MRS mode
0	MRS
1	EMRS

tWR

A11	A10	A9	tWR
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

$\overline{CAS}$ Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6(Optional)
1	1	1	Reserved

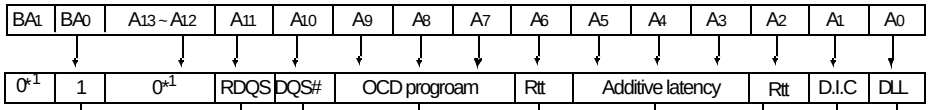
*1 : BA1 and A12~A13 are reserved for future use and must be programmed to 0 when setting the mode register.

3.2.2.2 DDR-II SDRAM Extended Mode Register Set (EMRS)

The extended mode register stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0, while controlling the states of address pins A0 ~ A13. The DDR-II SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength data-output driver. A3~A5 determines the additive latency, A2 and A6 are used for ODT value selection, A7~A9 are used for OCD control, A10 is used for DQS# disable and A11 is used for RDQS enable.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.



A11	RDQS Enable
0	Disable
1	Enable

A10	DQS# Enable
0	Enable
1	Disable

A0	DLL Enable
0	Enable
1	Disable

A6	A2	Rtt (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	TBD

BA0	MRS mode
0	MRS
1	EMRS

Additive Latency

A5	A4	A3	Latency
0	0	0	0 (Default)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Driver Impedance Adjustment

A9	A8	A7	
0	0	0	OCD Calibration mode exit
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode
1	1	1	OCD Calibration default

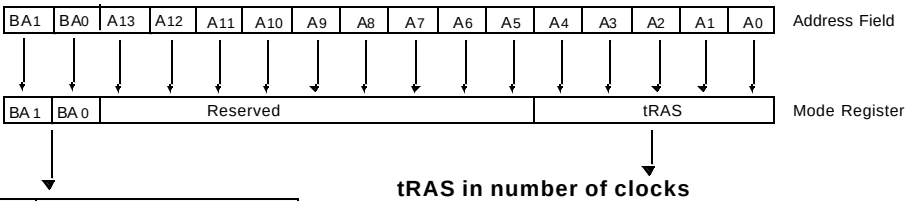
* Refer to the following 2.2.2.3 for detailed information

Driver Impedance Adjustment

A1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

*1 : A12~A13 are reserved for future use and must be programmed to 0 when setting the mode register.
BA1 is used for tRAS Programming on to EMRS(3)

tRAS programming on to EMRS(3)



BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3)

tRAS in number of clocks

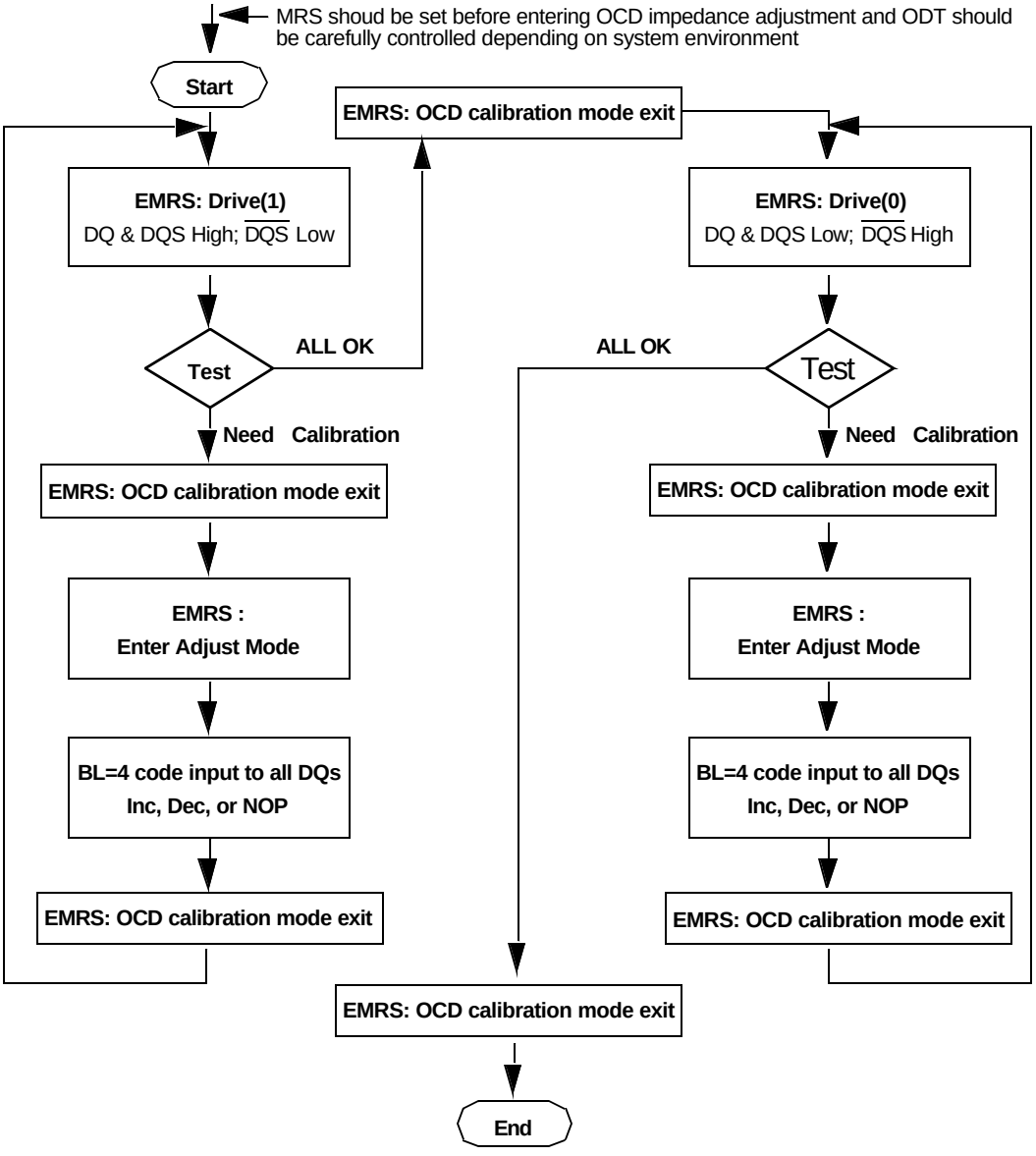
A4	A3	A2	A1	A0	tRAS
0	0	0	0	0	Reserved
0	0	0	0	1	Reserved
0	0	0	1	0	Reserved
0	0	0	1	1	Reserved
0	0	1	0	0	4*tCK
0	0	1	0	1	5*tCK
0	0	1	1	0	6*tCK
0	0	1	1	1	7*tCK
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	0	1	29*tCK
1	1	1	1	0	30*tCK
1	1	1	1	1	31*tCK

tRAS value is defined in AC spec table, and required number of clocks is calculated from it. Users should write tRAS field of EMRS(3) for proper operation.

*A5~A13 are reserved for future use and must be programmed to 0 when setting the mode register.

3.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR-II SDRAM supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR-II SDRAM and drive of RDQS is depedent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics follow approximate nominal V/I curve for 18ohm output drivers, but are not guaranteed. If tighter control is required, which is controlled within 18ohm +/- 3ohm driver impedance range, OCD must be used.

Off- Chip-Driver program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

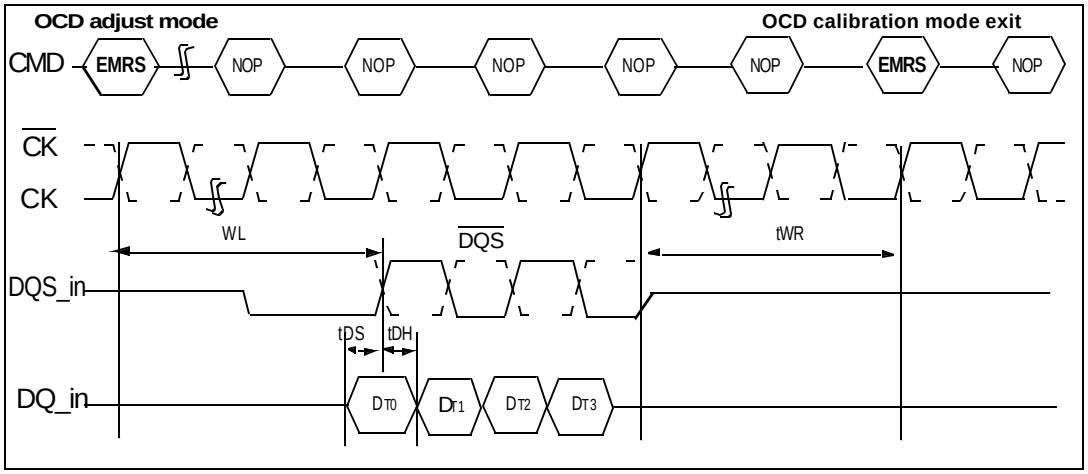
OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR-II SDRAM as in table X. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table X means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DR-II SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR-II SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range.

Off- Chip-Driver Program

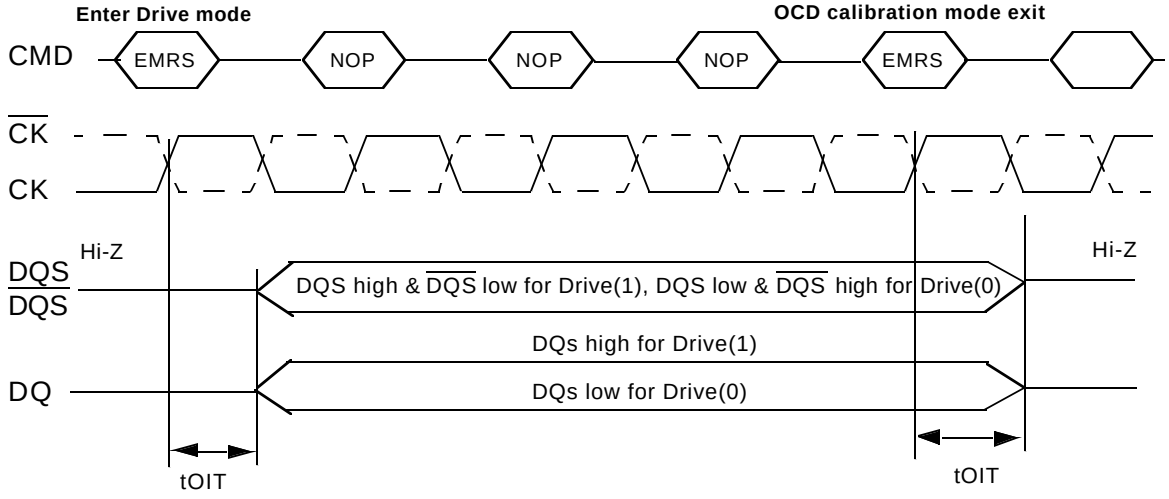
4bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as the following timing diagram. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by MRS addressing mode (ie. sequential or interleave).



Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR-II SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the following timing diagram.



3.2.2.4 ODT (On Die Termination)

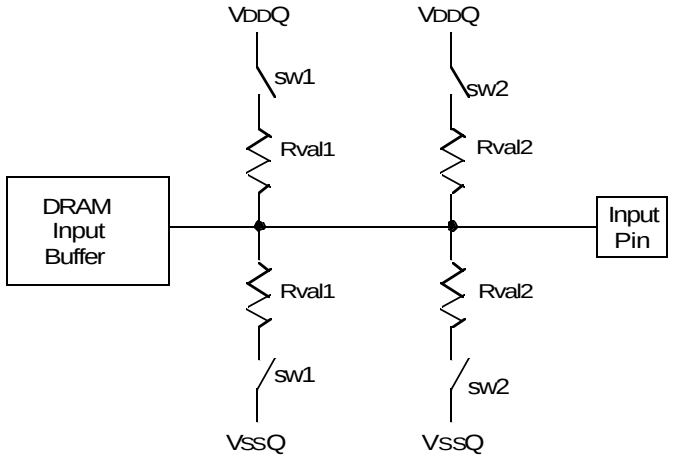
On Die Termination (ODT), is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS#, RDQS/RDQS#, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS#, LDQS/LDQS#, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

This proposal outlines DDR II SDRAM ODT definition and functionality for ACTIVE and STANDBY modes. The ODT function is turned off and not supported in SELF REFRESH mode.

FUNCTIONAL DESCRIPTION

BALL LOCATION	SYMBOL	TYPE	DESCRIPTION
F9 : x4/x8 K9 : x16	ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR II SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS#, RDQS, RDQS#, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS#, LDQS/LDQS#, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.

FUNCTIONAL REPRESENTATION OF ODT



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, DQS#, RDQS, and RDQS# pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt mismatch tolerance between any pull-up/pull-down pair	Rtt(mis)	-3.75		+3.75	%	1

TEST CONDITION FOR Rtt MEASUREMENTS (Note1)

Measurement Definition for Rtt(eff)

Apply VIHac and VILac to test pin separately, then measure current I(VIHac) and I(VILac) respectively.

$$Rtt(eff) = \frac{VIHac - VILac}{I(VIHac) - I(VILac)}$$

Measurement Definition for Rtt(mis)

Measure voltage (V_M) at test pin (midpoint) with no load.

$$\Delta Rtt(mis) = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

Note1: VIHac, VILac, and VDDQ values defined in SSTL_18 (JC-16 item #103).

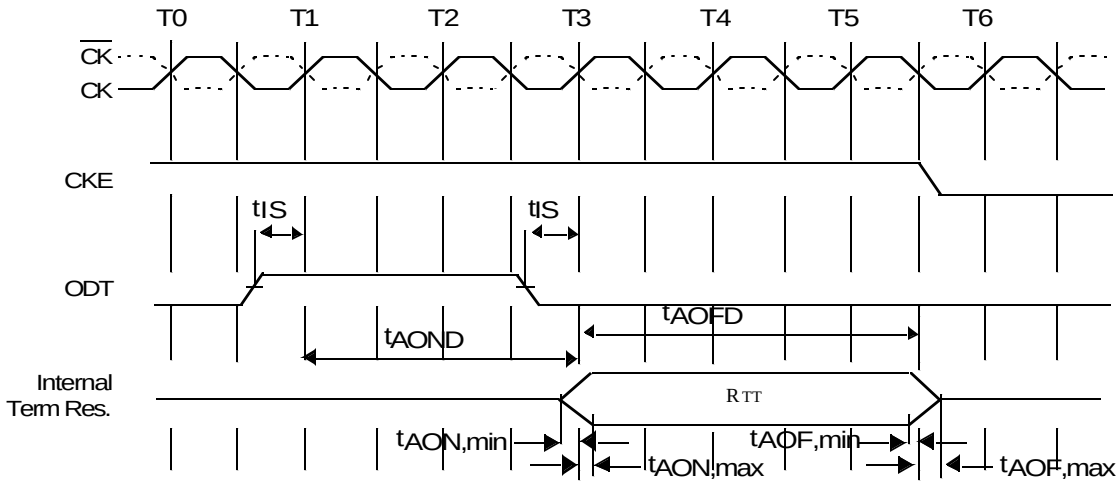
AC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
ODT turn-on delay	^{t}AOND	2	2	tCK	
ODT turn-on	^{t}AON	tAC(min)	tAC(max)+1.0ns	ns	1
ODT turn-on(Power-Down mode)	^{t}AONPD	tAC(min)+2ns	2*tCK+tAC(max)+1.0ns	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	tCK	
ODT turn-off	^{t}AOF	tAC(min)	tAC(max)+0.6ns	ns	2
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+2ns	2.5*tCK+tAC(max)+1.0ns	ns	

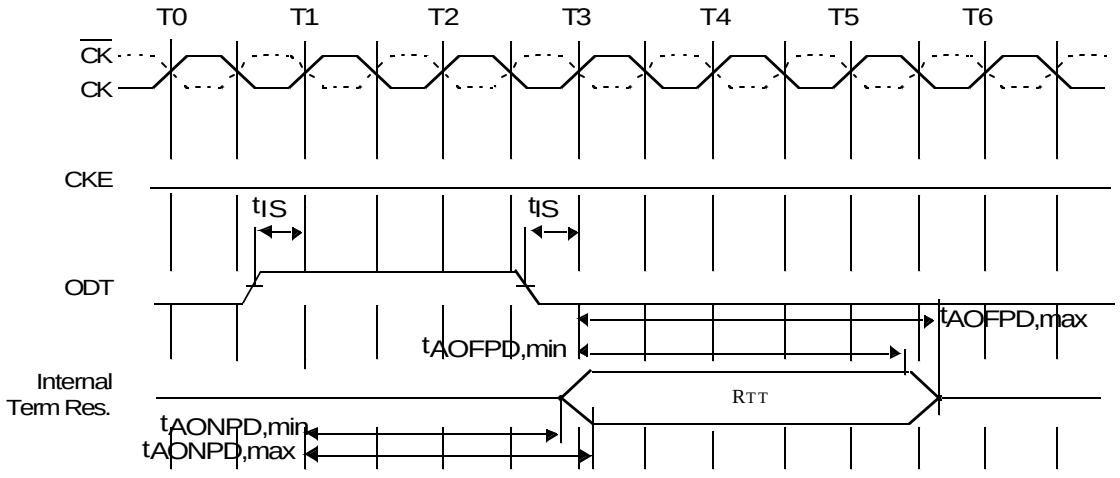
Note 1 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

Note 2 ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

ODT TIMING FOR ACTIVE/STANDBY MODE.



ODT TIMING FOR POWERDOWN MODE



The following reference material is based on a typical 2 slot RDIMM system. Each RDIMM module may have up to 2 Ranks of memory.

TABLE 1. Termination Matrix for Writes to DRAM

Configuration	Write To	Target DQ ODT Resistance RTT				
		Controller	Module in Slot 1		Module in Slot2	
			Rank 1	Rank 2	Rank 1	Rank 2
2R/2R	Slot 1	infinite	infinite	infinite	75 ohm	infinite (note1)
	Slot 2	infinite	75 ohm	infinite (note1)	infinite	infinite
2R/1R	Slot 1	infinite	infinite	infinite	75 ohm	unpopulated
	Slot 2	infinite	75 ohm	infinite (note1)	infinite	unpopulated
1R/2R	Slot 1	infinite	infinite	unpopulated	75 ohm	infinite (note1)
	Slot 2	infinite	75 ohm	unpopulated	infinite	infinite
1R/1R	Slot 1	infinite	infinite	unpopulated	75 ohm	unpopulated
	Slot 2	infinite	75 ohm	unpopulated	infinite	unpopulated
2R/Empty	Slot 1	infinite	150 ohm	infinite	unpopulated	unpopulated
Empty/2R	Slot 2	infinite	unpopulated	unpopulated	150 ohm	infinite
1R/Empty	Slot 1	infinite	150ohm	unpopulated	unpopulated	unpopulated
Empty/1R	Slot 2	infinite	unpopulated	unpopulated	150 ohm	unpopulated

note 1: Alternatively, the controller may use rank2 for termination instead of rank1.

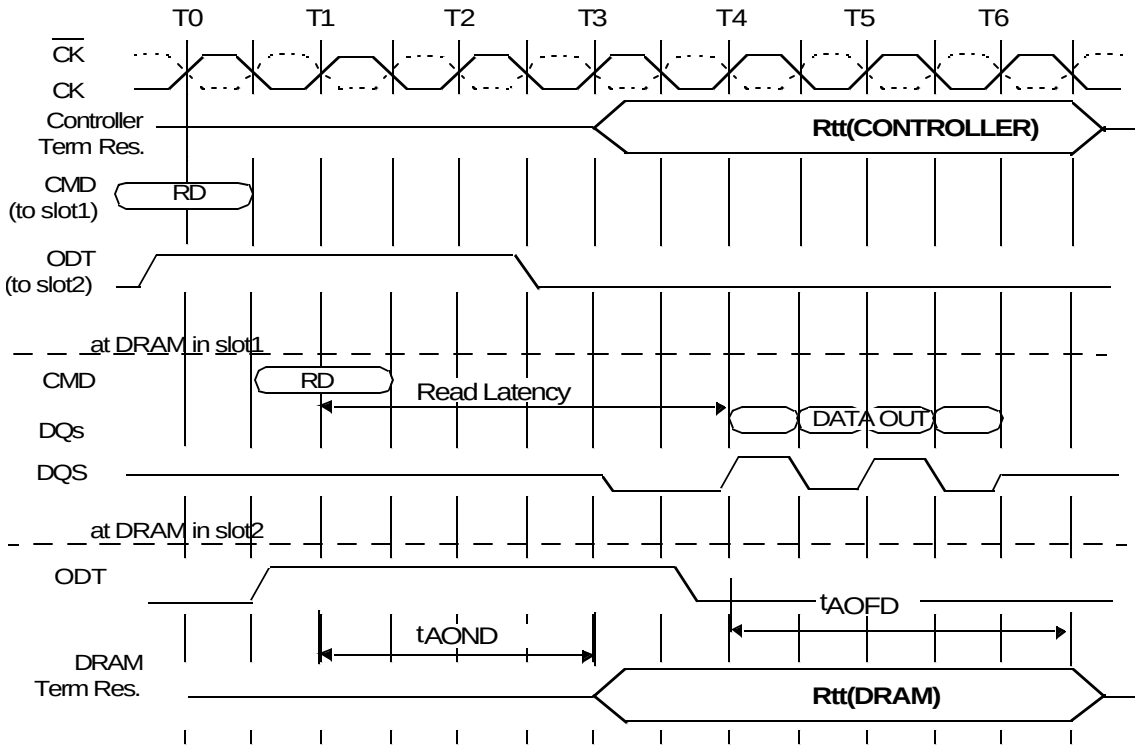
TABLE 2. Termination Matrix for Reads from DRAM

Configuration	Read From	Target DQ ODT Resistance RTT				
		Controller	Module in Slot 1		Module in Slot2	
			Rank 1	Rank 2	Rank 1	Rank 2
2R/2R	Slot 1	150 ohm	infinite	infinite	75 ohm	infinite (note1)
	Slot 2	150 ohm	75 ohm	infinite (note1)	infinite	infinite
2R/1R	Slot 1	150 ohm	infinite	infinite	75 ohm	unpopulated
	Slot 2	150 ohm	75 ohm	infinite (note1)	infinite	unpopulated
1R/2R	Slot 1	150 ohm	infinite	unpopulated	75 ohm	infinite (note1)
	Slot 2	150 ohm	75 ohm	unpopulated	infinite	infinite
1R/1R	Slot 1	150 ohm	infinite	unpopulated	75 ohm	unpopulated
	Slot 2	150 ohm	75 ohm	unpopulated	infinite	unpopulated
2R/Empty	Slot 1	75 ohm	infinite	infinite	unpopulated	unpopulated
Empty/2R	Slot 2	75 ohm	unpopulated	unpopulated	infinite	infinite
1R/Empty	Slot 1	75 ohm	infinite	unpopulated	unpopulated	unpopulated
Empty/1R	Slot 2	75 ohm	unpopulated	unpopulated	infinite	unpopulated

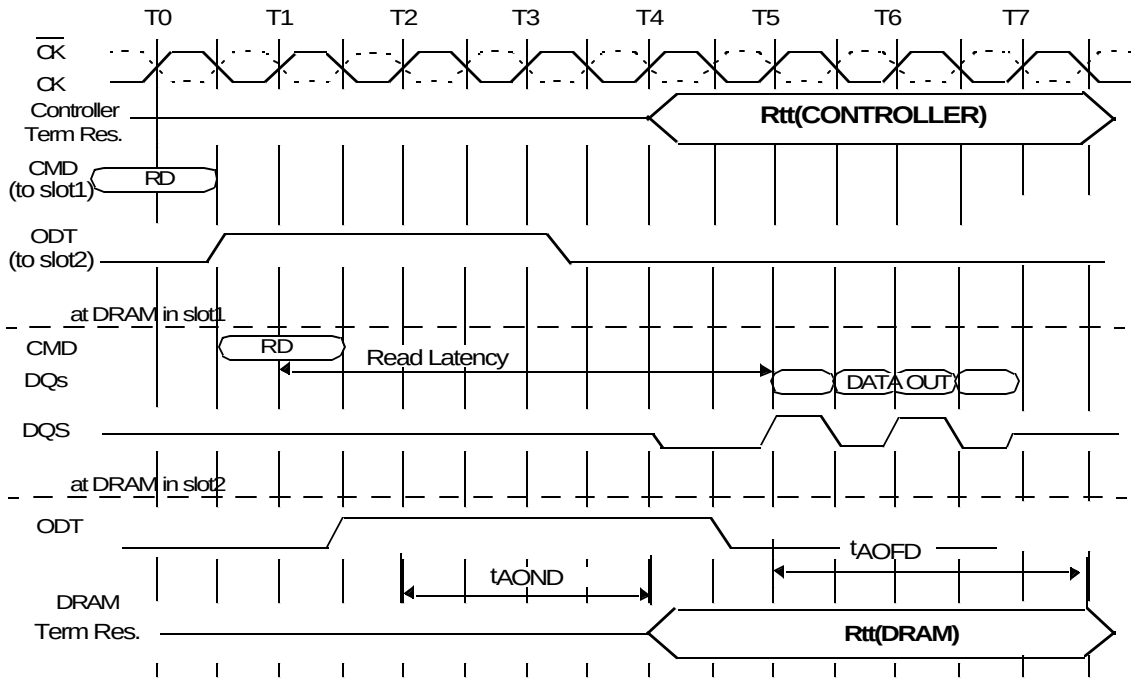
note 1: Alternatively, the controller may use rank2 for termination instead of rank1.

ODT Control of READs

At a minimum, ODT must be latched HIGH by CK at (Read Latency - 3^{t}CK) after the RD command and remain high until (Read Latency + BL/2 - 2^{t}CK) after the RD command (where Read Latency = AL + CL). The controller is also required to activate it's own termination with a turn on time the same as the DRAM and keeping it on until valid data is no longer on the system bus.



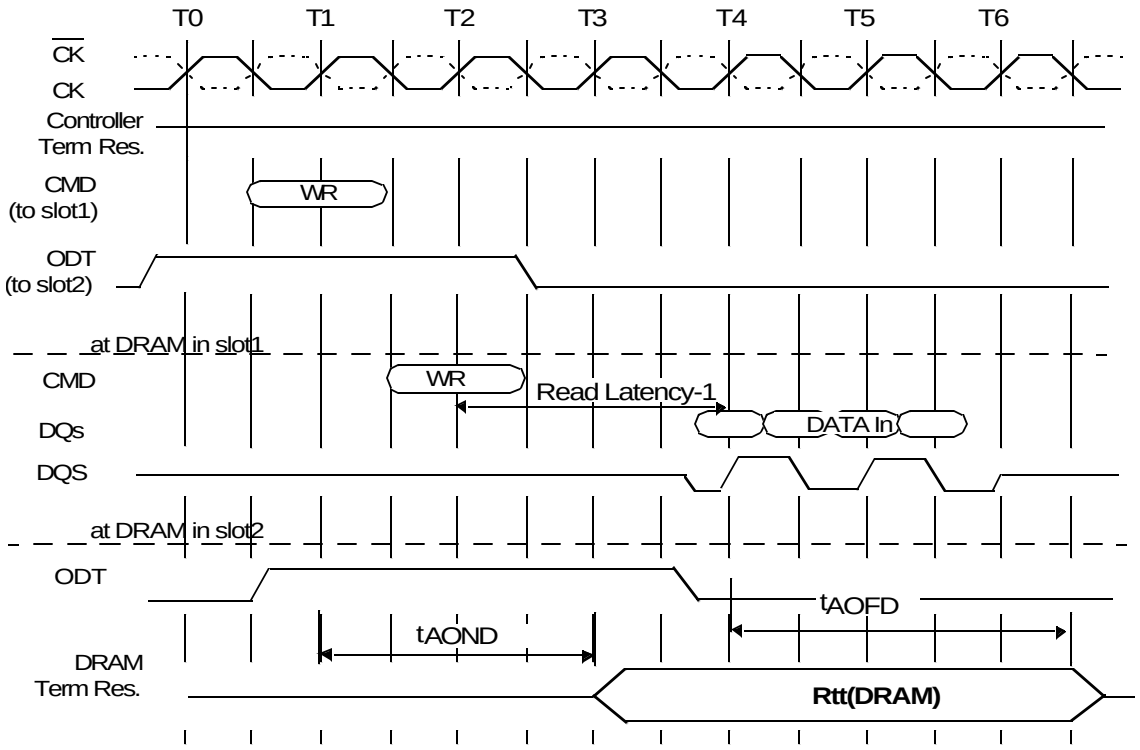
Read Example for a 2 slot registered system with 2nd slot in Active Mode
(Read Latency = 3 ^{t}CK; tAOND=2^{t}CK; tAOFD=2.5^{t}CK)



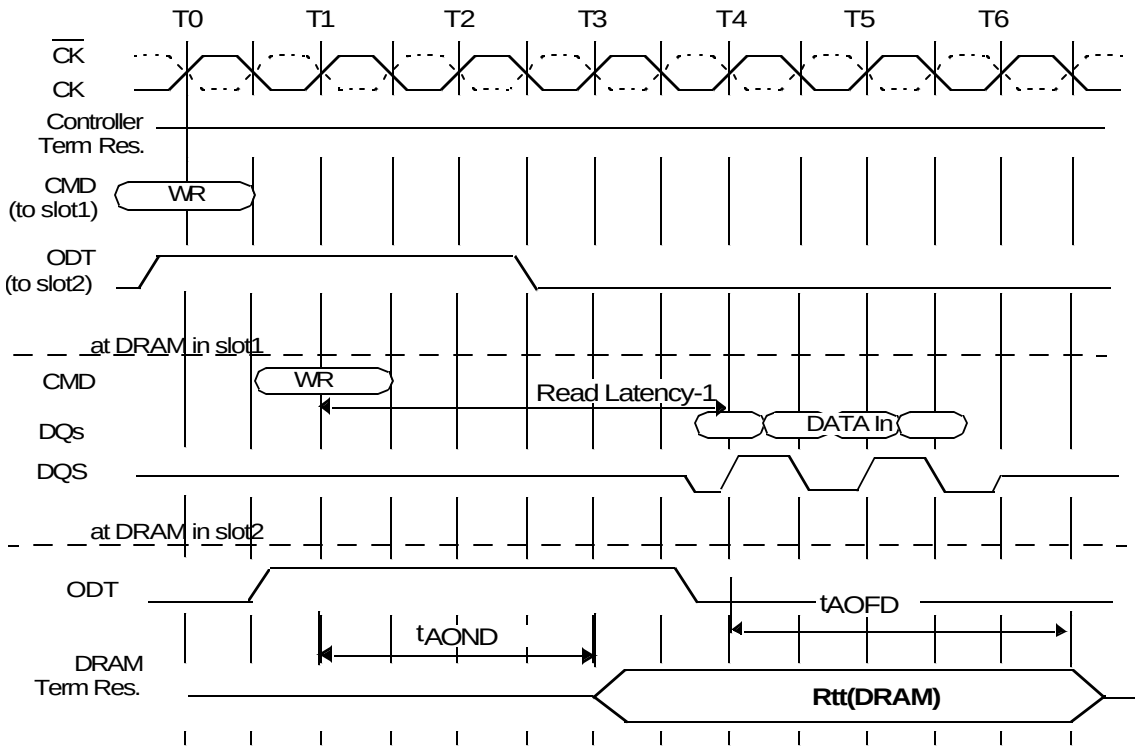
Read Example for a 2 slot registered system with 2nd slot in Active Mode
(Read Latency = 4^{t}CK; tAOND=2^{t}CK; tAOFD=2.5^{t}CK)

ODT Control of Writes

At a minimum, ODT must be latched HIGH by CK at (Write Latency - 3^{t}CK) after the WR command and remain high until (Write Latency + BL/2 - 2^{t}CK) after the WR command (where Write Latency = Read Latency - 1^{t}CK). During writes, no ODT is required at the controller.



Write Example for a 2 slot registered system with 2nd slot in Active Mode
(Read Latency = 3^{t}CK; tAOND=2^{t}CK; tAOFD=2.5^{t}CK)

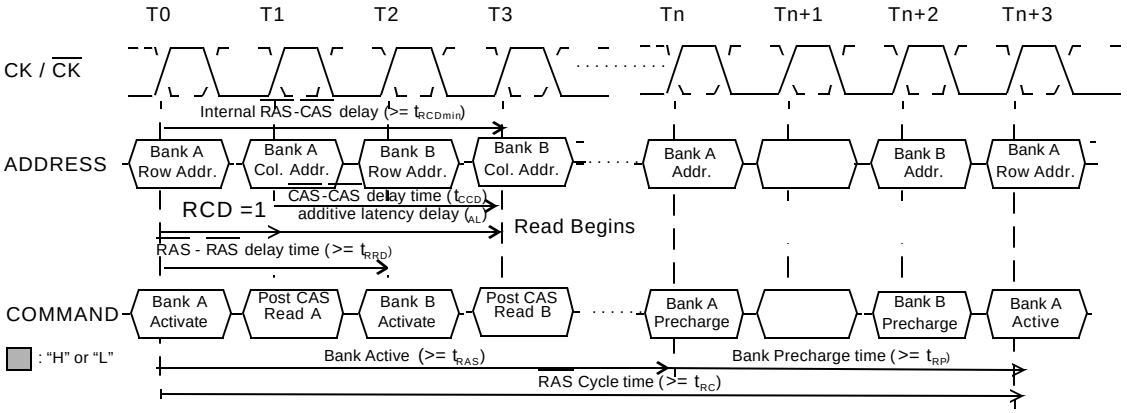


Write Example for a 2 slot registered system with 2nd slot in Active Mode
(Read Latency = 4tCK; tAOND=2tCK; tAOFD=2.5tCK)

3.2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 and BA1, are used to select the desired bank. The row address A0 through A13 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR-II SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}), which is equal to tRAS + tRP. The minimum time interval between Bank Activate commands, Bank 0,1, 2, 3 (in any order), is the Bank to Bank delay time (t_{RRD}).

Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2



3.2.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

The DDR-II SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 uniquely addressable boundary segments (4-bits each). A 4-bit burst operation will occur entirely within one of the 512 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

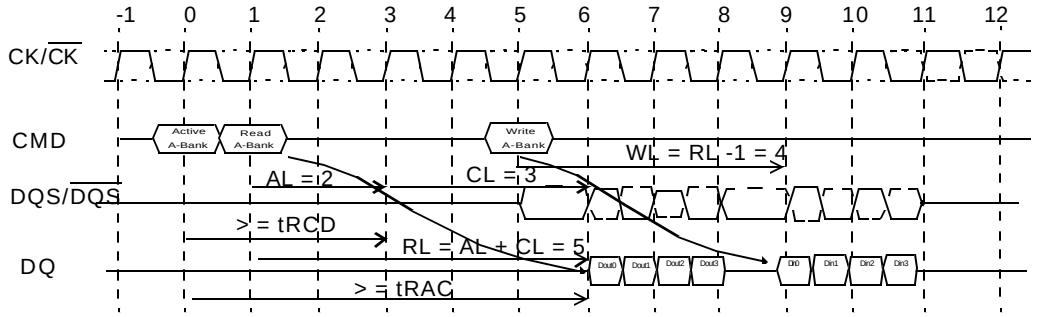
A new burst access must not interrupt the previous burst operation. The minimum CAS to CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

3.2.4.1 Posted $\overline{CAS}$

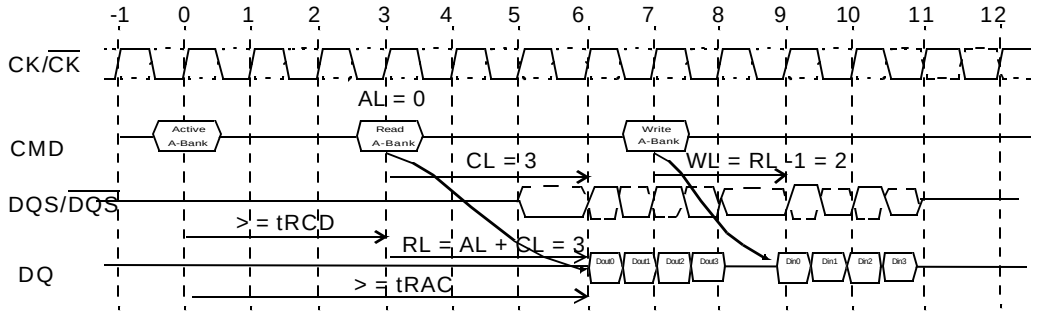
Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR-II SDRAM. In this operation, the DDR-II SDRAM allows a $\overline{CAS}$ read or write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the RAS-CAS-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS. The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL).

Examples of posted $\overline{CAS}$ operation

Example 1 Read followed by a write to the same bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4]



Example 2 Read followed by a write to the same bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2]



3.2.4.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR-II SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR-I SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR-I devices, interruption of a burst read or write operation is prohibited, but specially read interrupted by read & write interrupted by write at burst length 4bit boundary are allowed. Otherwise the Burst Stop command is not supported on DDR-II SDRAM devices.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	X 0 0	0, 1, 2, 3	0, 1, 2, 3
	X 0 1	1, 2, 3, 0	1, 0, 3, 2
	X 1 0	2, 3, 0, 1	2, 3, 0, 1
	X 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

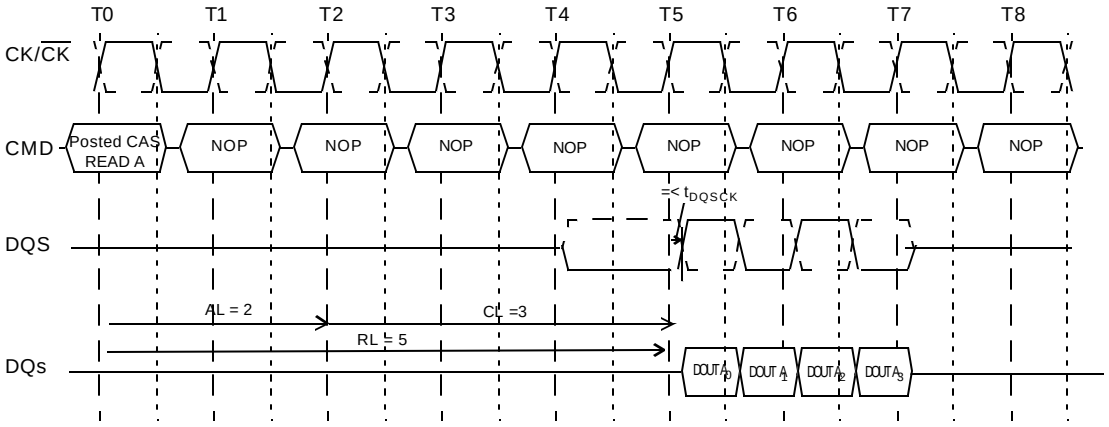
Note: Page length is a function of I/O organization and column addressing

** For BL of 8, the sequential mode is the nibble sequential mode.

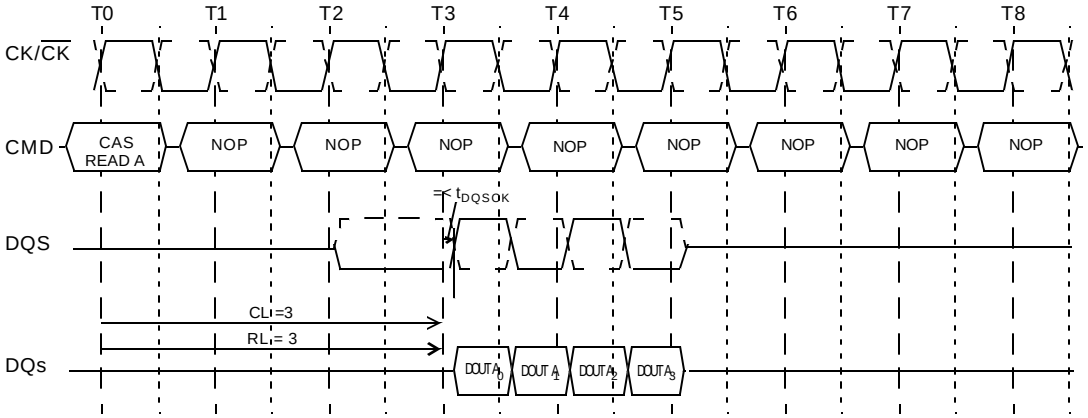
3.2.4.3 Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR-I SDRAMs. The AL is defined by the Extended Mode Register Set (EMRS).

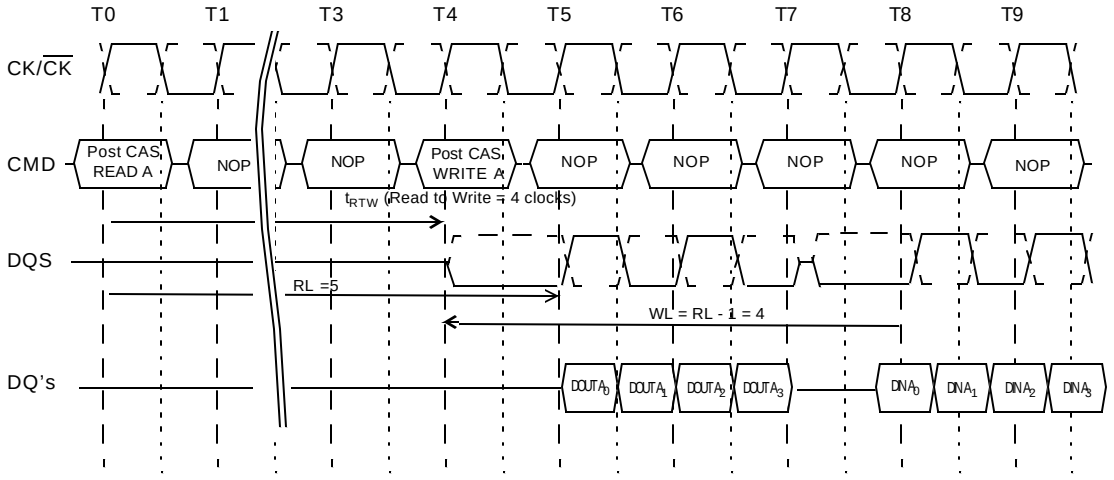
Burst Read Operation: RL = 5 (AL = 2, CL = 3), BL=4



Burst Read Operation: RL = 3 (AL = 0 and CL = 3), BL=4

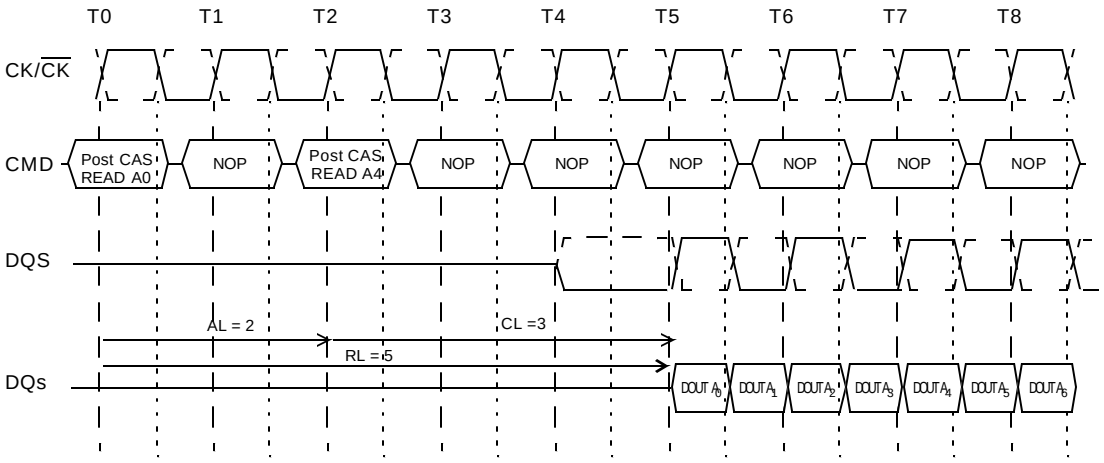


Burst Read followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL=4



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks .

Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL=4

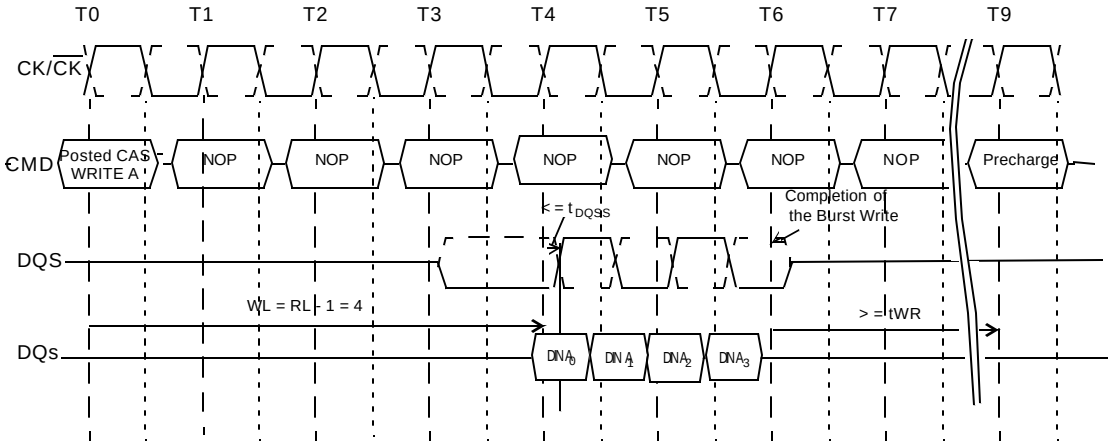


The seamless burst read operation is supported by enabling a read command at every other clock. This operation is allowed regardless of same or different banks as long as the banks are activated.

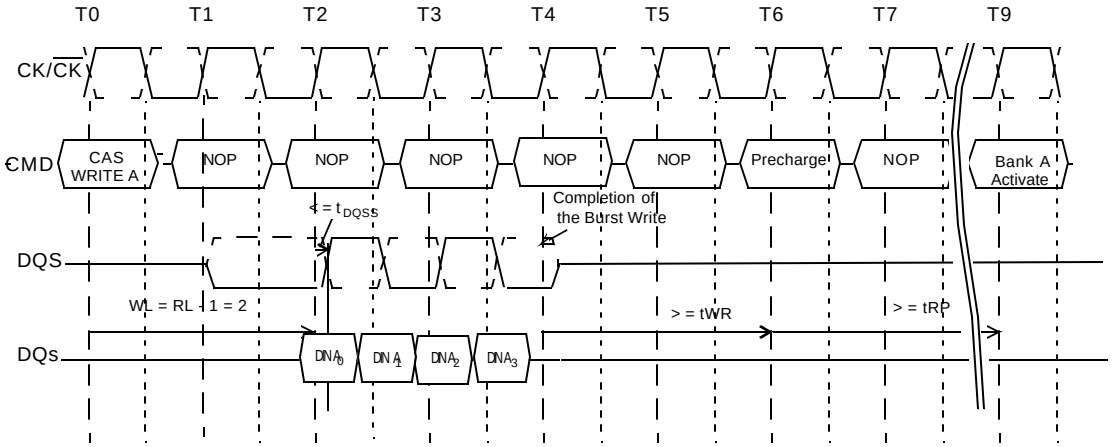
3.2.4.4 Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length of 4 is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (tWR).

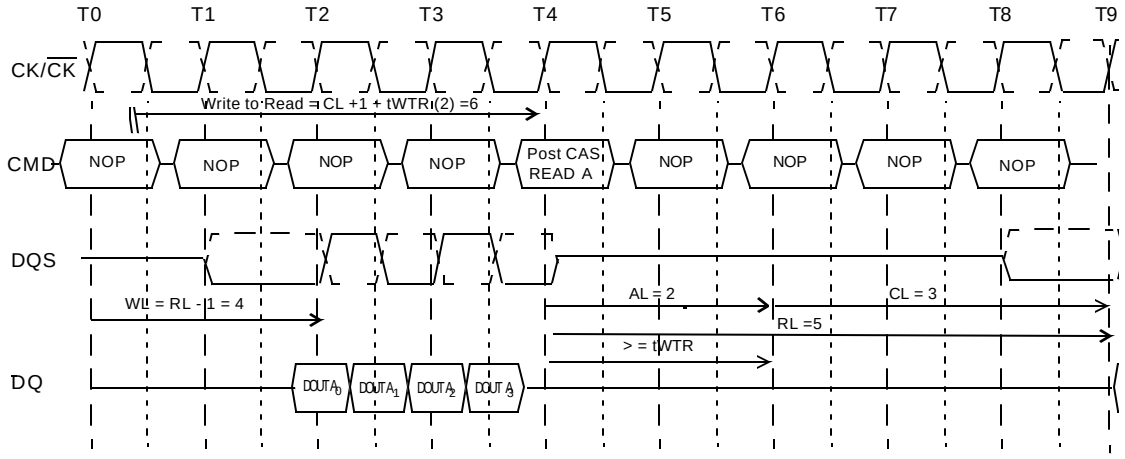
Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL=4



Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL=4

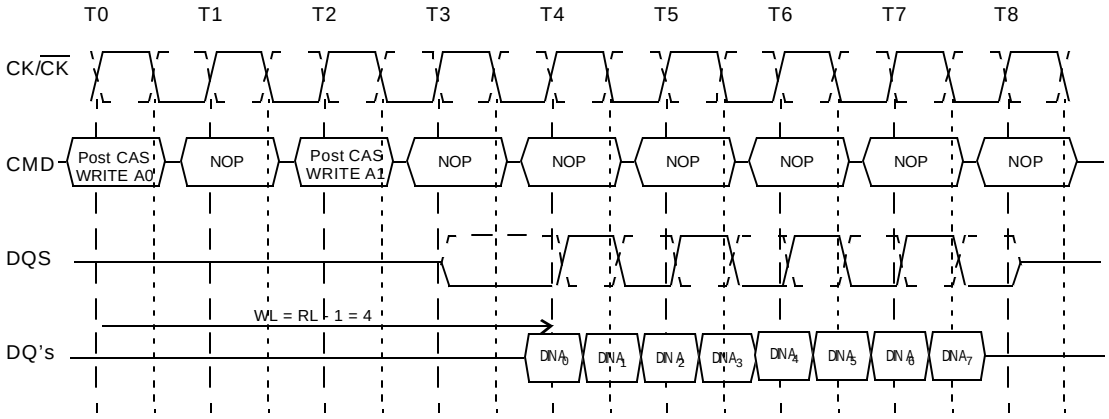


Burst Write followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL=4



The minimum number of clock from the burst write command to the burst read command is CL + 1 + a write-to-read-turn-around-time(tWTR). This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array.

Seamless Burst Write Operation: RL = 5, WL = 4, BL=8



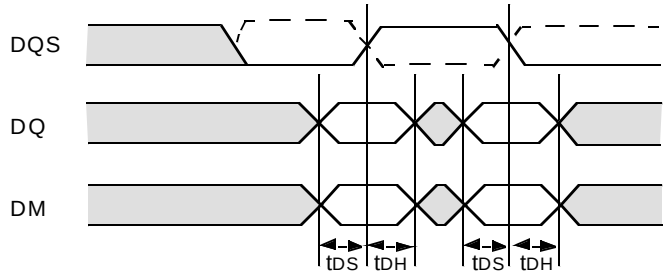
The seamless burst write operation is supported by enabling a write command every other clock. This operation is allowed regardless of same or different banks as long as the banks are activated

3.2.4.5 Write data mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR-II SDRAMs, Consistent with the implementation on DDR I SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is intermally loaded identically to data bits to insure matched system timing. DM is not used during read cycles.

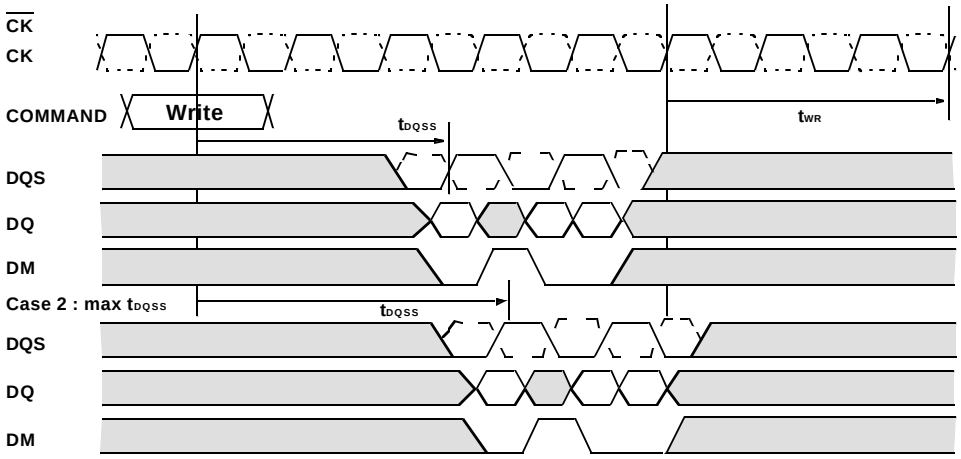
To allow the data mask function to occur at high frequencies, write recovery time t_{WR} and WRITE-to-READ delay t_{WTR} are given one extra clock cycle compared to DDR I

Data Mask Timing



Data Mask Function, WL=3, AL=0 shown

Case 1 : min t_{DQSS}



3.2.5 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 are used to define which bank to precharge when the command is issued.

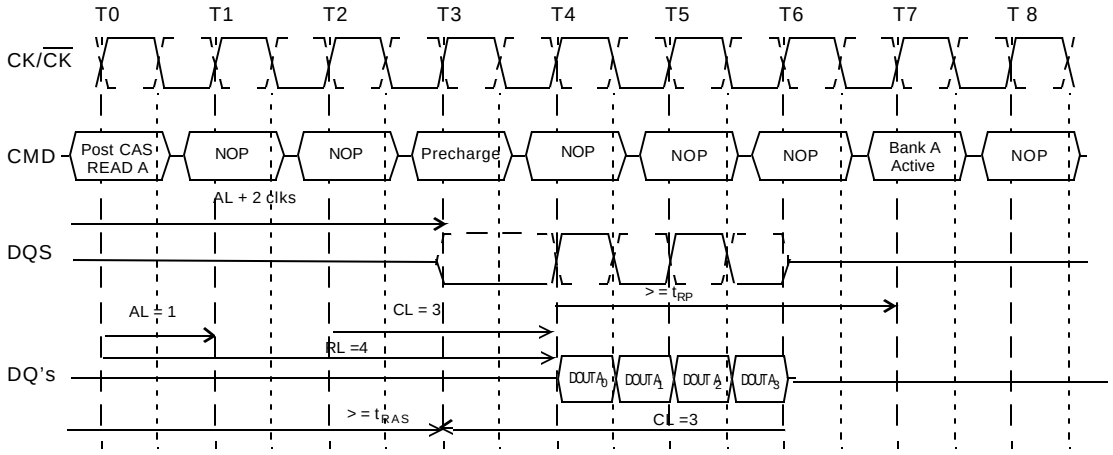
Bank Selection for Precharge by Address Bits

A10	BA0	BA1	Precharged Bank(s)
LOW	LOW	LOW	Bank 0 only
LOW	LOW	HIGH	Bank 1 only
LOW	HIGH	LOW	Bank 2 only
LOW	HIGH	HIGH	Bank 3 only
HIGH	DON'T CARE	DON'T CARE	All Banks 0 ~ 3

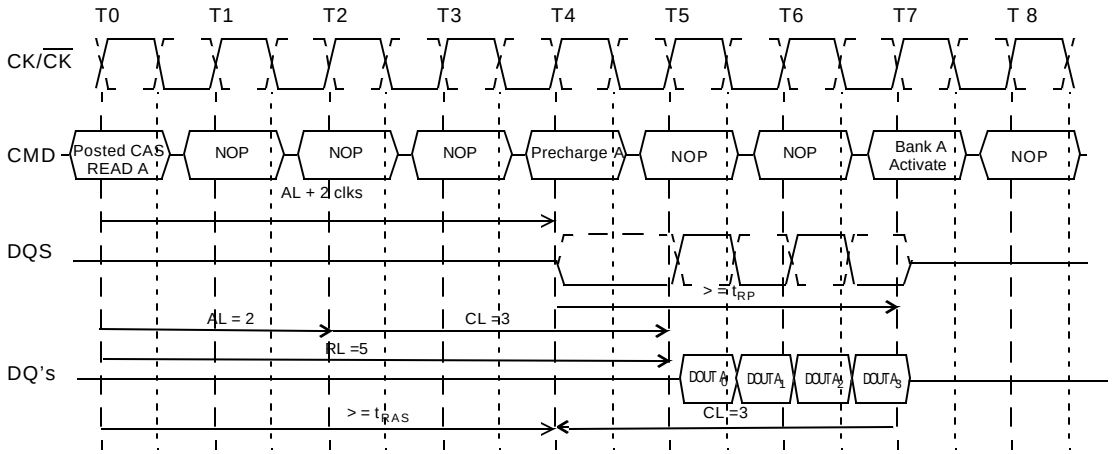
Burst Read Operation Followed by Precharge

Minium Read to precharge command spacing to the same bank = AL + BL/2 clocks
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

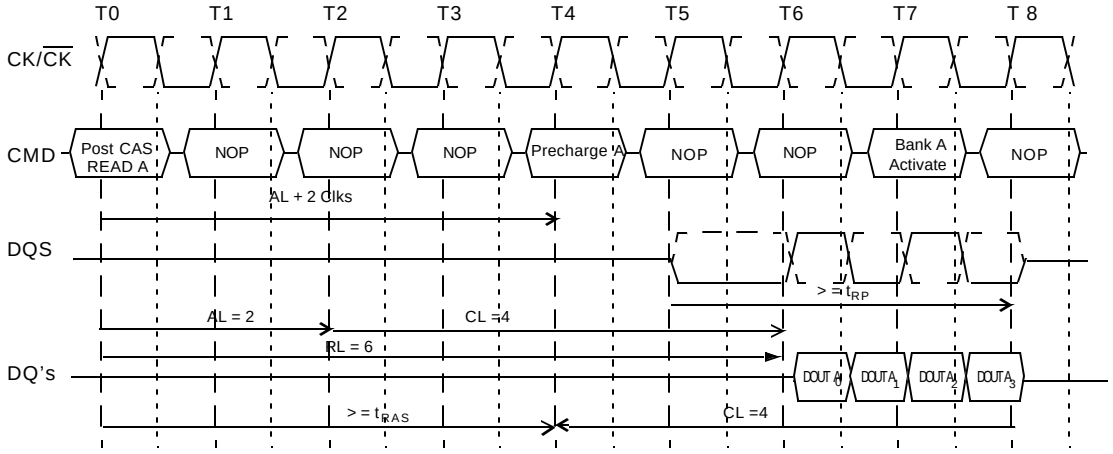
Example 1: Burst Read Operation Followed by Precharge: RL = 4 (AL=1, CL=3), BL=4



Example 2: Burst Read Operation Followed by Precharge: RL = 5 (AL=2, CL=3), BL=4



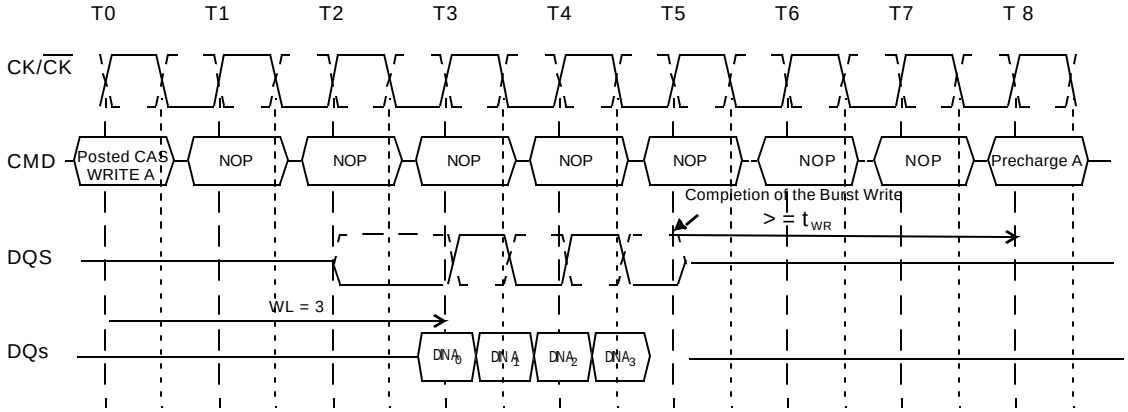
Example 3: Burst Read Operation Followed by Precharge: RL = 6 (AL=2, CL=4), BL=4



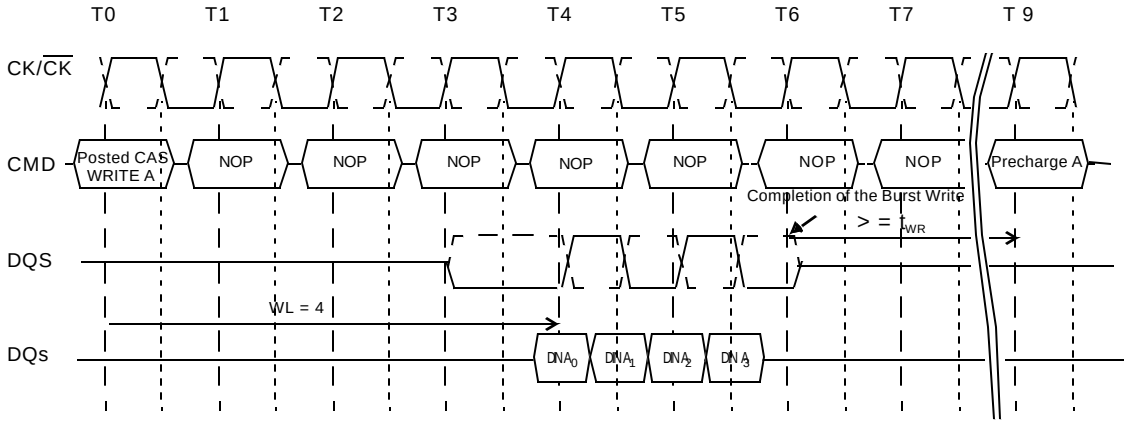
Burst Write followed by Precharge

Minium Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR
For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay, as DDR-II SDRAM does not support any burst interrupt operation.

Example 1: Burst Write followed by Precharge: WL = (RL-1) =3, BL=4



Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4, BL=4



3.2.6 Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the DDR-II SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is $\overline{CAS}$ latency (CL) clock cycles before the end of the read burst.

Auto-precharge also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Burst Read with Auto Precharge

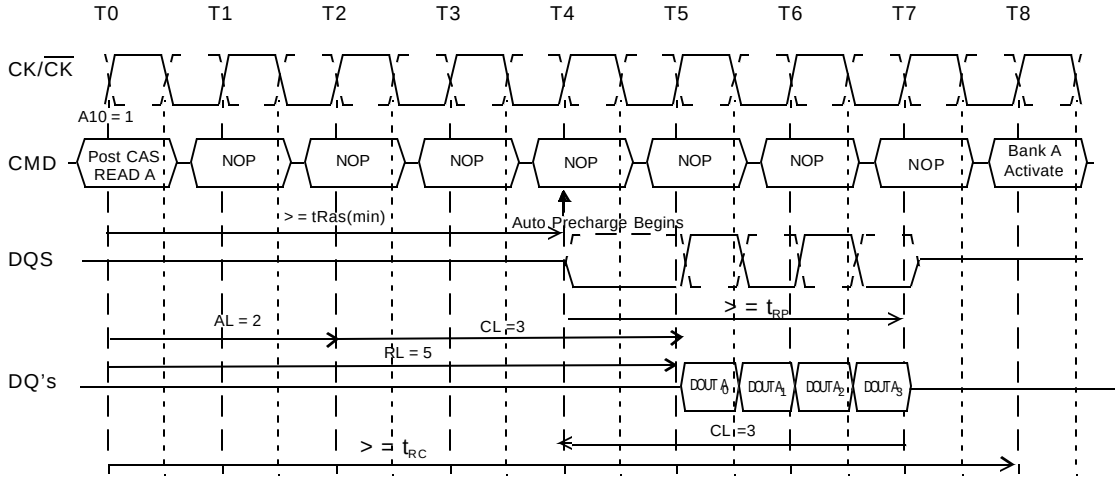
If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR-II SDRAM starts an auto Precharge operation on the rising edge which is (AL + 2)cycles later from the read with AP command when the condition that. when tRAS(min) is satisfied. If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied. A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

(1) The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

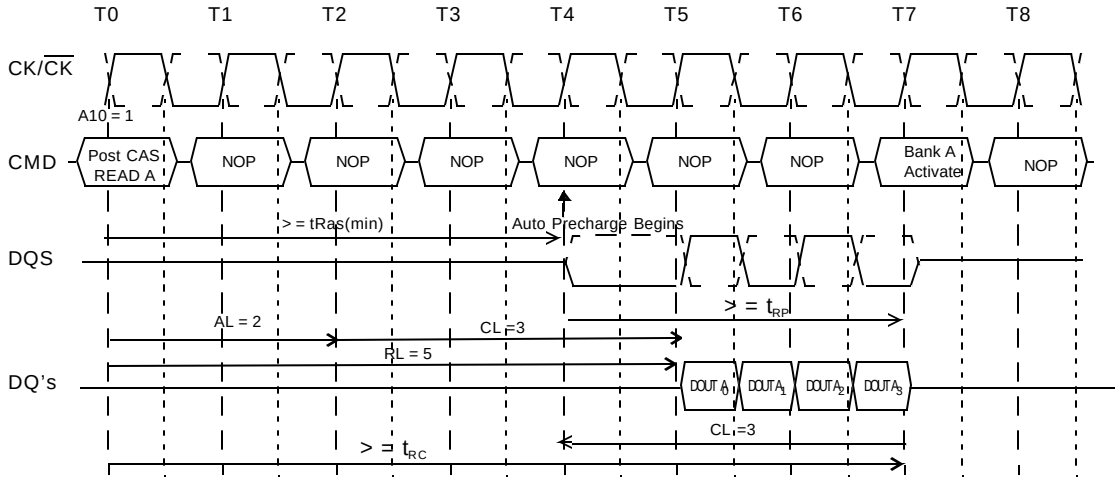
Burst Read with Auto Precharge Followed by an activation to the Same Bank(tRC Limit):

RL = 5 (AL = 2, CL = 3, internal tRCD = 3), BL=4



Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRP Limit):

RL = 5 (AL = 2, CL = 3, internal tRCD = 3), BL=4



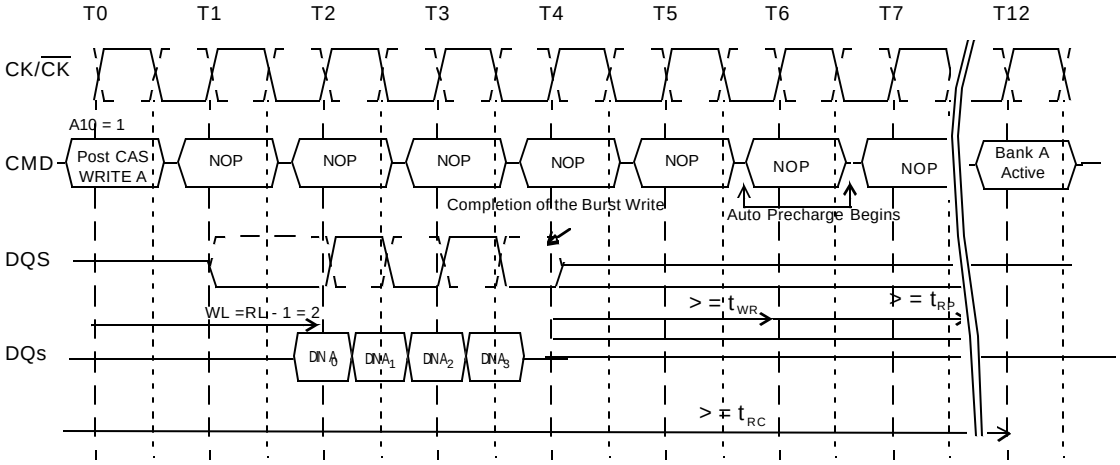
Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR-II SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

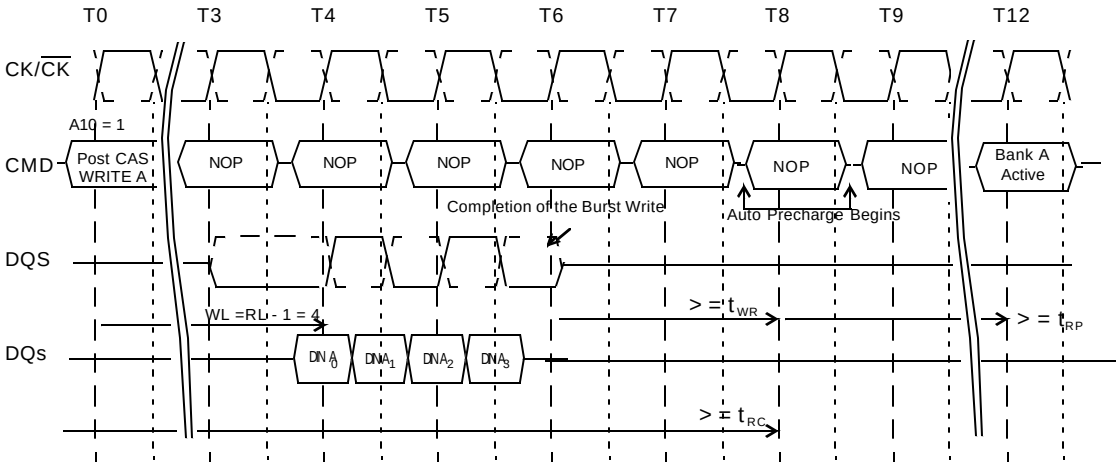
(1) The data-in to bank activate delay time (tWR + tRP) has been satisfied.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Burst Write with Auto-Precharge (tRC Limit): WL = 2, tWR =2, tRP=3, BL=4



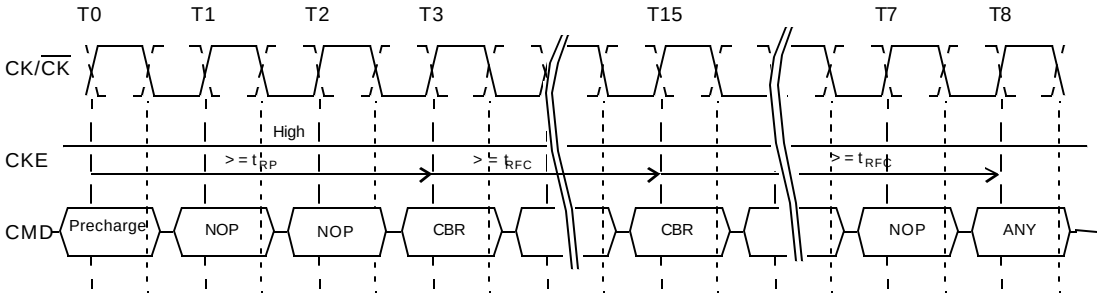
Burst Write with Auto-Precharge (tWR + tRP): WL = 4, tWR =2, tRP=3, BL=4



3.2.7 Automatic Refresh Command ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)

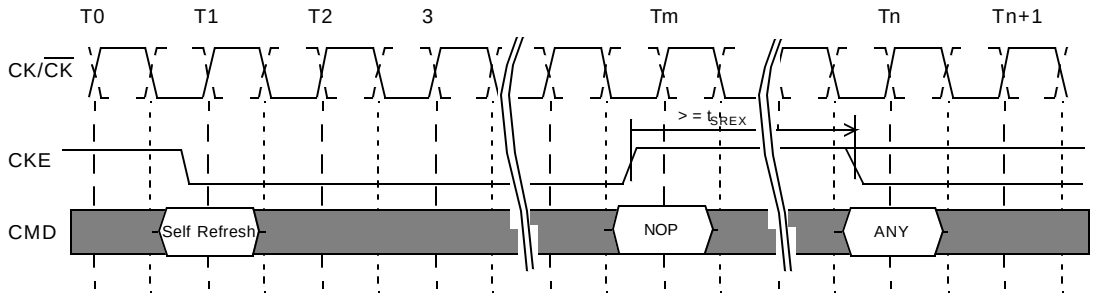
When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). All banks of the DDR-II SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto Refresh Command (CBR) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR-II SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the Auto Refresh cycle time (t_{RFC}).



3.2.8 Self Refresh Command

The DDR-II SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit Self Refresh operation. Once the clock is cycling, the exit command will be registered asynchronously by bringing CKE high. After CKE is brought high, an internal timer is started to insure CKE is held high for approximately 10ns before registering the Self Refresh exit command. The purpose of this circuit is to filter out noise glitches on the CKE input which may cause the DDR-II SDRAM to erroneously exit Self Refresh operation. Once the Self Refresh command is registered, a delay equal or longer than the tXSNR must be satisfied before any non-read command can be issued to the device. Additionally, a delay equal or longer than tXSRD must be satisfied before any read command. CKE must remain high for the entire Self Refresh exit period (t_{SREX}) and commands must be gated off with $\overline{CS}$ held high. Alternatively, NOP commands may be registered on each positive clock edge during the Self Refresh exit interval. (See Figure.)

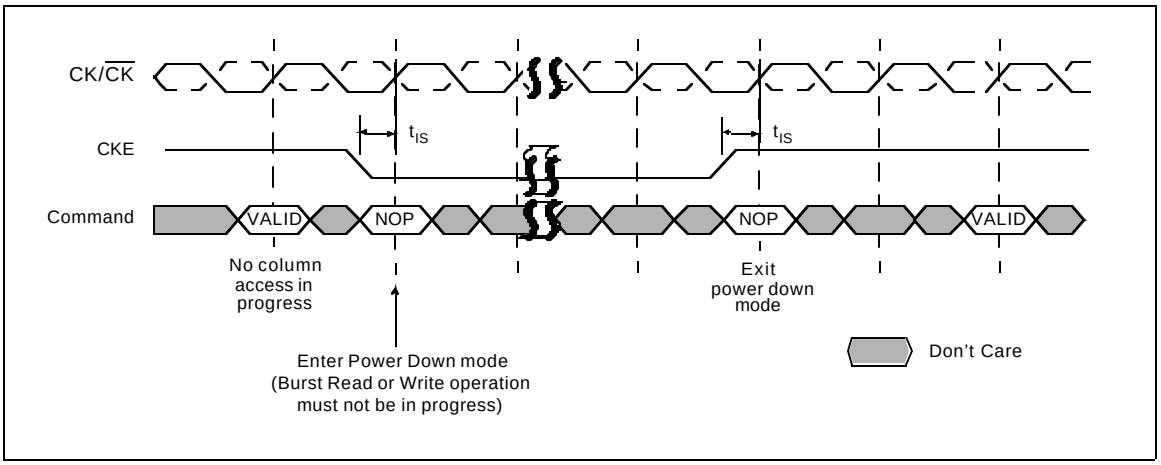


3.2.9 Power-Down

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. In Power Down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR-II SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered HIGH (along with a Nop or Deselect command). A valid, executable command may be applied two clock cycle later.

Power Down



Burst Interruption

Interruption of a burst read or write cycle is prohibited but read interrupted by read & write interrupted by write at burst length 4bit boundary are allowed

No Operation Command

The No Operation Command should be used in cases when the DDR-II SDRAM is in an idle or a wait state. The purpose of the No Operation Command is to prevent the DDR-II SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

4. Command Truth Table.

4.1 Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1	A13-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Mode Register Set	H	X	L	L	L	L	BA0 = 0 and MRS OP Code				1
Extended Mode Register Set	H	X	L	L	L	L	BA0 = 1 and EMRS OP Code				1
Auto (CBR) Refresh	H	H	L	L	L	H	X	X	X	X	1
Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	1
Exit Self Refresh	L	H	H	X	X	X	X	X	X	X	1
Single Bank Precharge	H	X	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	X	L	L	H	L	X	X	H	X	1
Bank Activate	H	X	L	L	H	H	BA	Row Address			1,2
Write	H	X	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	X	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	X	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	X	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Mode Entry	X	L	X	X	X	X	X	X	X	X	1,4,5
Power Down Mode Exit	X	H	X	X	X	X	X	X	X	X	1,4,5

1. All of the DDR-II SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, and $\overline{CAS}$ at the positive rising edge of the clock.
2. Bank Select (BA0,1), determine which bank is to be operated upon.
3. Burst read or write cycle may not be terminated.
4. The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
5. If $\overline{CS}$ is low, then when CKE returns high, no command is registered into the chip for one clock cycle.

4.2 Clock Enable (CKE) Truth Table

Current State	CKE		Command					Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1, BA0, A13 - A0		
Self Refresh	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	Exit Self Refresh with No Operation	2
	L	H	L	Command			Address	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	Command			Address	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X		Device Deselect	3
	H	H	L	Command			Address	Refer to the Current State Truth Table	3
	H	L	H	X	X	X		Power Down	
	H	L	L	Others			X	INVALID	
	H	L	L	L	L	H	X	Entry Self Refresh	4
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	Power Down	5
	L	H	X	X	X	X	X	Power Down	
	L	L	X	X	X	X	X	Power Down	

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CES}) must be satisfied before any command other than self refresh exit.
3. The inputs (BA1, BA0, A13 - A0) depend on the command that is issued. See the Current State Truth Table for more information.
4. The Auto Refresh, Self Refresh Mode, and the Mode Register Set modes can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

5. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Power Supply Voltage	-1.0 to +3.6	V	1
VDDQ	Power Supply Voltage for Output	-0.5 to +3.6	V	1
V_{IN}	Input Voltage	-0.5 to +3.6	V	1
V_{OUT}	Output Voltage	-0.5 to +3.6	V	1
T_J	Operating Temperature (Junction)	0 to +85	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6. AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL) - 1.8

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	4
VDDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	4, 5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	5, 6
VREF	Input Reference Voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V	1.2
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
3. VTT of transmitting device must track VREF of receiving device.
4. There may be DDR-II parts with 2.5V Vdd in the market, but 1.8V Vdd is expected to dorminate DDR-II market
5. Vddq tracks to Vdd, VDDL tracks to Vdd
6. Note 5 does not apply when Vdd = 2.5V normial

Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic high	VREF + 0.125	VDDQ + 0.3V	V	
V_{IL}(dc)	dc input low	- 0.3	VREF - 0.125	V	

Input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(ac)	ac input logic high	VREF + 0.250	-	V	
V_{IL}(ac)	ac input low	-	VREF - 0.250	V	

Output Buffer Levels

Output AC Test Conditions

Symbol	Parameter	Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	Vref + 0.63	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	Vref - 0.63	V	
V_{OTR}	Output Timing Measurement Reference Level	Vref	V	1

1. The VDDQ of the device under test is referenced.

Output DC Current Drive

Symbol	Parameter	Class II	Units	Notes
I_{OH}	Output Minimum Source DC Current	-12.6	mA	1, 3, 4
I_{OL}	Output Minimum Sink DC Current	12.6	mA	2, 3, 4

1. VDDQ = 1.7V; VOUT = 1.4V.
2. VDDQ = 2.3V; VOUT = 0.45V.
3. The dc value of VREF applied to the receiving device is expected to be set to VTT.

PACKAGE CAPACITANCE ASSUMPTIONS (FBGA)

Parameter	Symbol	Min	Max	Units
Input capacitance, CK and $\overline{CK}$	CCK	1.5	2.5	pf
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.5	2.5	pf
Input capacitance delta, all other input-only pins	CDI	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	3.0	4.0	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	pF

Operating Currents (T_J= 0 to + 85°C, VDD= 1.8V +/- 0.1V, VDDQ= 1.8V +/- 0.1V)

Symbol	Parameter/Condition	Ma	Unit	Notes
I_{DD0}	**Operating Current**: one bank; active / precharge; $t_{RC} = t_{RC\ MIN}$; $t_{CK} = t_{CK\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	mA	1, 2
I_{DD1}	**Operating Current**: one bank; active / read / precharge; Burst = 2; $t_{RC} = t_{RC\ MIN}$; CL = 2.5; $t_{CK} = t_{CK\ MIN}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	TBD	mA	1, 2
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE ≤ $V_{IL\ MAX}$; $t_{CK} = t_{CK\ MIN}$	TBD	mA	1, 2
I_{DD2N}	**Idle Standby Current:** $\overline{CS}$ ≥ $V_{IH\ MIN}$; all banks idle; CKE ≥ $V_{IH\ MIN}$; $t_{CK} = t_{CK\ MIN}$; address and control inputs changing once per clock cycle	TBD	mA	1, 2
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE ≤ $V_{IL\ MAX}$; $t_{CK} = t_{CK\ MIN}$	TBD	mA	1, 2
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS}$ ≥ $V_{IH\ MIN}$; CKE ≥ $V_{IH\ MIN}$; $t_{RC} = t_{RAS\ MAX}$; $t_{CK} = t_{CK\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	mA	1, 2
I_{DD4R}	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK\ MIN}$; I_{OUT} = 0mA	TBD	mA	1, 2
I_{DD4W}	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK\ MIN}$	TBD	mA	1, 2
I_{DD5}	**Auto-Refresh Current** : $t_{RC} = t_{RFC\ MIN}$	TBD	mA	1, 2
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	TBD	mA	1, 2, 3
I_{DD7A}	**Operating Current - Four bank operation**: Four bank interleaving with BL=4	TBD	mA	1, 2

1. I_{DD} specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ns.
3. Enables on-chip refresh and address counters.

Electrical Characteristics & AC Timing for DDR400/DDR533 - Absolute Specification

(0 °C ≤ T_J ≤ 85 °C; V_{DD} = 1.8V ± 0.1V; V_{DDQ} = 1.8V ± 0.1V)

REFRESH PARAMETERS

Parameter	Symbol	512Mb	Units
Auto refresh to active/auto refresh command time	tRFC	97.5	ns
Average periodic refresh interval	tREFI	7.8	µs

TIMING PARAMETERS BY SPEED GRADE

Parameter	Symbol	DDR II 400		DDR II 533B		DDR II 533A		Units
		min	max	min	max	min	max	
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	-500	+500	ps
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	-450	+450	ps
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	min(tCL,tCH)	x	ps
Clock cycle time, CL=3	tCK	-	-	-	-	5000	8000	ps
Clock cycle time, CL=4		5000	8000	-	-	3750	8000	ps
Clock cycle time, CL=5		-	-	3750	8000	-	-	ps
DQ and DM input hold time	tDH	400	x	350	x	350	x	ps
DQ and DM input setup time	tDS	400	x	350	x	350	x	ps
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	0.35	x	tCK
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	x	tAC max	ps
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	x	300	ps
DQ hold skew factor	tQHS	x	450	x	400	x	400	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
Write command to first DQS latching transition	tDQSS	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	tCK
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	tCK

DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	tCK
Mode register set command cycle time	tMRD	2	x	2	x	2	x	tCK
Write preamble setup time	tWPRES	0	x	0	x	0	x	ps
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.25	x	0.25	x	0.25	x	tCK
Address and control input hold time	tIH	600	x	500	x	500	x	ps
Address and control input setup time	tIS	600	x	500	x	500	x	ps
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to precharge command	tRAS	45	x	45	x	45	x	ns
Active to active/auto refresh command time	tRC	65	x	60	x	60	x	ns
Active to read or write command delay	tRCD	20	x	15	x	15	x	ns
Precharge command period	tRP	20	x	15	x	15	x	ns
Active to autoprecharge delay	tRAP	tRCDmin	x	tRCDmin	x	tRCDmin	x	ns
Active bank A to active bank B command period (Note : 2*tCK min at any frequency)	tRRD 2KB page	10	x	10	x	10	x	ns
	tRRD 1KB page	7.5	x	7.5	x	7.5	x	ns
Write recovery time	tWR	15	x	15	x	15	x	ns
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tWR+tRP*	x	tCK
Internal write to read command delay	tWTR	10	x	7.5	x	7.5	x	ns
Exit self refresh to any command	tXSC	200		200		200		tCK
Exit power down to any non-read command	tXPNR	2	x	2	x	2	x	tCK
Exit active power down to read command	tXARD	2	x	2	x	2	x	tCK
Exit precharge power down to read command	tXPRD	6-AL	x	6-AL	x	6-AL	x	tCK
*: tDAL formula and description will be the same as that used for DDR I								

Parameter	Symbol	DDR II 667		Units
		min	max	
DQ output access time from CK/$\overline{CK}$	tAC			ps
DQS output access time from CK/$\overline{CK}$	tDQSCK			ps
CK high-level width	tCH	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	tCK
CK half period	tHP	min(tCL,tCH)	x	ps
Clock cycle time, CL=4	tCK	3000	8000	ps
DQ and DM input hold time	tDH		x	ps
DQ and DM input setup time	tDS		x	ps
Control & Address input pulse width for each input	tIPW	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	x	tCK
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	ps
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x		ps
DQ hold skew factor	tQHS	x		ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	ps
Write command to first DQS latching transition	tDQSS	WL- 0.25	WL+ 0.25	tCK
DQS input high pulse width	tDQSH	0.35	x	tCK
DQS input low pulse width	tDQSL	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	tCK
Mode register set command cycle time	tMRD	2	x	tCK
Write preamble setup time	tWPRES	0	x	ps
Write postamble	tWPST	0.4	0.6	tCK
Write preamble	tWPRE	0.25	x	tCK
Address and control input hold time	tIH		x	ps
Address and control input setup time	tIS		x	ps
Read preamble	tRPRE	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	tCK
Active to precharge command	tRAS	45	x	ns

Active to active/auto refresh command time	tRC		x	ns
Active to read or write command delay	tRCD		x	ns
Precharge command period	tRP		x	ns
Active to autoprecharge delay	tRAP	tRCDmin	x	ns
Active bank A to active bank B command period (Note : 2*tCK min at any frequency)	tRRD 2KB page	10	x	ns
	tRRD 1KB page	7.5	x	ns
Write recovery time	tWR		x	ns
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tCK
Internal write to read command delay	tWTR	7.5	x	ns
Exit self refresh to any command	tXSC	200		tCK
Exit power down to any non-read command	tXPNR	2	x	tCK
Exit active power down to read command	tXARD	2	x	tCK
Exit precharge power down to read command	tXPRD	6-AL	x	tCK
*: tDAL formula and description will be the same as that used for DDR I				