OKI Electronic Components

KGL4226D 14-Gbps 1:16 DEMUX

1. DESCRIPTION

KGL 4226D converts one data stream into 16bit parallel data operating over 14GHz clock frequency. The KGL 4226D is fabricated by OKI 0.18μm gate length GaAs MESFETs process. By using of OKI unique flip-flops, which are MCFF(Memory Cell type Flip Flop) and CBFF(Common gate Bias Flip Flop), high speed operation has been realized. Capacitive coupling is recommended for clock input connection. The data input level is compatible with SCFL. Low speed signal interfaces are compatible with ECL. The device is mounted in 48pin package

2. ABSOLUTE MAXIMUM RATINGS

No.	Item	Symbol	Min.	Max.	Units
1	Supply Voltage	VTT	-2.3	0.3	V
2	Clock and Data Input Voltage	VCDI	-2.3	-0.5	V
3	Package Base Temperature under Bias	Ts	-45	100	°C
4	Storage Temperature	Tst	-45	125	°C

3. FUNCTIONAL BLOCK DIAGRAM

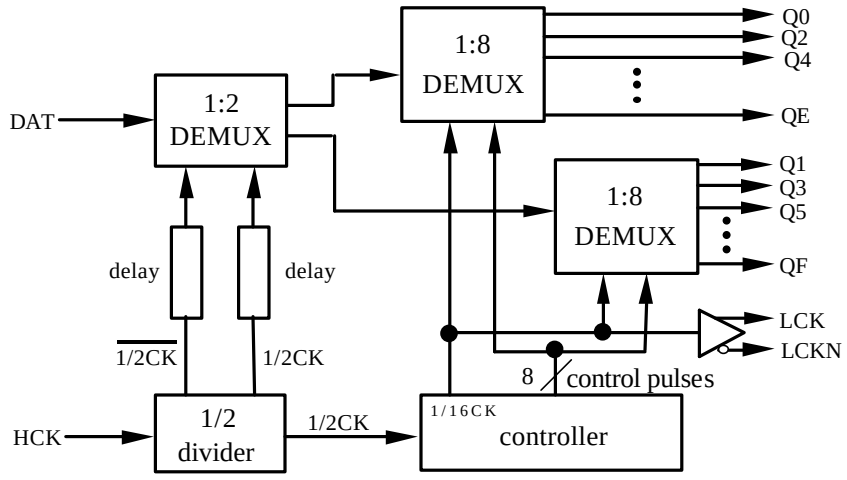


Figure 1 Block Diagram of KGL4226D

4. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Units
Power Supply	VTT	-2.1	-2.0	-1.9	V
Operating Temperature Range at Package Base	Ts	0		70	°C

5. ELECTRICAL CHARACTERISTICS

5-1. AC CHARACTERISTICS

VTT=-2V±0.1V, Ts = 0~70°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Units
Clock Period	Δt_C		71	-	-	ps
Set-up Time (DAT to HCK↓)	t_{DS}	Input clock period : 71ps	TBD	-13	TBD	ps
Hold Time (HCK↓ to DAT)	t_{DH}	Input clock period : 71ps	TBD	33	TBD	ps
HCK-DAT Phase Margin	Δt_M	Input clock period : 71ps	TBD	30	-	ps
LCK↓ to Output Data Delay	t_{C16O}	Input clock period : 71ps	0	45	90	ps

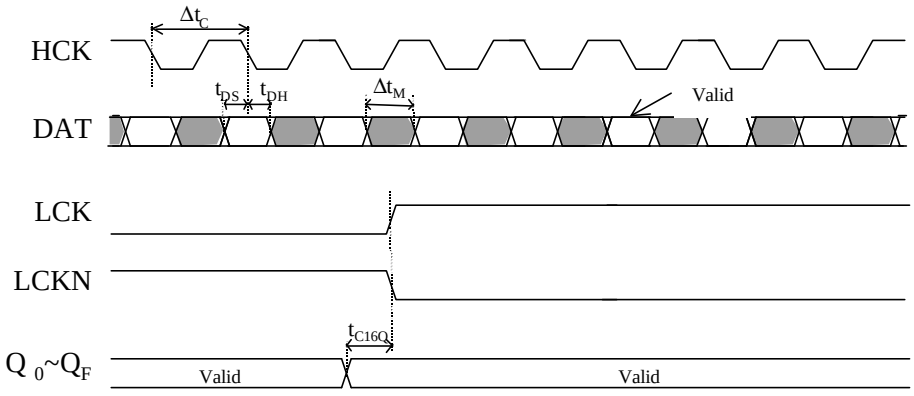


Figure 2 Waveforms of KGL4226D

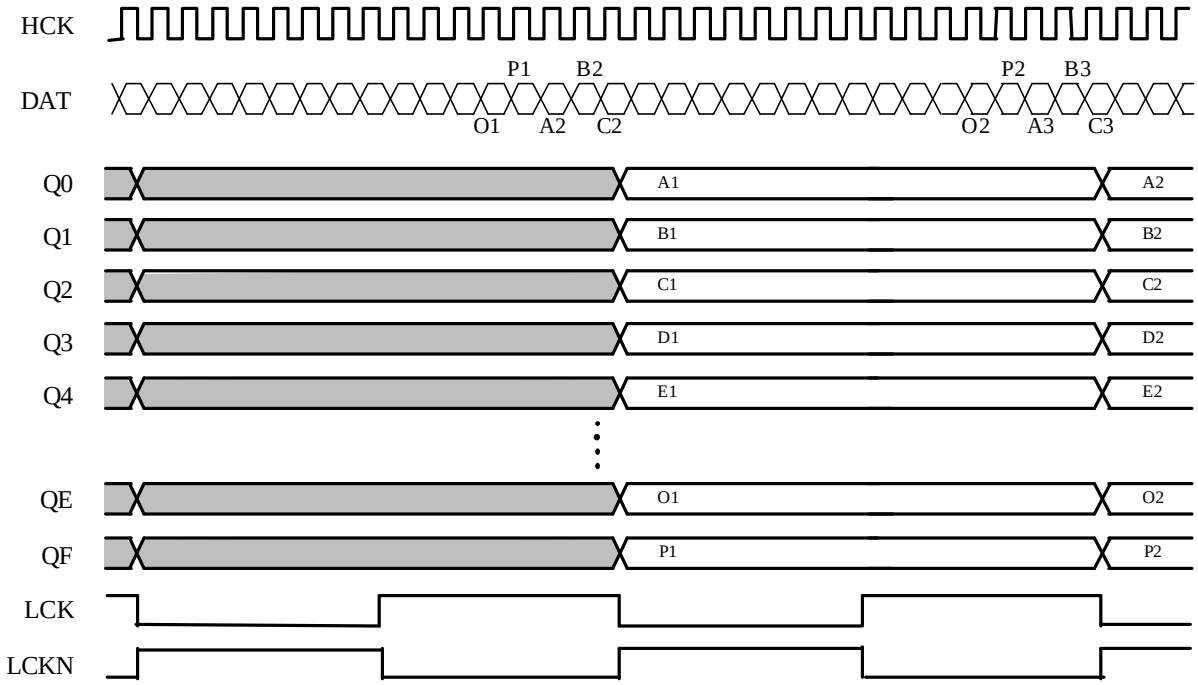


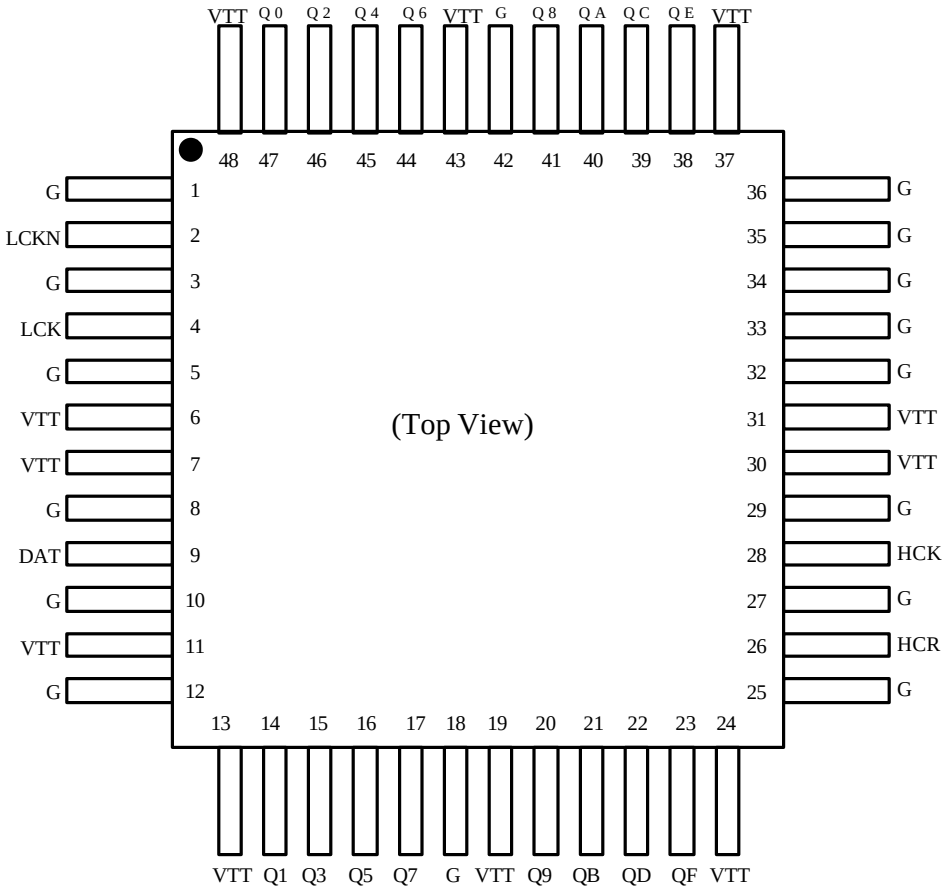
Figure 3 Time Chart of KGL4226D

5-2. DC CHARACTERISTICS

VTT=-2V±0.1V, Ts = 0~70°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Units
Power Dissipation	PW			2.2	2.8	W
Clock Input Voltage Swing (HCK)	VCKI	AC Coupling	TBD	1.0	TBD	Vpp
Low Level of Data Input (DAT)	VDIL	50 Ω to GND	TBD	-0.8	TBD	V
High Level of Data Input (DAT)	VDIH	50 Ω to GND	TBD	-0.2	TBD	V
Low level of Data Output (Q0~QF)	VDOL	50 Ω to VTT	-1.95	-1.8	-1.6	V
High level of Data Output (Q0~QF)	VDOH	50 Ω to VTT	-1.1	-0.9	-0.75	V
Low Level of 1/16 clock Output (LCN, LCKN)	VCOL	50 Ω to VTT	-1.95	-1.8	-1.55	V
High Level of 1/16 clock Output (LCN, LCKN)	VCOH	50 Ω to VTT	-1.15	-0.93	-0.75	V

6. PIN ASSIGNMENT



Note: 1 G is a ground terminal.
2 HCR is a reference bias terminal of clock. Usually HCR is connected to VTT through a capacitor (100nF).

Figure 4 PIN Assignment of KGL4226D

7. PACKAGE DIMENSIONS

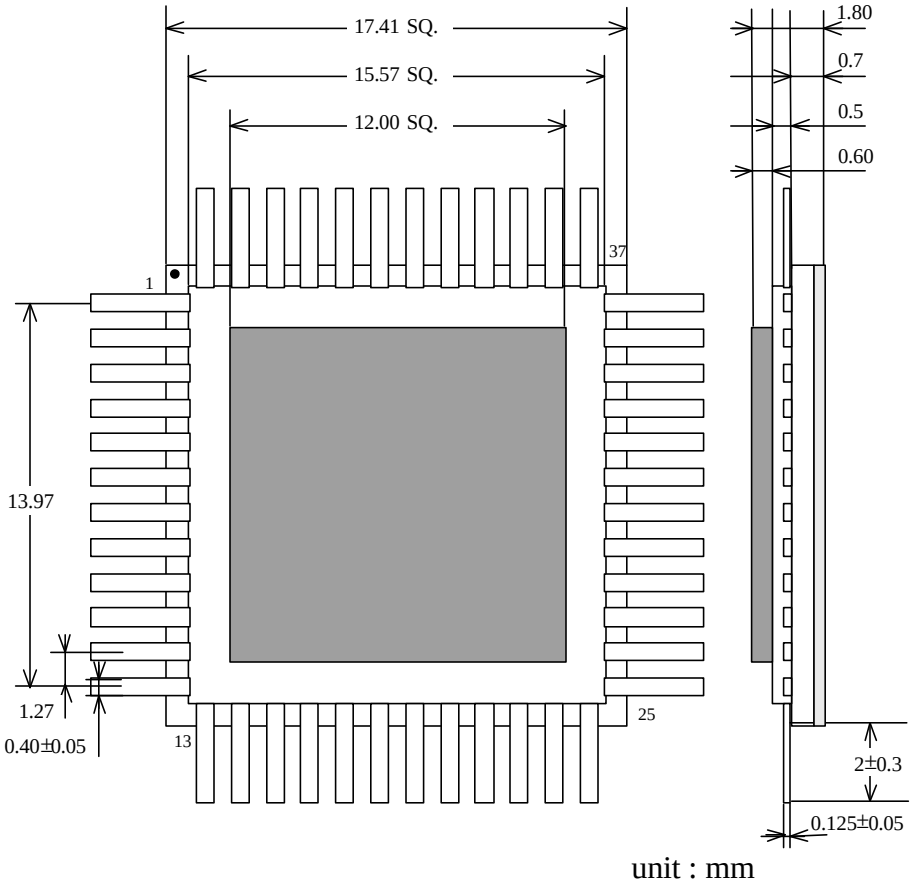


Figure 5 48pin Package Dimensions

8. TYPICAL INTERFACE CONFIGURATION

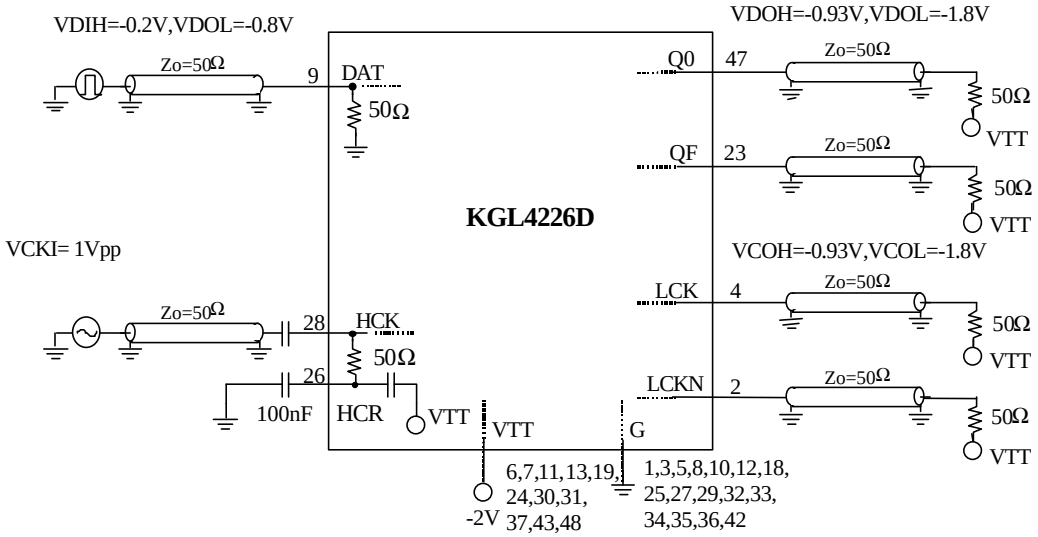


Figure 6 Typical Interfacing Configuration of KGL4226D