KGL4224 5-Gbps 8:1 DEMUX

1. SCOPE

This document describes the electrical characteristics of the KGL4224.

2. PRODUCT NAME

KGL4224

3. FUNCTIONS

This device converts serial data into 8bit parallel streams up to 5GHz clock frequency. Output parallel data are synchronized with an internal 1/8clock, which is generated by dividing the input clock on chip.

Functional diagram and time chart are indicated Figure1 and Figure2.

4. ABSOLUTE MAXIMUM RATINGS

No.	Item	Symbol	Min.	Max.	Unit
1	Supply Voltage for Internal Logic	VDD	-0.3	2.3	V
2	Supply Voltage for Output Buffer	VB	-0.3	2.3	V
3	Clock Input	CK	-0.3	1.5	V
4	Data Inputs	D	-0.3	1.5	V
6	Temperature at Package Base under Bias	Ts	-45	100	•
7	Storage Temperature	Tst	-45	125	•

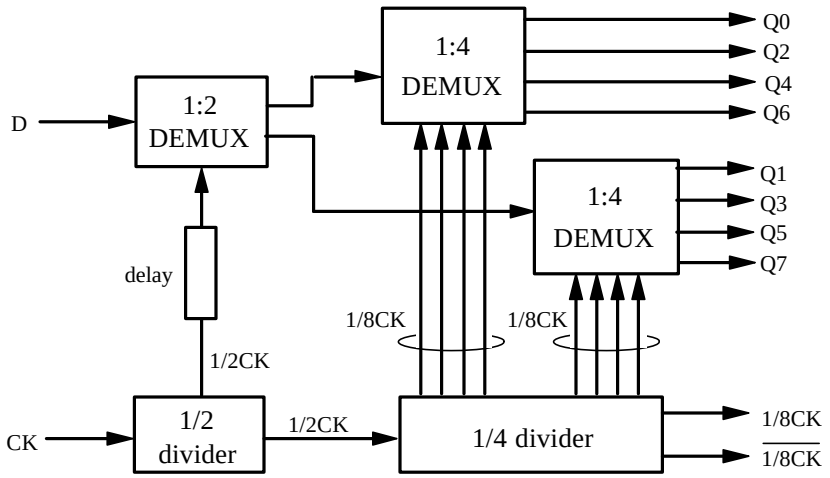


Figure 1 Block Diagram of KGL4224

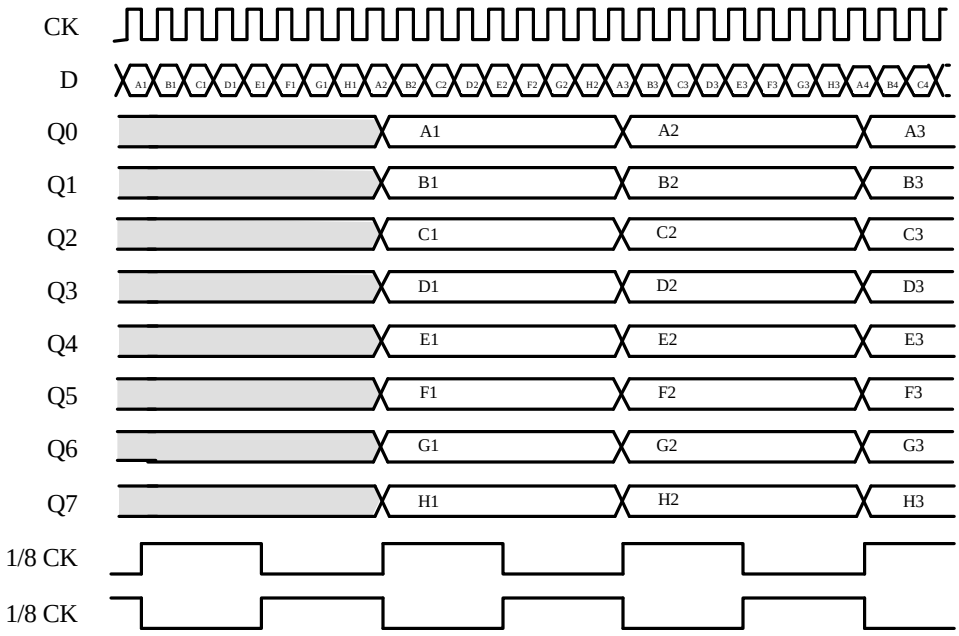


Figure 2 Time Chart of KGL4224

5. RRECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage for Internal Logic	VDD	1.9	2.0	2.1	V
Power Supply Voltage for Output Buffer	VB	1.9	2.0	2.1	V
Operating Temperature Range at Package Base	Ts	0		70	•

6. ELECTRICAL CHARACTERISTICS

6-1 DC CHARACTERISTICS

VDD=2V•}0.1V, VB=2V•}0.1V, Ts = 0•`70•

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Dissipation	P				4.0	W
High-level Output Voltage	VOH	50 ƒ ¶Load	0.85		1.3	V
Low-level Output Voltage	VOL	50 ƒ ¶Load	0.0		0.3	V
Output Voltage Swing	VOS	50 ƒ ¶Load	0.7		1.2	Vpp
Clock Input Voltage Swing	VIC		0.5		0.9	Vpp
High-level Data Input Voltage	VIDH		0.8		1.3	V
Low-level Data Input Voltage	VIDL		0		0.3	V

6-2. AC CHARACTERISTICS

VDD=2V±0.1V, VB=2V±0.1V, Ts=0~70

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum Operating Clock Frequency	fo		5	---	---	GHz
Set-up time (D to CK)	t_{DS}	fo=5GHz	-55	-45	-30	ps
Hold time (1/8CK to Data)	t_{DH}	fo=5GHz	70	80	95	ps
CK-D Phase Margin	t_M	fo=5GHz	145	160		ps
1/8CK to Valid Data Delay	tr	fo=5GHz	-70	-10	50	ps

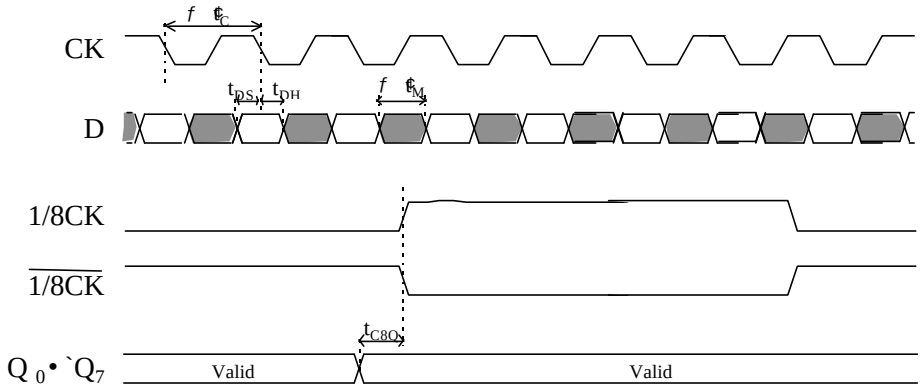


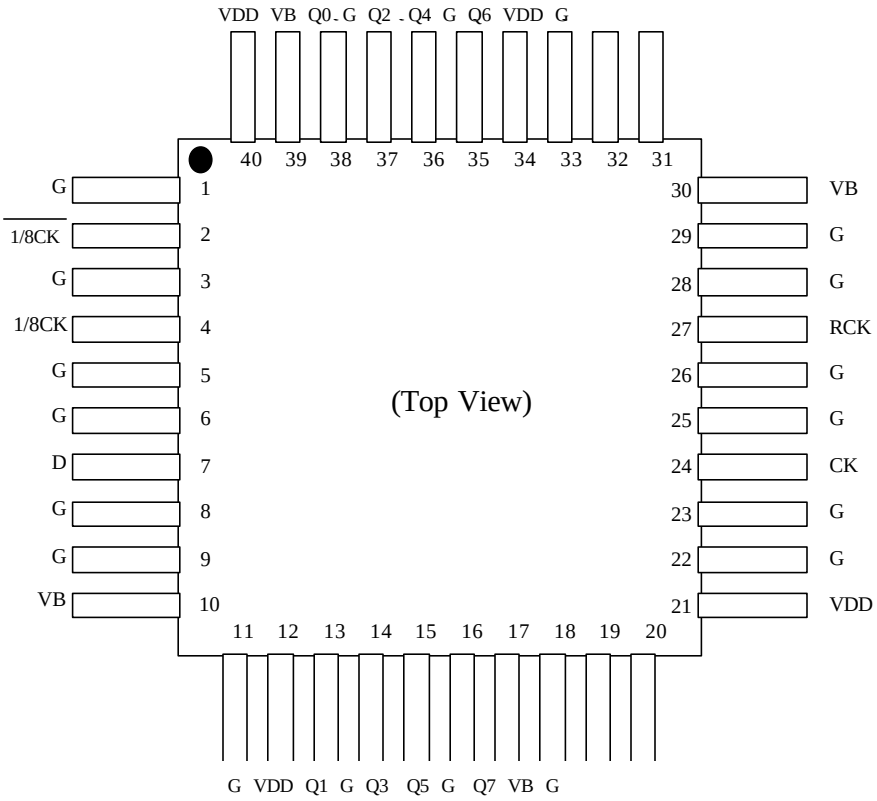
Figure 3 Waveforms of KGL4224

fo=1/Δtc

7. DEVICE ACCEPT/REJECT CRITERIA

Each device must meet all parameters listed in Paragraph 6. A device is rejected if it fails to meet one or any combination of parameters.

8. PIN ARRANGEMENT



Note: 1. G is a ground terminal.
2 . RCK is a clock reference terminal. Usually RCK is connected to ground through a capacitor (100nF).

Figure 4 PIN Arrangement of KGL4224

9. PACKAGE DIMENSIONS

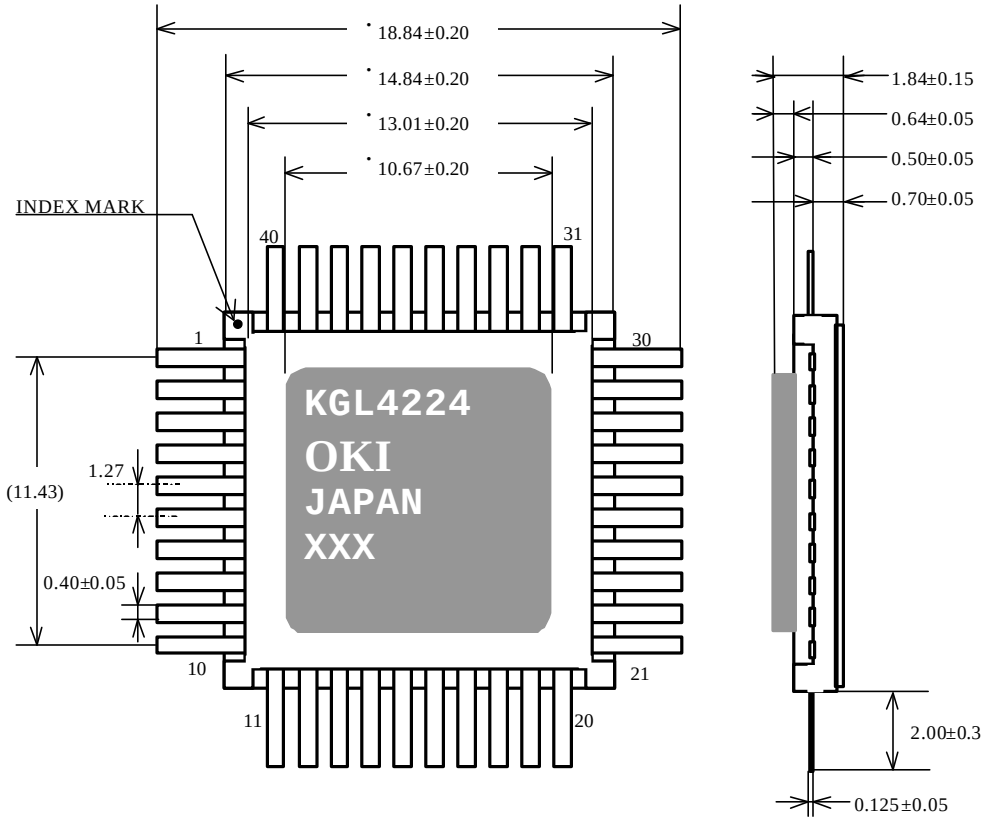


Figure 5 Dimensions of KGL4224

Unit : mm

10. TYPICAL INTERFACE CONFIGURATION

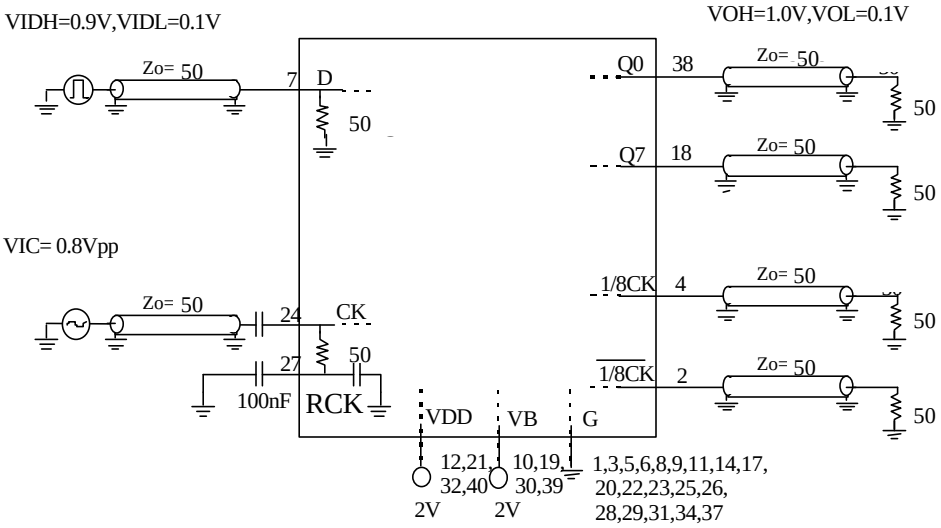


Figure 6 Typical Interfacing Configuration of KGL4224