

8M-Bit (1Mx8 /512Kx16) CMOS MASK ROM

FEATURES

- Switchable organization
1,048,576 x 8(byte mode)
524,288 x 16(word mode)
- Fast access time
Random Access : 100ns(Max.)
Page Access : 30ns(Max.)
- 4 Words / 8 bytes page access
- Supply voltage : single +5V
- Current consumption
Operating : 80mA(Max.)
Standby : 50μA(Max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
-. KM23C8105D : 42-DIP-600
-. KM23C8105DG : 44-SOP-600

GENERAL DESCRIPTION

The KM23C8105D(G) is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 1,048,576 x 8 bit(byte mode) or as 524,288 x 16 bit(word mode) depending on BHE voltage level.(See mode selection table)

This device includes page read mode function, page read mode allows 4 words (or 8bytes) of data to read fast in the same page, $\overline{CE}$ and $A_2 \sim A_{18}$ should not be changed.

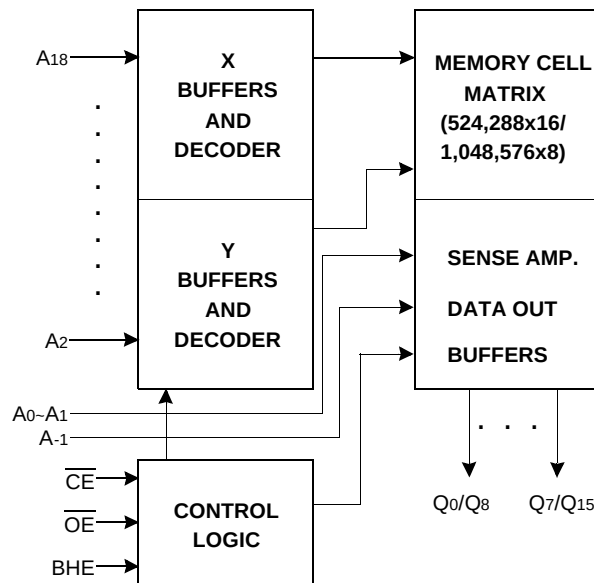
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

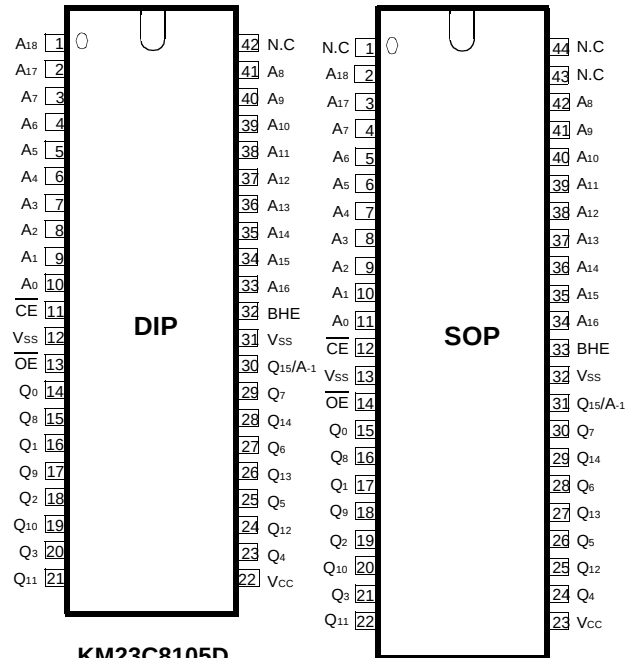
The KM23C8105D is packaged in a 42-DIP and the KM23C8105DG in a 44-SOP.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A0 - A1	Page Address Inputs
A2- A18	Address Inputs
Q0 - Q14	Data Outputs
Q15 /A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

PIN CONFIGURATION



KM23C8105D

KM23C8105DG

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN}	-0.3 to +7.0	V
Temperature Under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I _{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, all outputs open	-	80	mA
Standby Current(TTL)	I _{SB1}	$\overline{CE}=V_{IH}$, all outputs open	-	1	mA
Standby Current(CMOS)	I _{SB2}	$\overline{CE}=V_{CC}$, all outputs open	-	50	μA
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC}	-	10	μA
Output Leakage Current	I _{LO}	V _{OUT} =0 to V _{CC}	-	10	μA
Input High Voltage, All Inputs	V _{IH}		2.2	V _{CC} +0.3	V
Input Low Voltage, All Inputs	V _{IL}		-0.3	0.8	V
Output High Voltage Level	V _{OH}	I _{OH} =-400μA	2.4	-	V
Output Low Voltage Level	V _{OL}	I _{OL} =2.1mA	-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

MODE SELECTION

CE	OE	BHE	Q15/A-1	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q0~Q15 : Dout	Active
		L	Input	Operating	Q0~Q7 : Dout Q8~Q14 : Hi-Z	Active

CAPACITANCE(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	12	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS($T_A=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L=100\text{pF}$

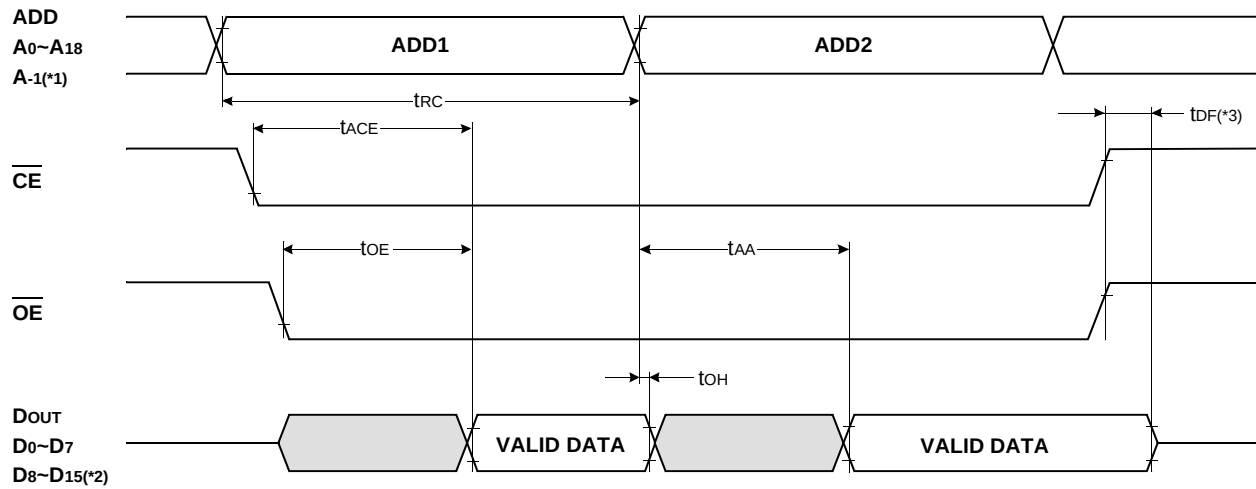
READ CYCLE

Item	Symbol	KM23C8105D(G)-10		KM23C8105D(G)-12		KM23C8105D(G)-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	100		120		150		ns
Chip Enable Access Time	t _{ACE}		100		120		150	ns
Address Access Time	t _{AA}		100		120		150	ns
Page Address Access Time	t _{PA}		30		50		70	ns
Output Enable Access Time	t _{OE}		30		50		70	ns
Output or Chip Disable to Output High-Z	t _{DF}		20		20		30	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns

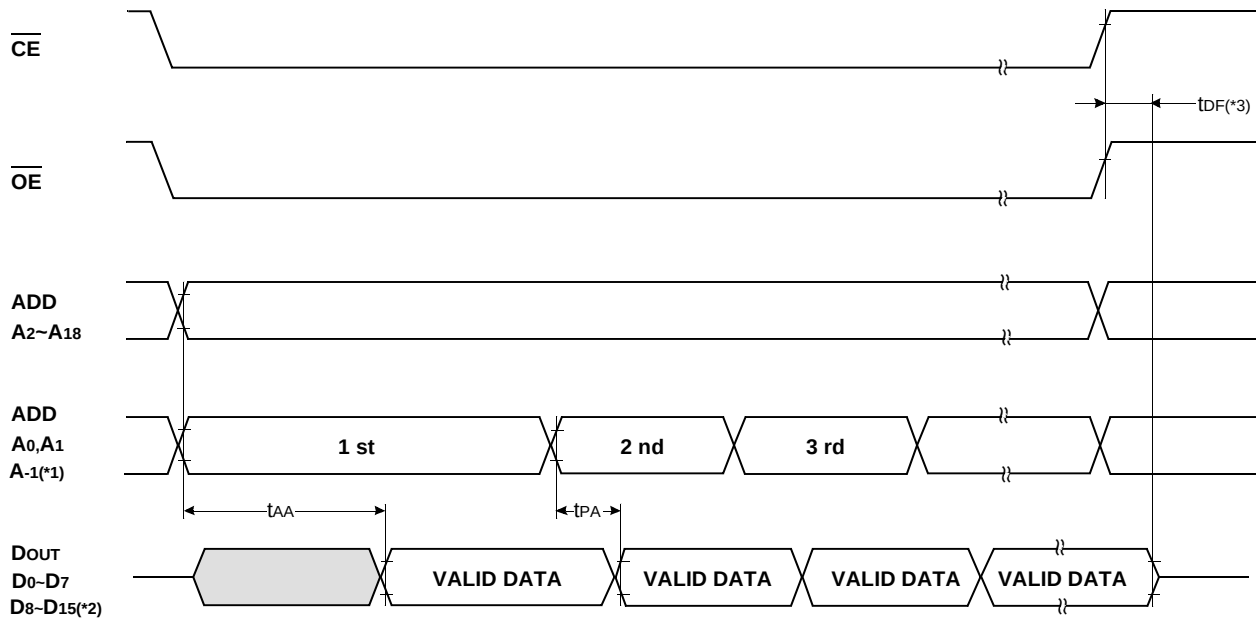
NOTE : Page Address is determined as below.Word mode ($BHE = V_{IH}$) : A₀, A₁Byte mode ($BHE = V_{IL}$) : A-1, A₀, A₁

TIMING DIAGRAM

READ



PAGE READ



NOTES :

*1. Byte Mode only. A-1 is Least Significant Bit Address.(BHE = V_{IL})

*2. Word Mode only.(BHE = V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.

CMOS MASK ROM

(Unit : mm/inch)

[illegible]

44-SOP-600

Top View Dimensions:

- Pin 1 to Pin 22: 28.95 ± 0.20 MAX
- Pin 1 to Pin 23: 28.50 ± 0.20
- Pin 1 to Pin 24: 1.122 ± 0.008
- Pin 22 to Pin 23: 1.140
- Pin 23 to Pin 24: 0.110 ± 0.008
- Pin 24 to Pin 25: 3.10 MAX
- Pin 25 to Pin 26: 0.122
- Pin 26 to Pin 27: 0.05 MIN
- Pin 27 to Pin 28: 0.002
- Pin 28 to Pin 29: 0.016 ± 0.004
- Pin 29 to Pin 30: 0.050
- Pin 30 to Pin 31: 0.016 ± 0.004
- Pin 31 to Pin 32: 0.050
- Pin 32 to Pin 33: 0.016 ± 0.004
- Pin 33 to Pin 34: 0.050
- Pin 34 to Pin 35: 0.016 ± 0.004
- Pin 35 to Pin 36: 0.050
- Pin 36 to Pin 37: 0.016 ± 0.004
- Pin 37 to Pin 38: 0.050
- Pin 38 to Pin 39: 0.016 ± 0.004
- Pin 39 to Pin 40: 0.050
- Pin 40 to Pin 41: 0.016 ± 0.004
- Pin 41 to Pin 42: 0.050
- Pin 42 to Pin 43: 0.016 ± 0.004
- Pin 43 to Pin 44: 0.050
- Pin 44 to Pin 45: 0.016 ± 0.004
- Pin 45 to Pin 46: 0.050
- Pin 46 to Pin 47: 0.016 ± 0.004
- Pin 47 to Pin 48: 0.050
- Pin 48 to Pin 49: 0.016 ± 0.004
- Pin 49 to Pin 50: 0.050
- Pin 50 to Pin 51: 0.016 ± 0.004
- Pin 51 to Pin 52: 0.050
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- Pin 130 to Pin 131: 0.016 ± 0.004
- Pin 131 to Pin 132: 0.050
- Pin 132 to Pin 133: 0.016 ± 0.004
- Pin 133 to Pin 134: 0.050
- Pin 134 to Pin 135: 0.016 ± 0.004
- Pin 135 to Pin 136: 0.050
- Pin 136 to Pin 137: 0.016 ± 0.004
- Pin 137 to Pin 138: 0.050
- Pin 138 to Pin 139: 0.016 ± 0.004
- Pin 139 to Pin 140: 0.050
- Pin 140 to Pin 141: 0.016 ± 0.004
- Pin 141 to Pin 142: 0.050
- Pin 142 to Pin 143: 0.016 ± 0.004
- Pin 143 to Pin 144: 0.050
- Pin 144 to Pin 145: 0.016 ± 0.004
- Pin 145 to Pin 146: 0.050
- Pin 146 to Pin 147: 0.016 ± 0.004
- Pin 147 to Pin 148: 0.050
- Pin 148 to Pin 149: 0.016 ± 0.004
- Pin 149 to Pin 150: 0.050
- Pin 15