64M-Bit (4Mx16 /2Mx32) CMOS MASK ROM

FEATURES

- Switchable organization
  4,194,304 x 16(word mode)
  2,097,152 x 32(double word mode)
- Fast access time
  Random Access/Page Access
  3.3V Operation : 100/30ns(Max.)
  3.0V Operation : 120/40ns(Max.)
  4 double Words / 8 Words page access
- Supply voltage : single +3.0V/ single +3.3V
- Current consumption
  Operating : 60mA(Max.)
  Standby : 30µA(Max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
  -. KM23V64205ASG : 70-SSOP-500

GENERAL DESCRIPTION

The KM23V64205ASG is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304 x 16 bit(word mode) or as 2,097,152 x 32 bit(double word mode) depending on WORD voltage level.(See mode selection table)

This device includes page read mode function, page read mode allows 4 double words (or 8 words) of data to read fast in the same page, $\overline{CE}$ and A_2 ~ A_{20} should not be changed.

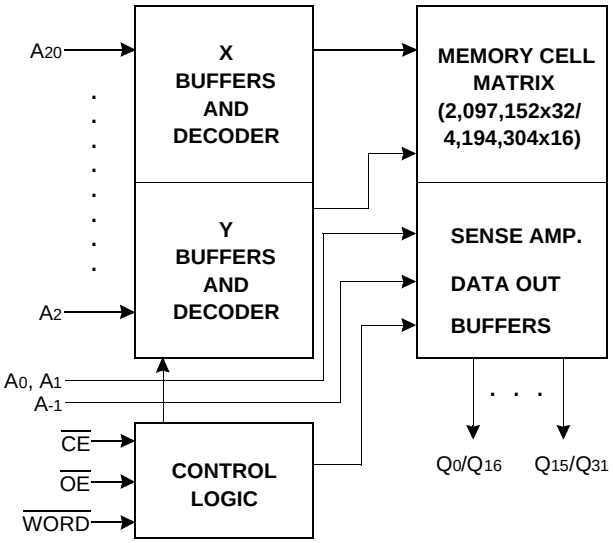
This device operates with 3.0V or 3.3V power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

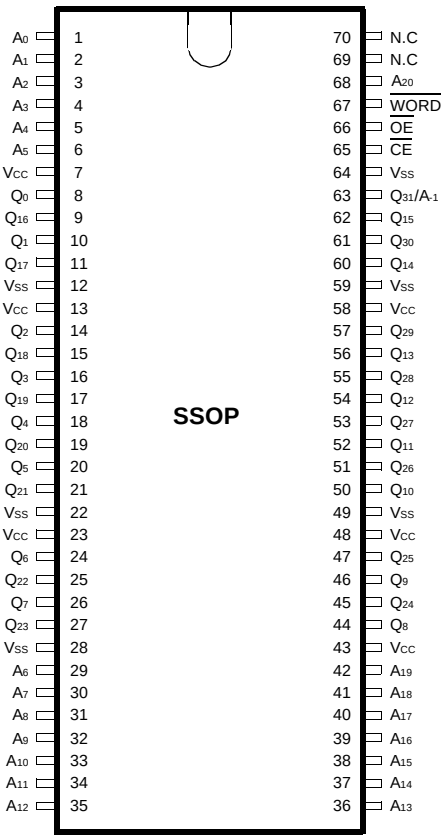
The KM23V64205ASG is packaged in a 70-SSOP.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0 - A_1	Page Address Inputs
A_2 - A_{20}	Address Inputs
Q_0 - Q_{30}	Data Outputs
Q_{31} /A_{-1}	Output 31(Double word mode)/ LSB Address(Word mode)
$\overline{WORD}$	Double word/Word mode selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
V_{SS}	Ground
N.C	No Connection

PIN CONFIGURATION



KM23V64205ASG

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	-0.3 to +4.5	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7/3.0	3.0/3.3	3.3/3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$=$\overline{OE}$=V_{IL}, all outputs open	V_{CC}=3.3V±0.3V	-	60	mA
			V_{CC}=3.0V±0.3V		50	mA
Standby Current(TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all outputs open			500	µA
Standby Current(CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}, all outputs open			30	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		-	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}		-	10	µA
Input High Voltage, All Inputs	V_{IH}			2.0	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}			-0.3	0.6	V
Output High Voltage Level	V_{OH}	I_{OH}=-400µA		2.4	-	V
Output Low Voltage Level	V_{OL}	I_{OL}=2.1mA		-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WORD}$	Q_{31}/A_{-1}	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q_0~Q_{31}:Dout	Active
		L	Input	Operating	Q_0~Q_{15} : Dout Q_{16}~Q_{30} : Hi-Z	Active

CAPACITANCE(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0°C to 70°C, V_{CC}=3.3V/3.0V±0.3V, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	1.5V
Output Loads	1 TTL Gate and C_L=100pF

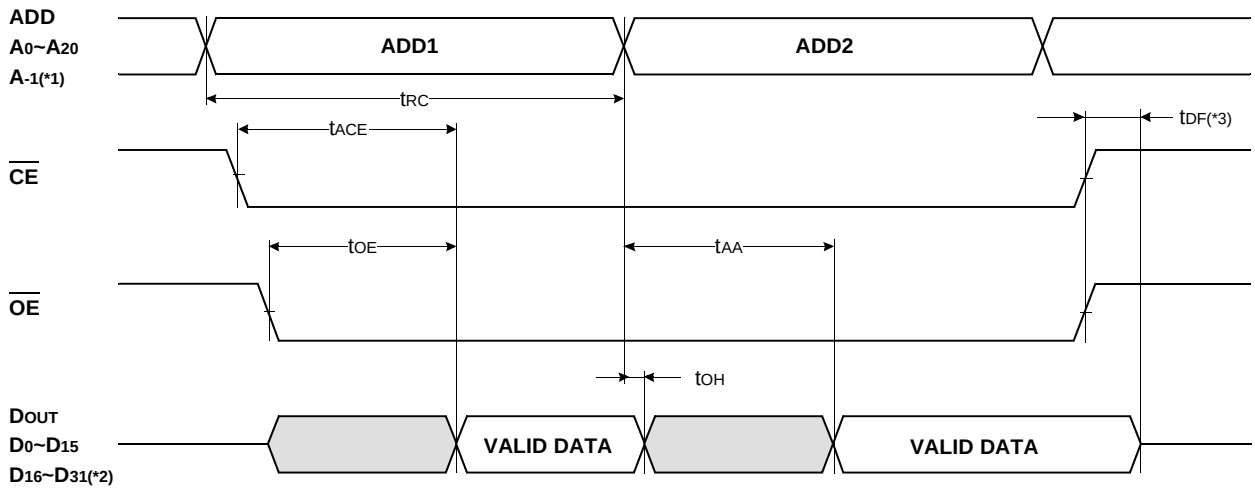
READ CYCLE

Item	Symbol	Vcc=3.3V±0.3V		Vcc=3.0V±0.3V		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		ns
Chip Enable Access Time	t_{ACE}		100		120	ns
Address Access Time	t_{AA}		100		120	ns
Page Address Access Time	t_{PA}		30		40	ns
Output Enable Access Time	t_{OE}		30		40	ns
Output or Chip Disable to Output High-Z	t_{DF}		20		20	ns
Output Hold from Address Change	t_{OH}	0		0		ns

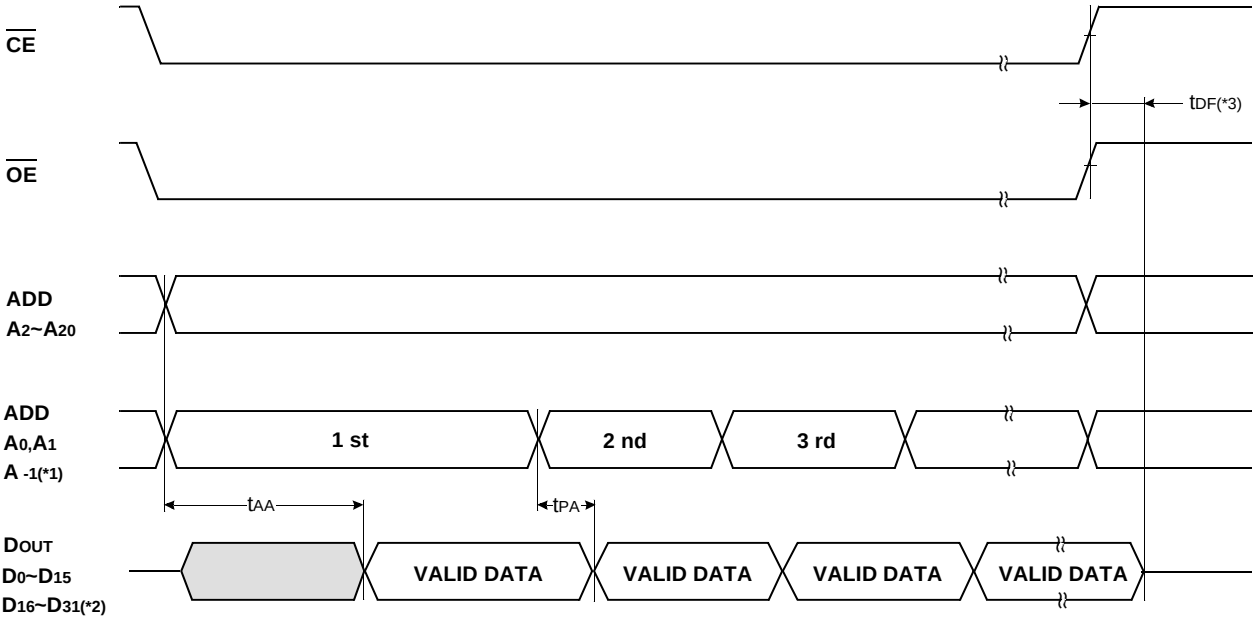
NOTE : Page Address is determined as below.
Double Word mode (WORD=V_{IH}) : A_0, A_1
Word mode (WORD=V_{IL}) : A_{-1}, A_0, A_1

TIMING DIAGRAM

READ



PAGE READ



NOTES :

*1. Word Mode only. A_{-1} is Least Significant Bit Address.($\overline{WORD}$ = V_{IL})

*2. Double Word Mode only.($\overline{WORD}$ = V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.

PACKAGE DIMENSIONS

(Unit : mm/inch)

70-SSOP-500