

64M-Bit (8Mx8 /4Mx16) CMOS MASK ROM

FEATURES

- Switchable organization
8,388,608 x 8(byte mode)
4,194,304 x 16(word mode)
- Fast access Time ($C_L=30\text{pF}$)
Random Access Time/Page Access Time : 100/30ns(max.)
- Supply voltage
Vcc : single +3.3V/ single +3.0V
Vccq : single +1.8V
- 8 words/16 bytes page access
- Temperature : 0°C ~ +70°C
- Current consumption
Operating(Icc) : 60mA (max)
Standby(ISB2) : 50uA (max)
- Fully static operation
- All inputs and outputs TTL compatible
- Package
K3P7P(Q)1000B-FC : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The K3P7P(Q)1000B-FC is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 8,388,608 x 8 bit(byte mode) or as 4,194,304 x 16 bit(word mode) depending on BHE voltage level. This device includes page read mode function, page read mode allows 8 words (or 16 bytes) of data to be read fast in the same page, $\overline{CE}$ and A3 ~ A21 should not be changed.

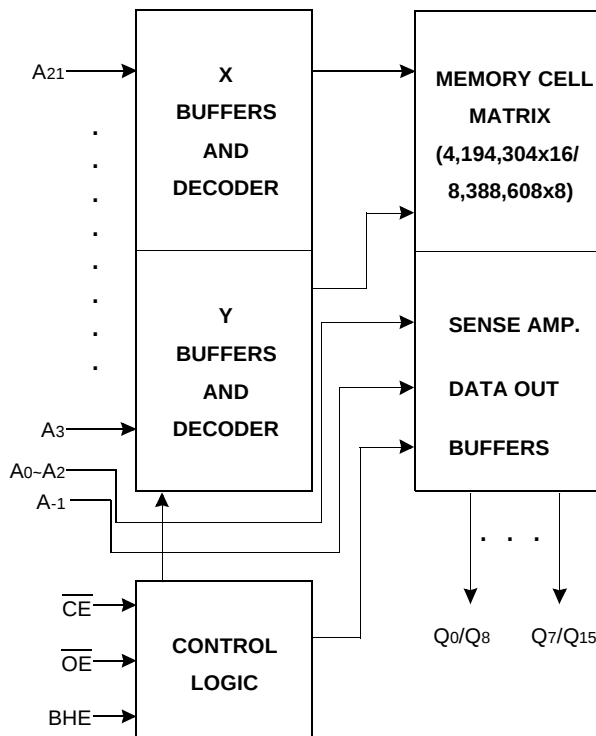
This device operates with 3.0V or 3.3V power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and operating system and/or application software storage for hand-held application.

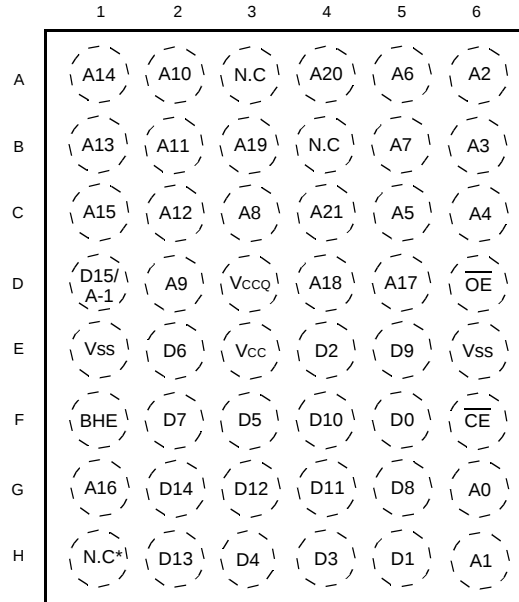
The K3P7P(Q)1000B-FC is packaged in a 48-CSP with 0.75mm ball pitch and 6x8 ball array.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A0 - A2	Page Address Inputs
A3 - A21	Address Inputs
Q0 - Q14	Data Outputs
Q15 /A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
Vcc	Power
Vccq	Data Output Power (+1.8V)
Vss	Ground
NC	No Connection

48FP-BGA PIN CONFIGURATION (TOP VIEW)



Note : See last page for package dimension.
N.C* : will be MSB Address for the 128Mbit.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN}	-0.3 to +4.5	V
Temperature Under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature	T _{Stg}	-55 to +150	°C
Operating Temperature	T _A	0 to +70	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	2.7/3.0	3.0/3.3	3.3/3.6	V
Supply Voltage	V _{CCQ}	1.6	1.8	2.0	V
Supply Voltage	V _{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I _{CC}	$\overline{CE}=\overline{OE}=V_{IL}$, all outputs open	-	60	mA
Standby Current	TTL Level	$\overline{CE}=V_{IH}$, all outputs open	-	500	uA
	CMOS Level	$\overline{CE}=V_{CC}$, all outputs open	-	50	uA
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC}	-	10	uA
Output Leakage Current	I _{LO}	V _{OUT} =0 to V _{CC}	-	10	uA
Input High Voltage, All Inputs	V _{IH}		1.3	V _{CC} +0.3	V
Input Low Voltage, All Inputs	V _{IL}		-0.3	0.5	V
Output High Voltage Level	V _{OH}	I _{OH} = -200uA (V _{CCQ} =1.8V)	1.4	-	V
Output Low Voltage Level	V _{OL}	I _{OL} = 2.1mA	-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{DD}+0.3V which, during transitions, may overshoot to V_{DD}+2.0V for periods <20ns.

MODE SELECTION

CE	OE	BHE	Q _{15/A-1}	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q ₀ ~Q ₁₅ : Dout	Active
		L	Input	Operating	Q ₀ ~Q ₇ : Dout Q ₈ ~Q ₁₄ : Hi-Z	Active

CAPACITANCE(T_A =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	12	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0°C to +70°C, V_{CC}=3.3V/3.0V±0.3V, V_{CCQ}=1.8V±0.2V, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	GND to V _{CCQ}
Input Rise and Fall Times	3ns
Input Timing Reference Levels	V _{CCQ} x 0.5V
Output timing Reference Levels	V _{CCQ} x 0.5V
Output Loads	1 TTL Gate and C _L =30pF

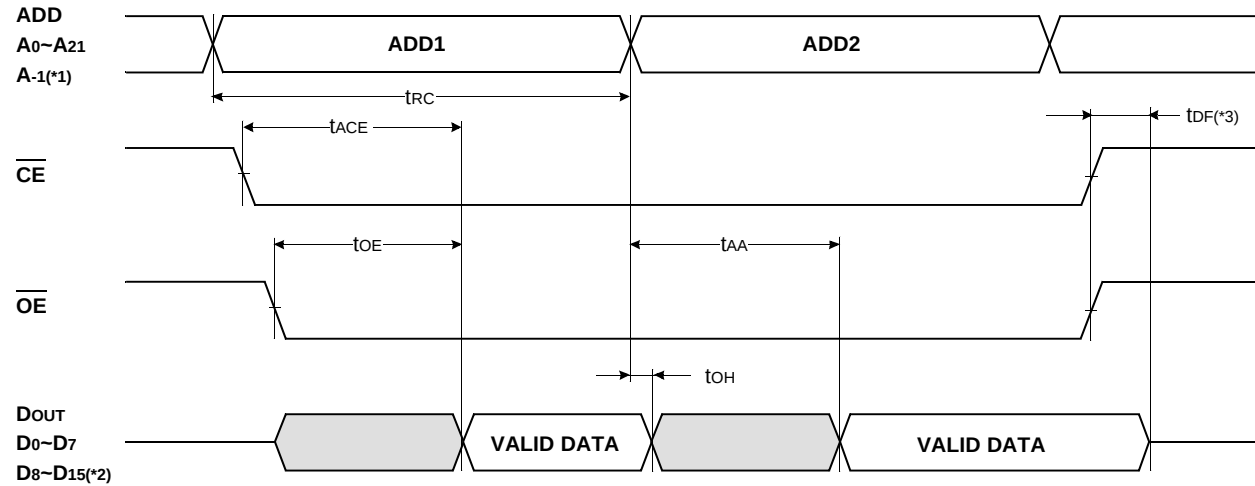
READ CYCLE ($V_{CCQ}=1.8V \pm 0.2V$, $C_L=30pF$)

Item	Symbol	K3P7P(Q)1000B-FC10		Unit
		Min	Max	
Read Cycle Time	tRC	100		ns
Chip Enable Access Time	tACE		100	ns
Address Access Time	tAA		100	ns
Page Address Access Time	tPA		30	ns
Output Enable Access Time	tOE		30	ns
Output or Chip Disable to Output High-Z	tDF		20	ns
Output Hold from Address Change	tOH	0		ns

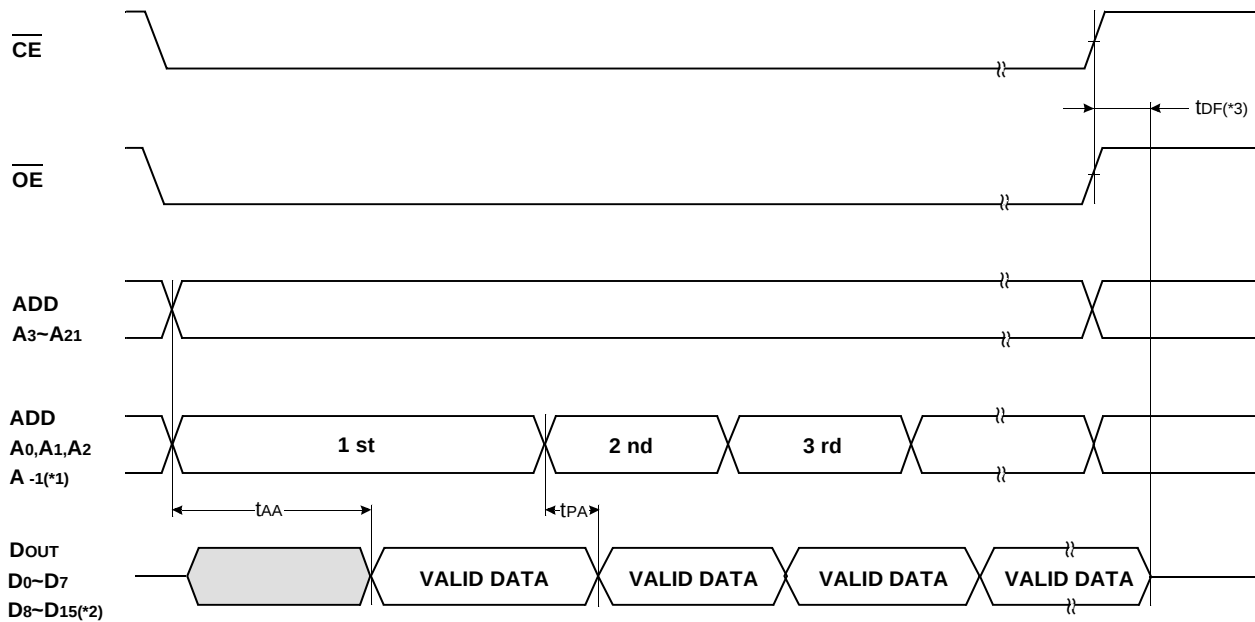
NOTE : Page Address is determined as below.Word mode (BHE= V_{IH}) : A₀, A₁, A₂Byte mode (BHE= V_{IL}) : A₋₁, A₀, A₁, A₂

TIMING DIAGRAM

READ



PAGE READ



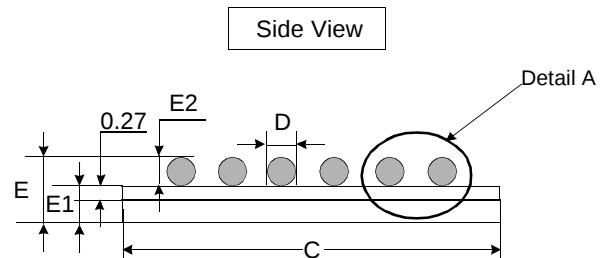
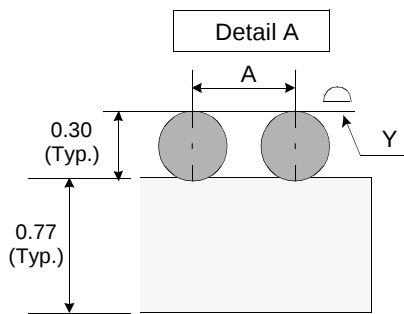
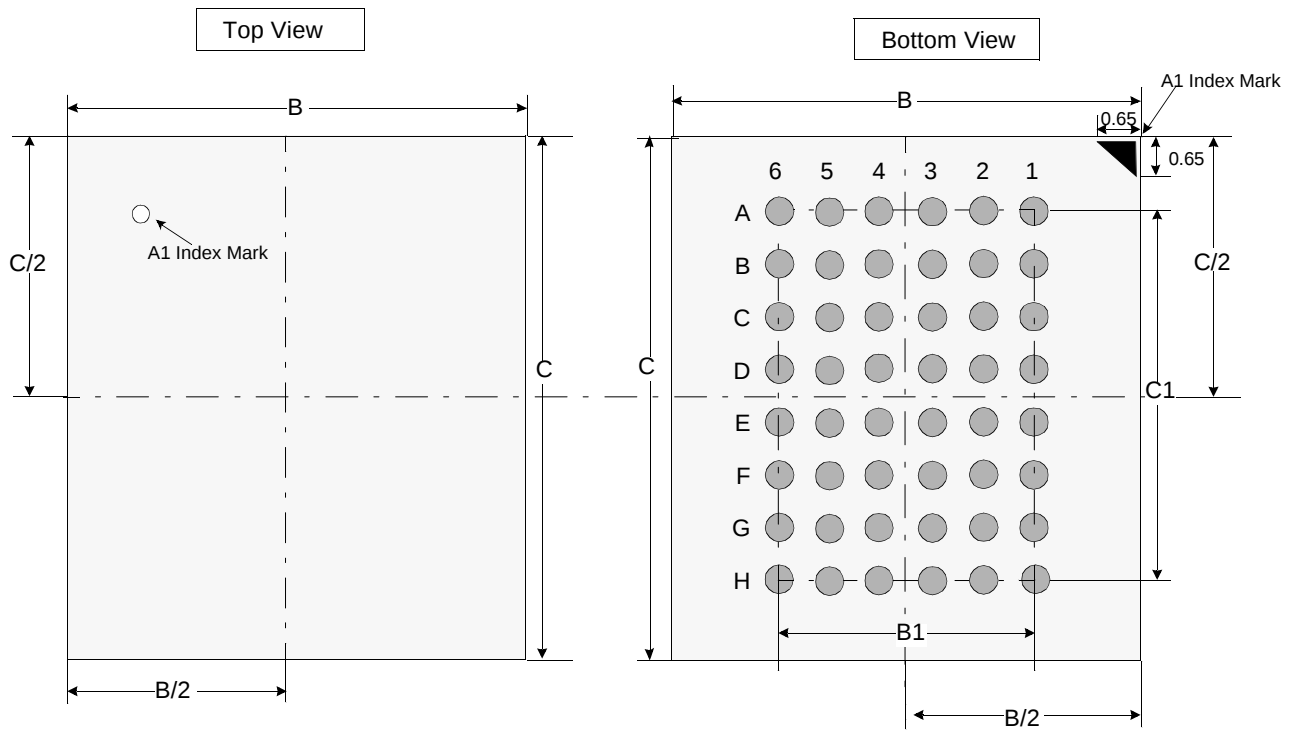
NOTES :

*1. Byte Mode only. A₋₁ is Least Significant Bit Address. (BHE = V_{IL})

*2. Word Mode only. (BHE = V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.

PACKAGE DIMENSIONS (48 FP-BGA)



(Unit : mm)

	Min	Typ.	Max
A	-	0.75	-
B	8.90	9.00	9.10
B1	-	3.75	-
C	8.90	9.00	9.10
C1	-	5.25	-
D	0.35	0.40	0.45
E	1.00	1.10	1.20
E1	0.72	0.77	0.82
E2	0.25	0.30	0.35
Y	-	-	0.08

Notes.

1. Bump counts : 48 (6 x 8 Array)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(max)