

Document Title

512Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial Draft	December 3, 1998	Preliminary
1.0	Finalize	April 28, 1999	Final

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512K×8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 512K×8
- Power Supply Voltage
K6T4008V2C Family: 3.0~3.6V
K6T4008U2C Family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 48(36)-uBGA-6.10x8.90

GENERAL DESCRIPTION

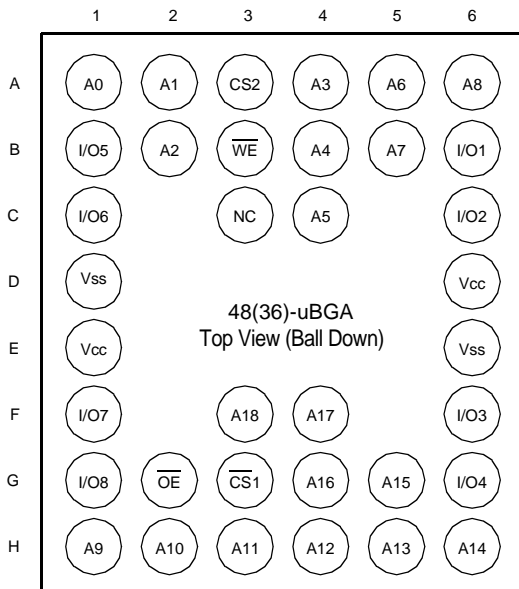
The K6T4008V2C and K6T4008U2C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature range and have chip scale package type for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
K6T4008V2C-F	Industrial(-40~85°C)	3.0~3.6V	70 ¹⁾ /85ns	20μA	30mA	48(36)-uBGA
K6T4008U2C-F		2.7~3.3V	70 ¹⁾ /85/100ns			

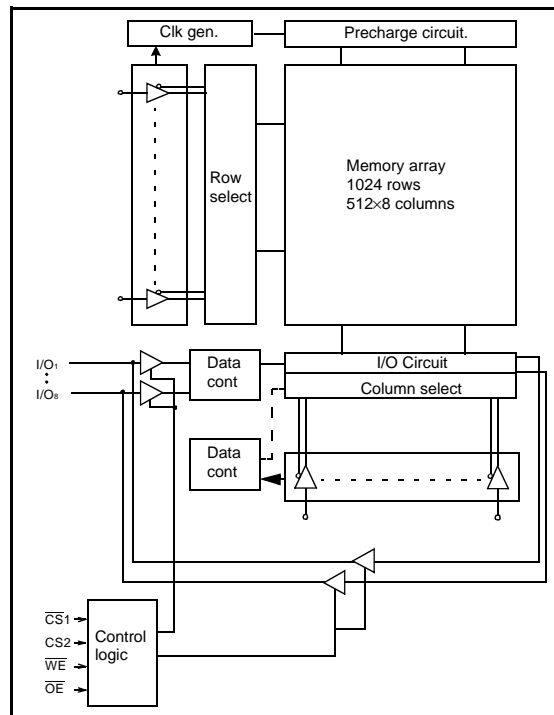
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	I/O1~I/O8	Data Inputs/Outputs
\overline{WE}	Write Enable Input	Vcc	Power
\overline{OE}	Output Enable Input	Vss	Ground
A0~A18	Address Inputs	NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temp Products(-40~85°C)	
Part Name	Function
K6T4008V2C-ZF70	48-uBGA, 70ns, 3.3V, LL
K6T4008V2C-ZF85	48-uBGA, 85ns, 3.3V, LL
K6T4008U2C-ZF70	48-uBGA, 70ns, 3.0V, LL
K6T4008U2C-ZF85	48-uBGA, 85ns, 3.0V, LL
K6T4008U2C-ZF10	48-uBGA, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	-40 to 85	°C	K6T4008V2C-P, K6T4008U2C-P

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T4008V2C Family K6T4008U2C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6T4008V2C, K6T4008U2C Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	K6T4008V2C, K6T4008U2C Family	-0.3 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified2. Overshoot: V_{CC}+2.0V in case of pulse width ≤ 30ns

3. Undershoot: -2.0V in case of pulse width ≤ 30ns

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $\overline{CS}_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, $\overline{CS}_2=V_{IH}$, $\overline{WE}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	4	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS}_1 \leq 0.2V$, $\overline{CS}_2 \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, $\overline{CS}_2=V_{IH}$, V _{IN} =V _{IH} or V _{IL}	-	-	30	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, $\overline{CS}_2=V_{IL}$, Other inputs = V _{IL} or V _{IH}	-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, $\overline{CS}_2 \geq V_{CC}-0.2V$ or $\overline{CS}_2 \leq 0.2V$, Other inputs=0~V _{CC}	-	-	20	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V

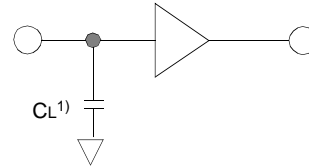
Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$

$C_L^{(1)}=30\text{pF}+1\text{TTL}$

1. 70ns products



1. Including scope and jig capacitance

AC CHARACTERISTICS (TA=-40 to 85°C, K6T4008V2C Family: 3.0~3.6V, K6T4008U2C Family: 2.7~3.3V)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO1, tCO2	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tdW	30	-	35	-	40	-	ns
	Data hold from write time	tdH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

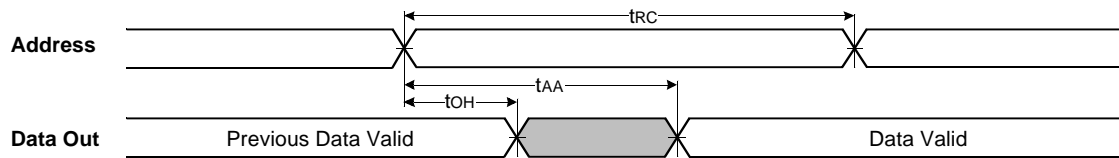
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0V, \overline{CS}_1 \geq V_{CC}-0.2V^{(1)}$	-	0.5	20	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

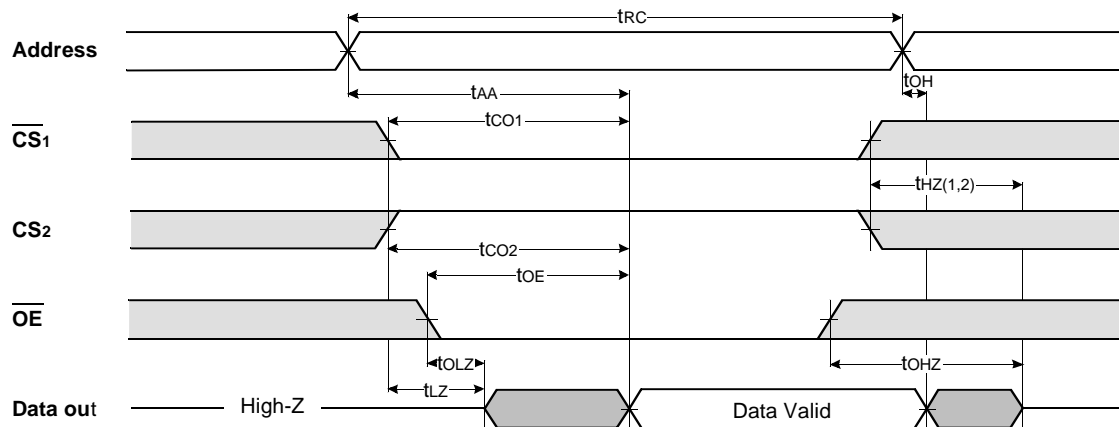
1. $\overline{CS}_1 \geq V_{CC}-0.2V$, $\overline{CS}_2 \geq V_{CC}-0.2V$ (\overline{CS}_1 controlled) or $\overline{CS}_2 \leq 0.2V$ (\overline{CS}_2 controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}=\overline{OE}=V_{IL}$, $CS_2=\overline{WE}=V_{IH}$)



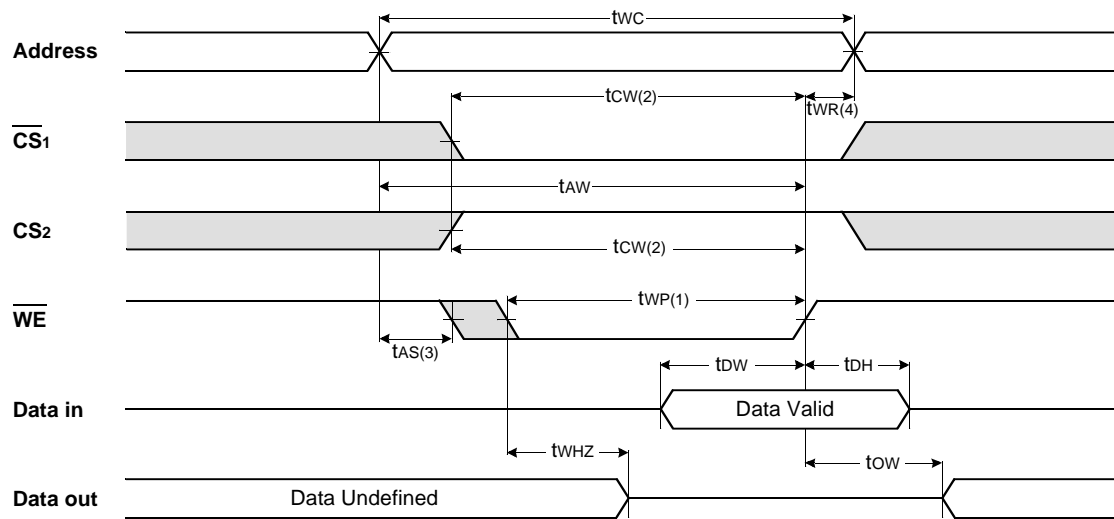
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



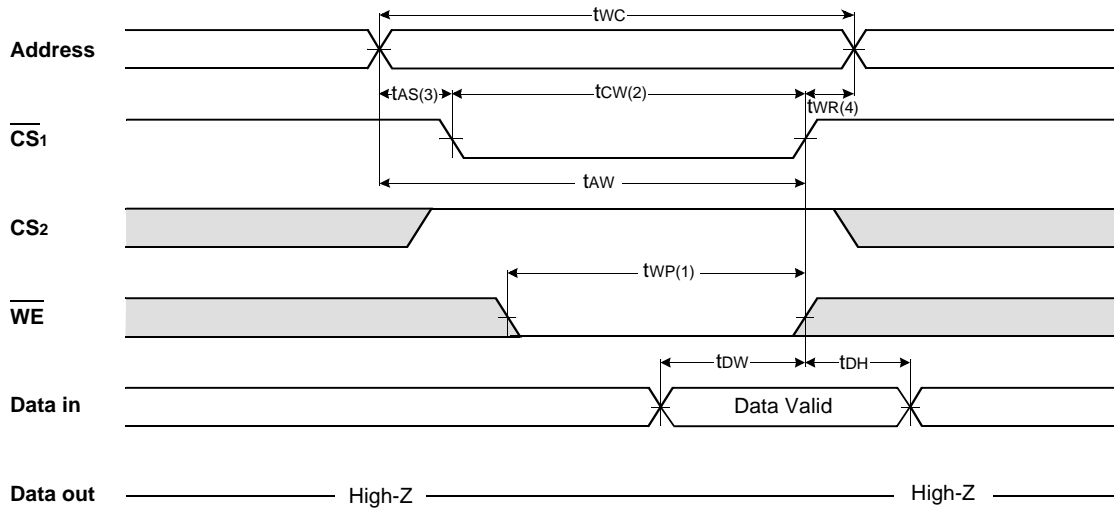
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

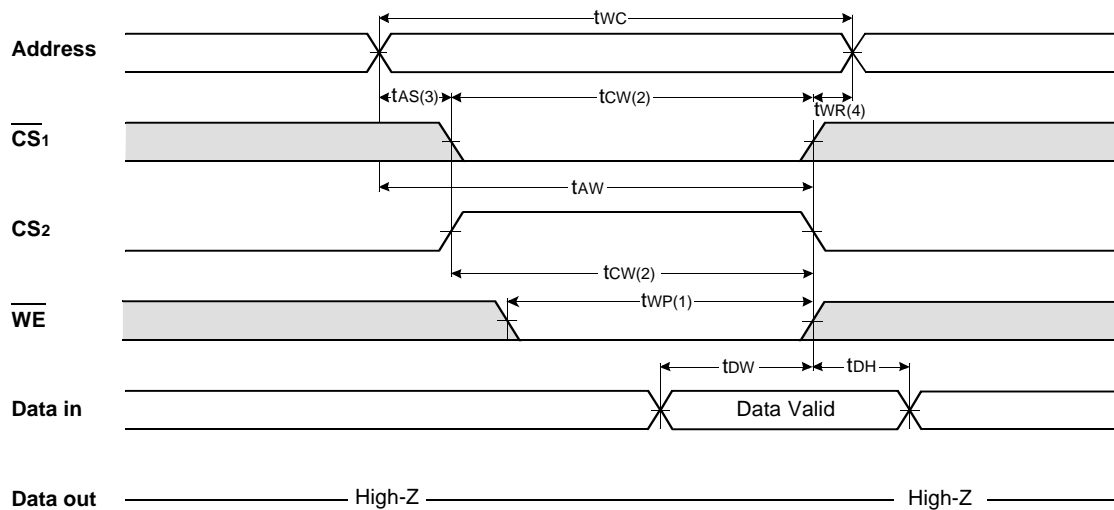
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

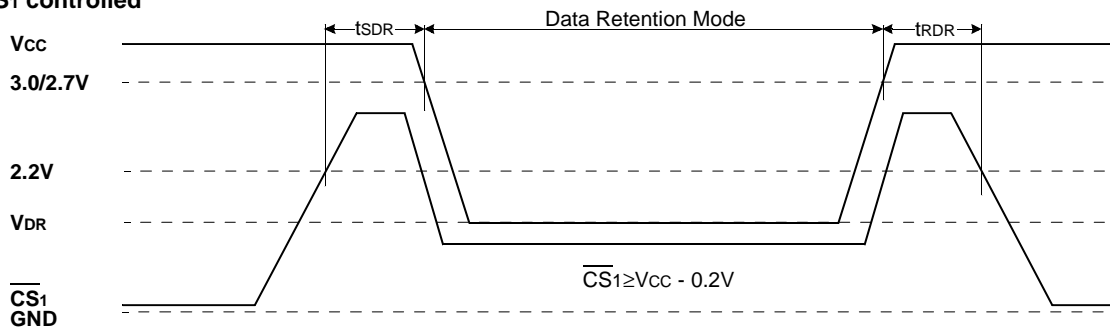


NOTES (WRITE CYCLE)

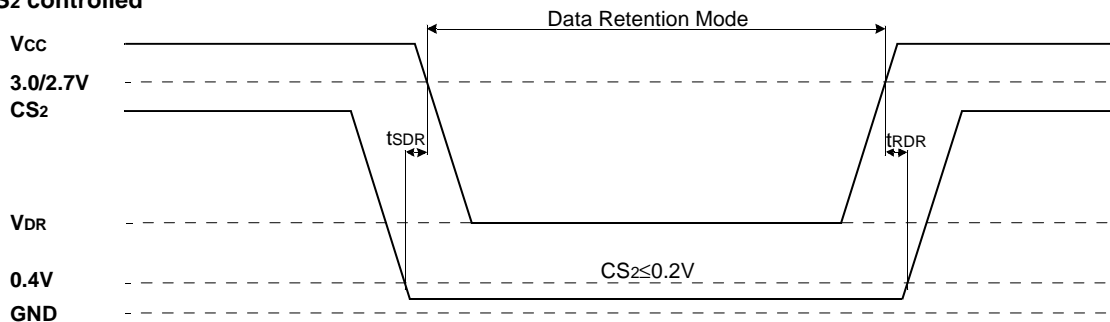
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS₂ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ going high and WE going low : A write end at the earliest transition among CS₁ going high, CS₂ going low and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS₁ going low or CS₂ going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR₁ applied in case a write ends as $\overline{CS_1}$ or \overline{WE} going high tWR₂ applied in case a write ends as CS₂ going to low.

DATA RETENTION WAVE FORM

CS₁ controlled



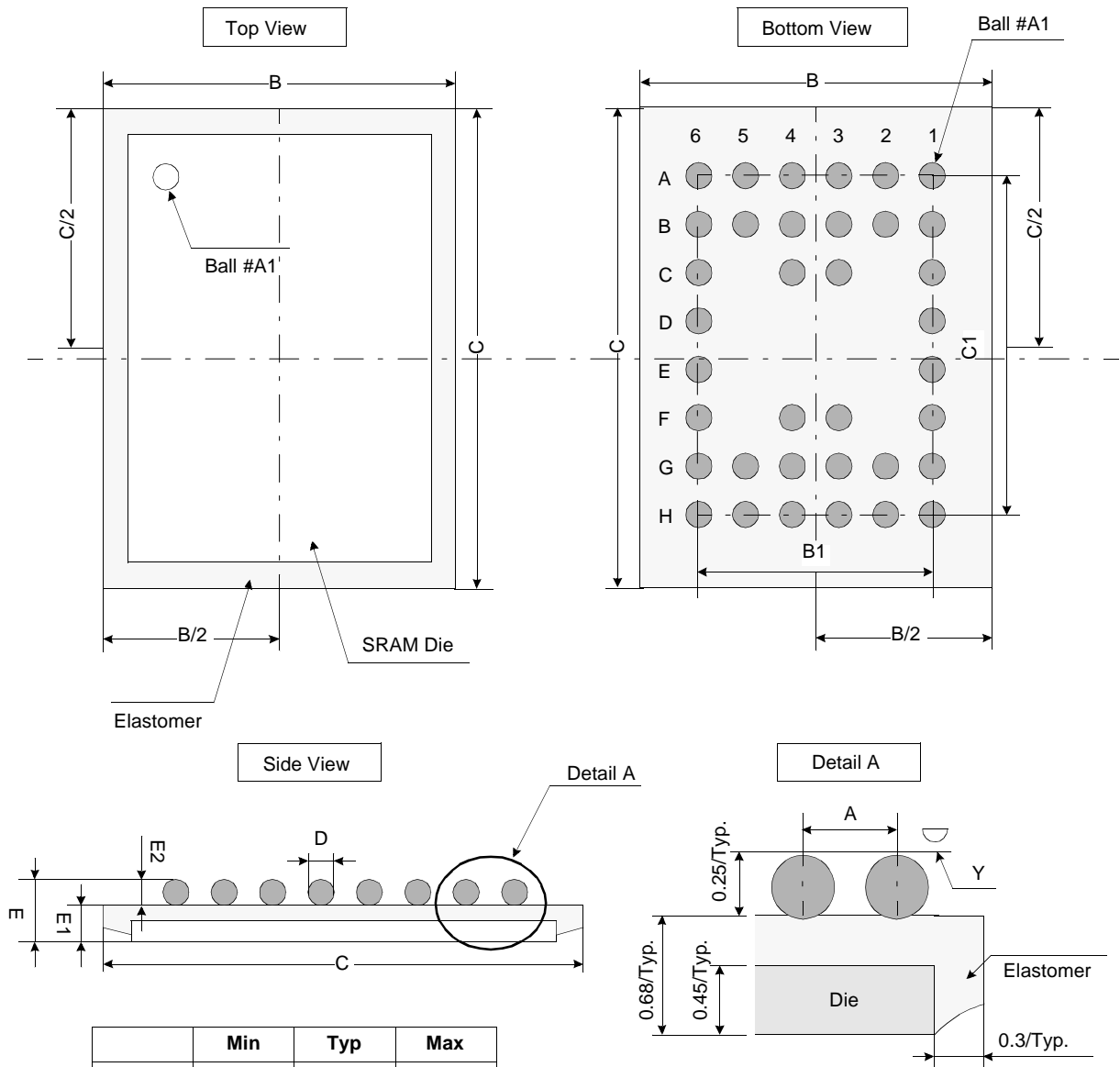
CS₂ controlled



PACKAGE DIMENSIONS

Units: millimeters

48 BALL MICRO BALL GRID ARRAY- 0.75mm ball pitch



Notes.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)