

Document Title

**512Kx8 Bit High Speed Static RAM(3.3V Operating).
 Operated at Commercial and Industrial Temperature Ranges.**

Revision History

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>																													
Rev. 0.0	Initial release with Preliminary.	Feb. 12. 1999	Preliminary																													
Rev. 1.0	1.1 Removed Low power Version. 1.2 Removed Data Retention Characteristics. 1.3 Changed I _{SB1} to 20mA	Mar. 29. 1999	Preliminary																													
Rev. 2.0	Relax D.C parameters.	Aug. 19. 1999	Preliminary																													
	<table border="1"> <thead> <tr> <th colspan="2">Item</th><th>Previous</th><th>Current</th></tr> </thead> <tbody> <tr> <td rowspan="3">I_{CC}</td><td>12ns</td><td>160mA</td><td>195mA</td></tr> <tr> <td>15ns</td><td>155mA</td><td>190mA</td></tr> <tr> <td>20ns</td><td>150mA</td><td>185mA</td></tr> </tbody> </table>	Item		Previous	Current	I _{CC}	12ns	160mA	195mA	15ns	155mA	190mA	20ns	150mA	185mA																	
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Rev. 3.0	3.1 Delete Preliminary 3.2 Update D.C parameters and 10ns part.	Mar. 27. 2000	Final																													
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Rev. 4.0	Add Low Power-Ver.	Apr. 24. 2000	Final																													

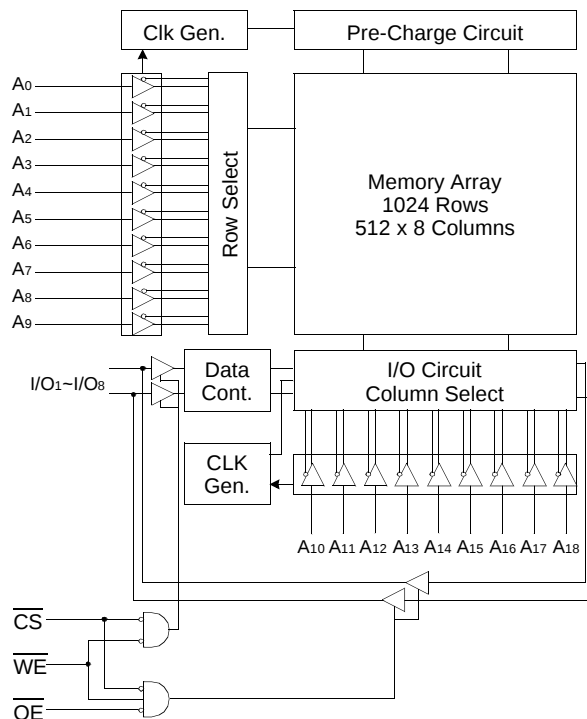
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

512K x 8 Bit High-Speed CMOS Static RAM**FEATURES**

- Fast Access Time 10,12,15,20ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 60mA(Max.)
 - (CMOS) : 10mA(Max.)
 - 1.2mA(Max.) L-Ver. only
- Operating
 - K6R4008V1C-10 : 155mA(Max.)
 - K6R4008V1C-12 : 145mA(Max.)
 - K6R4008V1C-15 : 135mA(Max.)
 - K6R4008V1C-20 : 125mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - K6R4008V1C-J : 36-SOJ-400
 - K6R4008V1C-T : 44-TSOP2-400BF

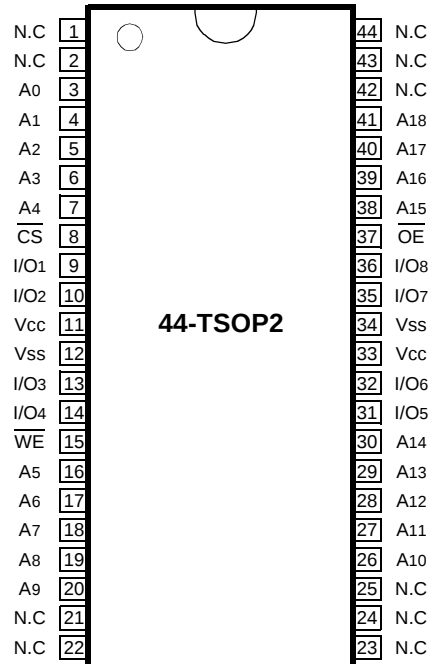
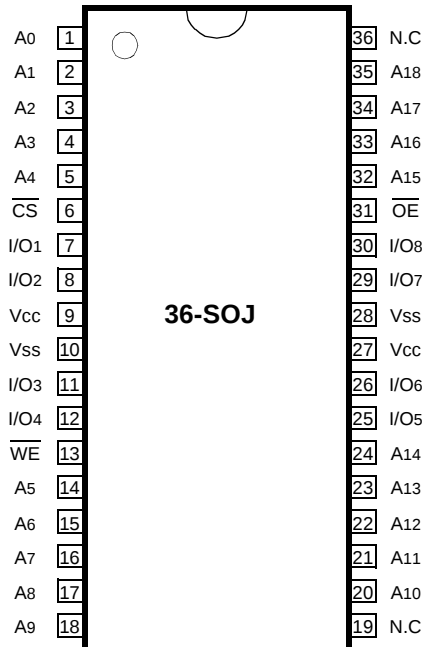
GENERAL DESCRIPTION

The K6R4008V1C is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The K6R4008V1C uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4008V1C is packaged in a 400 mil 36-pin plastic SOJ and 44-pin plastic TSOP type II.

FUNCTIONAL BLOCK DIAGRAM**ORDERING INFORMATION**

K6R4008V1C-C10/C12/C15/C20	Commercial Temp.
K6R4008V1C-I10/I12/I15/I20	Industrial Temp.

PIN CONFIGURATION (Top View)



PIN FUNCTION

RECOMMENDED DC OPERATING CONDITIONS*($T_A=0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3***	V
Input Low Voltage	V _{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS*($T_A=0$ to 70°C , V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-2	2	μA	
Output Leakage Current	I _{LO}	CS=V _{IH} or OE=V _{IH} or WE=V _{IL} V _{OUT} =V _{SS} to V _{CC}		-2	2	μA	
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	Com.	10ns	-	155	mA
				12ns	-	145	
				15ns	-	135	
				20ns	-	125	
			Ind.	10ns	-	170	
				12ns	-	160	
				15ns	-	150	
				20ns	-	140	
Standby Current	I _{SB}	Min. Cycle, CS=V _{IH}		-	60	mA	
	I _{SB1}	f=0MHz, CS≥V _{CC} -0.2V, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V					

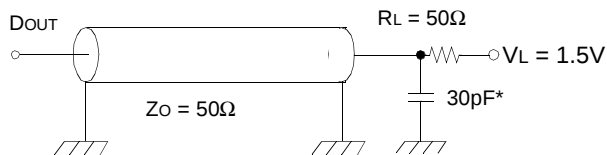
AC CHARACTERISTICS (T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise noted.)

TEST CONDITIONS*

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

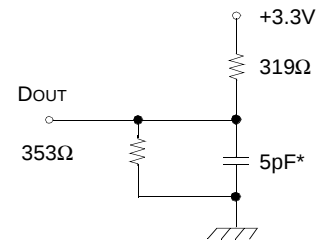
*The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

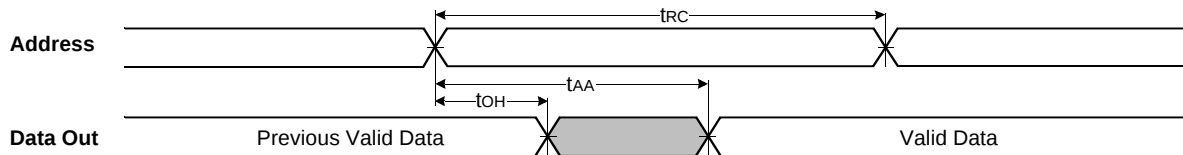
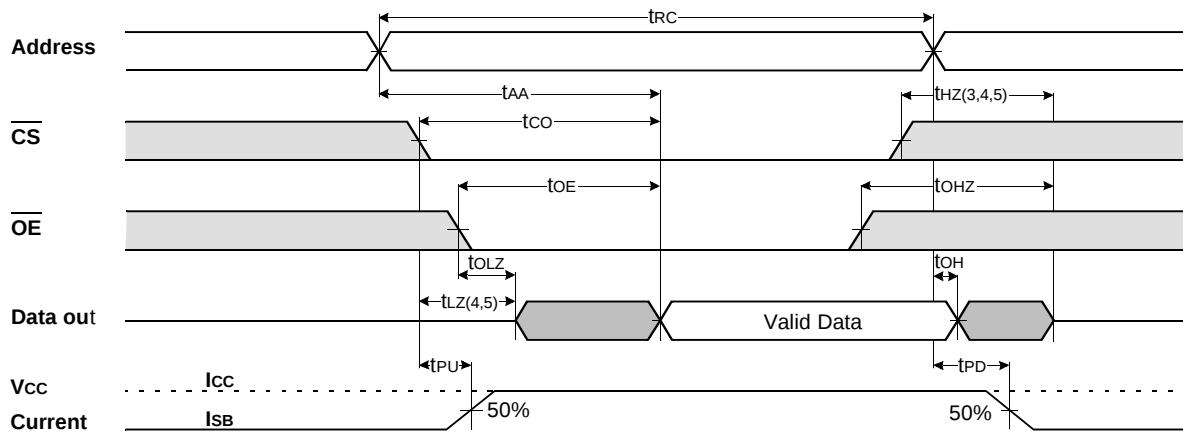
Parameter	Symbol	K6R4008V1C-10		K6R4008V1C-12		K6R4008V1C-15		K6R4008V1C-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	20	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	-	20	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	-	20	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	0	7	0	9	ns
Output Disable										

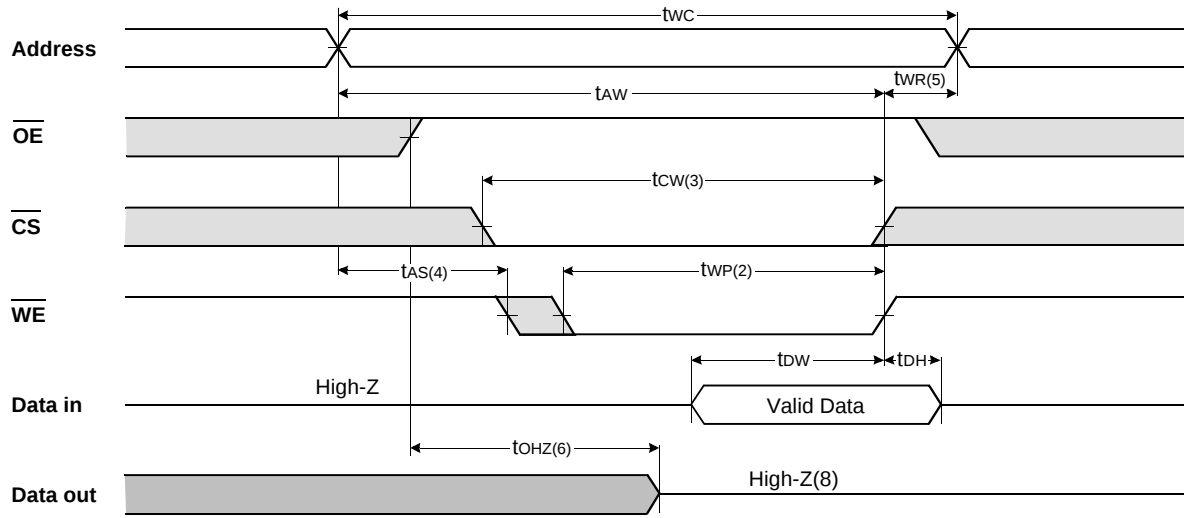
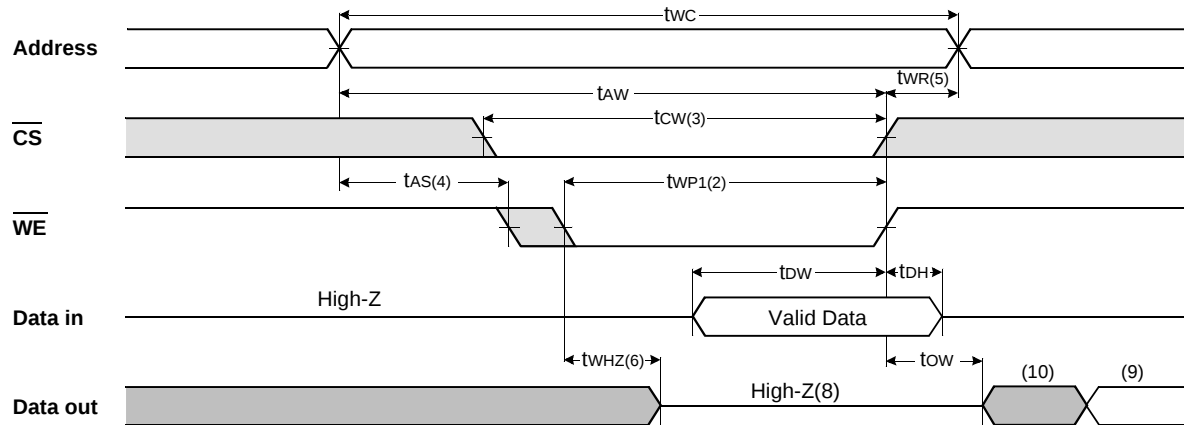
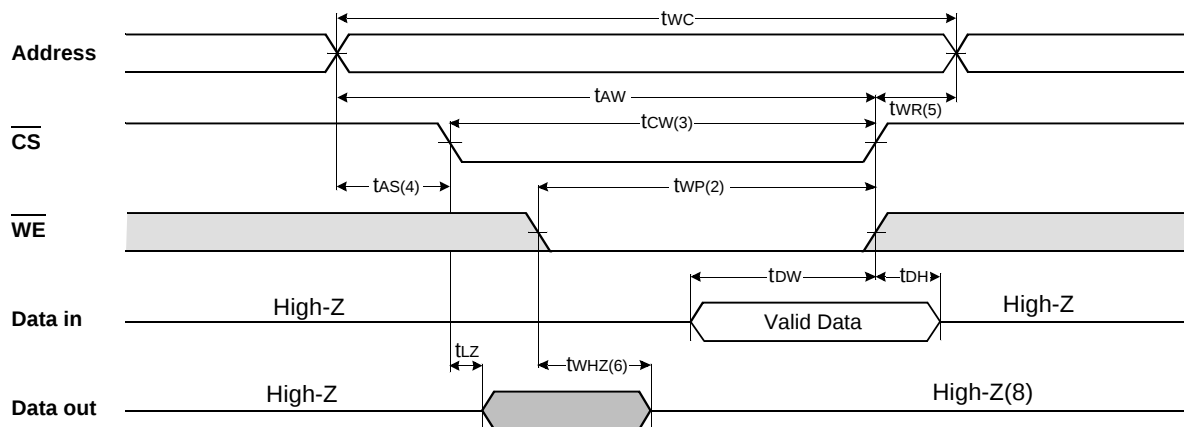
WRITE CYCLE*

Parameter	Symbol	K6R4008V1C-10		K6R4008V1C-12		K6R4008V1C-15		K6R4008V1C-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	20	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of	t _{AW}	7	-	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t _{WP}	7	-	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t _{WP1}	10	-	12	-	15	-	20	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	0	9	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	9	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	3	-	ns

* The above parameters are also guaranteed at industrial temperature range.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{OE}}$ = Clock)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{OE}}$ =Low Fixed)TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ = Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low ; A write ends at the earliest transition CS going high or WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CS or WE going high.
6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. DOUT is the read data of the new address.
10. When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	OE	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB} , I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

* X means Don't Care.

DATA RETENTION CHARACTERISTICS*($T_A=0$ to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	VDR	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
Data Retention Current	IDR	$V_{CC}=3.0V$, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	1.0	mA
		$V_{CC}=2.0V$, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled

