

Document Title

256Kx4 Bit (with OE) High-Speed CMOS Static RAM(3.3V Operating).

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>										
Rev. 0.0	Initial release with Preliminary.	Aug. 5th. 1998	Preliminary										
Rev. 1.0	Release to Final Data Sheet. 1.1. Delete Preliminary. 1.2. Relax DC characteristics.	Sep. 7th. 1998	Final										
<table border="1"> <thead> <tr> <th>Item</th> <th>Previous</th> <th>Changed</th> </tr> </thead> <tbody> <tr> <td rowspan="3">Icc</td> <td>12ns</td> <td>70mA</td> </tr> <tr> <td>15ns</td> <td>68mA</td> </tr> <tr> <td>20ns</td> <td>65mA</td> </tr> </tbody> </table>				Item	Previous	Changed	Icc	12ns	70mA	15ns	68mA	20ns	65mA
Item	Previous	Changed											
Icc	12ns	70mA											
	15ns	68mA											
	20ns	65mA											
Rev. 2.0	Add 10ns & Low Power Ver.	Apr. 24. 2000	Final										

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 4.6	V
Power Dissipation		P _d	1	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	-2	2	μA	
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC}	-2	2	μA	
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	10ns	-	75	mA
			12ns	-	70	
			15ns	-	68	
			20ns	-	65	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}=V_{IH}$	-	30	mA	
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	Normal	-		5
L-ver.			-	0.5		
Output Low Voltage Level	V _{OL}	I _{OL} =8mA	-	0.4	V	
Output High Voltage Level	V _{OH}	I _{OH} =-4mA	2.4	-	V	

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

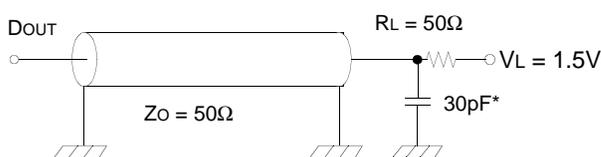
* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS (T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

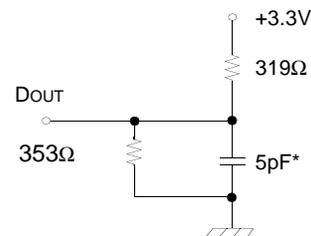
Output Loads(A)



* Capacitive Load consists of all components of the test environment.

Output Loads(B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	KM64V1003C-10		KM64V1003C-12		KM64V1003C-15		KM64V1003C-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	20	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	-	20	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	-	20	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	0	7	0	9	ns
Output Disable to High-Z Output	t _{OHZ}	0	5	0	6	0	7	0	9	ns
Output Hold from Address	t _{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection to Power Down-	t _{PD}	-	10	-	12	-	15	-	20	ns

* The above parameters are also guaranteed at industrial temperature range.

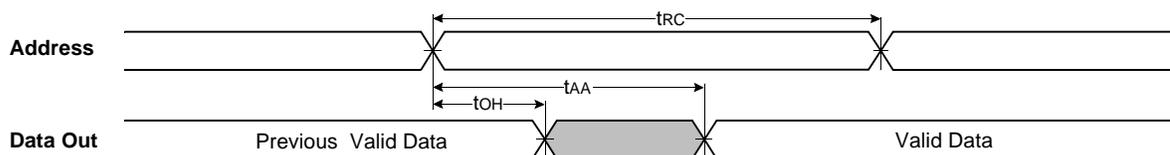
WRITE CYCLE*

Parameter	Symbol	KM64V1003C-10		KM64V1003C-12		KM64V1003C-15		KM64V1003C-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	20	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	9	-	10	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	9	-	10	-	ns
Write Pulse Width(OE High)	t _{WP}	7	-	8	-	9	-	10	-	ns
Write Pulse Width(OE Low)	t _{WP1}	10	-	12	-	15	-	20	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	0	9	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	8	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	3	-	ns

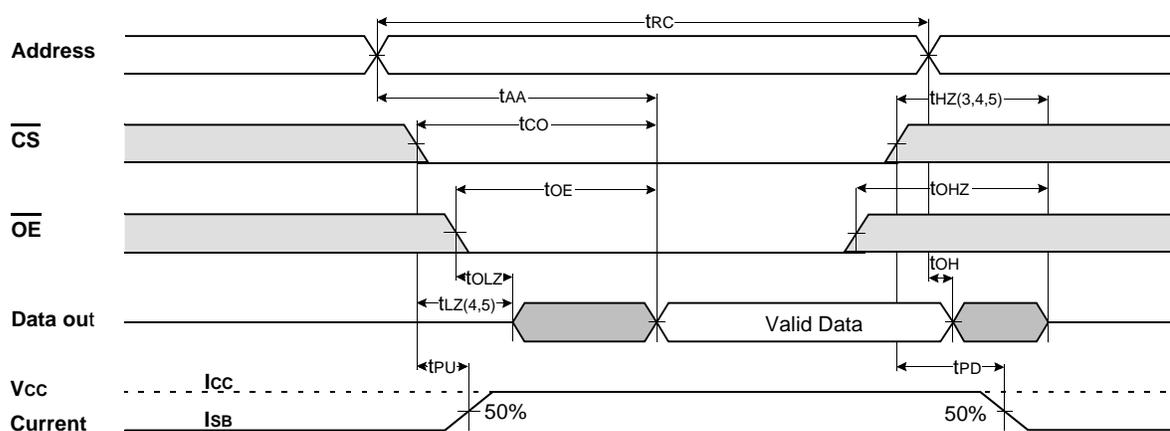
* The above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



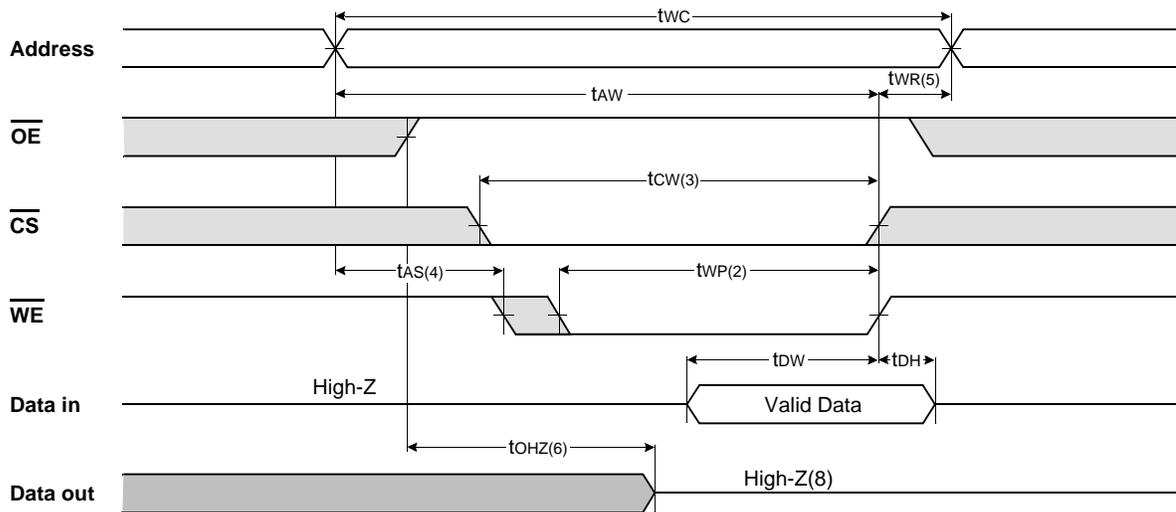
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



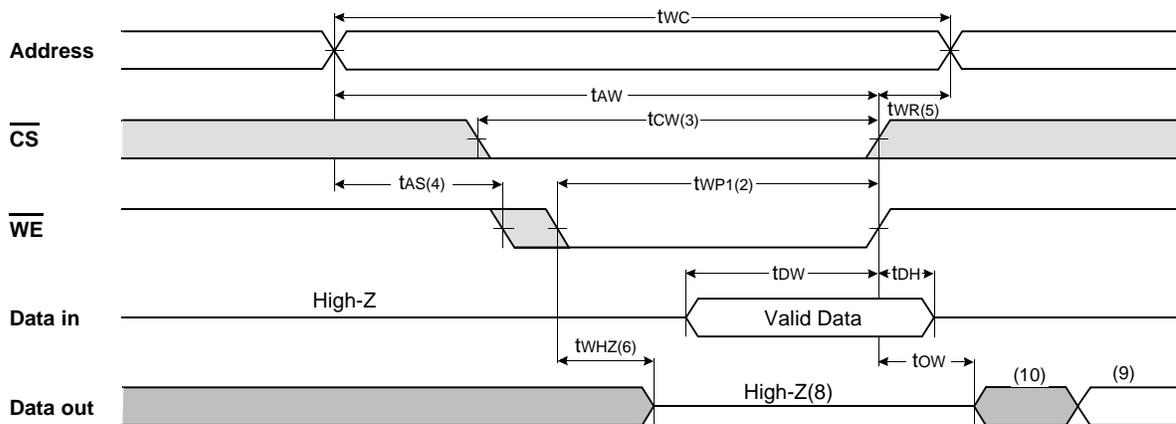
NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OH} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

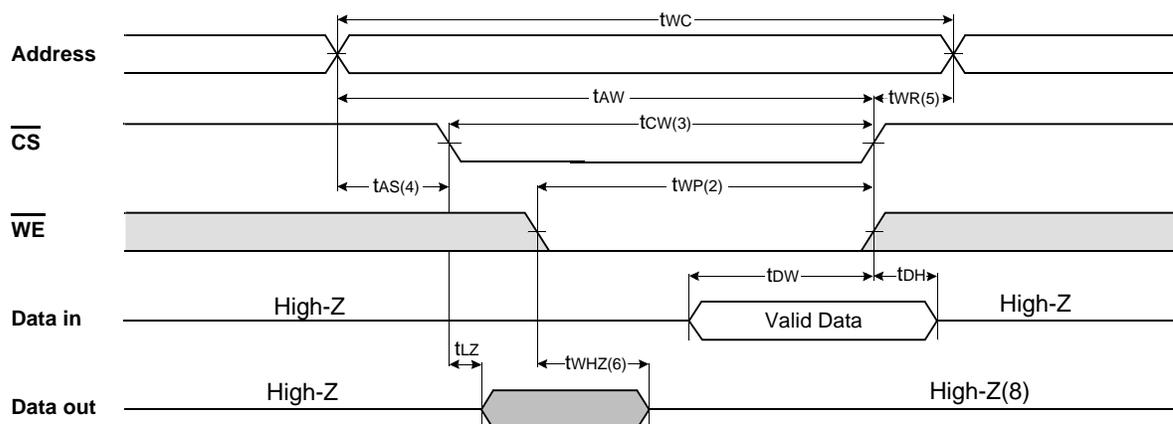
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}=\text{Clock}$)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}=\text{Low Fixed}$)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS} =Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. DOUT is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	DOUT	Icc
L	L	X	Write	DIN	Icc

* X means Don't Care.

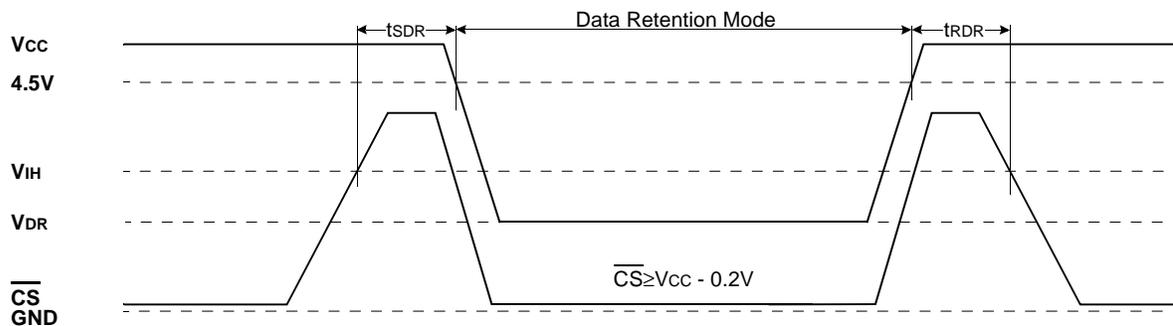
DATA RETENTION CHARACTERISTICS*($T_A=0$ to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	V _{DR}	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	2.0	-	3.6	V
Data Retention Current	I _{DR}	$V_{\text{CC}} = 3.0\text{V}, \overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	0.4	mA
		$V_{\text{CC}} = 2.0\text{V}, \overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	0.3	
Data Retention Set-Up Time	t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t _{RDR}	Wave form(below)	5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM

$\overline{\text{CS}}$ controlled



PACKAGE DIMENSIONS

Units: millimeters/Inches

32-SOJ-400

