Unbuffered SDRAM DIMM(168pin) PC133 4Layer SPD Specification

REV. 0.2

Nov. 1999

KMM366S823DTS-GA

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8030DT-GA
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 row of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	8Ch	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	6	36h	
79	..... Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	Blank	20h	
82	..... Manufacturer part # (Module density)	8	38h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	D	44h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM374S823DTS-GA

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : KM48S8030DT-GA
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	1 row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 row of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Eh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	7	37h	
79	..... Manufacturer part # (Data bits)	4	34h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	Blank	20h	
82	..... Manufacturer part # (Module density)	8	38h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	D	44h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM366S924BTS-GA

- Organization : 8Mx64
- Composition : 8Mx16 *4
- Used component part # : KM416S8030BT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	94h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	6	36h	
79	..... Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	Blank	20h	
82	..... Manufacturer part # (Module density)	9	39h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	4	34h	
85	Manufacturer part # (Component revision)	B	42h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM366S1723ATS-GA

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : KM48S16030AT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Dh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	6	36h	
79	..... Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	1	31h	
82	..... Manufacturer part # (Module density)	7	37h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	A	41h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM366S1723BTS-GA

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : KM48S16030BT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Dh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	6	36h	
79	..... Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	1	31h	
82	..... Manufacturer part # (Module density)	7	37h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	B	42h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM374S1723ATS-GA

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : KM48S16030AT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	AFh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	7	37h	
79	..... Manufacturer part # (Data bits)	4	34h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	1	31h	
82	..... Manufacturer part # (Module density)	7	37h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	A	41h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM374S1723BTS-GA

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : KM48S16030BT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	AFh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	7	37h	
79	..... Manufacturer part # (Data bits)	4	34h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	1	31h	
82	..... Manufacturer part # (Module density)	7	37h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	B	42h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM366S3253ATS-GA

- Organization : 32Mx64
- Composition : 32Mx8 *8
- Used component part # : KM48S32230AT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 256MB	40h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	C0h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	6	36h	
79	..... Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	3	33h	
82	..... Manufacturer part # (Module density)	2	32h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	5	35h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	A	41h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

KMM374S3253ATS-GA

- Organization : 32Mx72
- Composition : 32Mx8 *9
- Used component part # : KM48S32230AT-GA
- # of rows in module : 2 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 256MB	40h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	D2h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	7	37h	
79	..... Manufacturer part # (Data bits)	4	34h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	3	33h	
82	..... Manufacturer part # (Module density)	2	32h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	5	35h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	A	41h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	S	53h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	S	53h	
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Reserved	-	64h	5
127	Reserved	Detailed PC100 Information	ADh	5
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 application only,per Intel PC66/100 SPD standards.