Registered SDRAM PC133 DIMM(168pin)
SPD Specification

REV. 1

July. 1999

KMM390S823DT1-GA

•Organization : 8MX72
•Composition : 8MX8 *9
•Used component part # : KM48S8030DT-GA
•# of banks in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,500 mil height & double sided component
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and on-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	BDh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	9	39h	
79	..... Manufacturer part # (Data bits)	0	30h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	Blank	20h	
82	..... Manufacturer part # (Module density)	8	38h	
83	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2	32h	
84	Manufacturer part # (Compositon component)	3	33h	
85	Manufacturer part # (Component revision)	D	44h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	1	31h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	1	31h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Module Supports this CLK Frequency	100MHz	64h	
127	Attributes for CLK frequency defined	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	-	FFh	

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM390S1620DT1-GA

- Organization : 16Mx72
- Composition : 16MX4 *18
- Used component part # : KM44S16030DT-GA
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-Card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 Row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-A	-A	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	C6h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	3	33h	
77	Manufacturer part # (Data bits)	Blank	20h	
78	..... Manufacturer part # (Data bits)	9	39h	
79	..... Manufacturer part # (Data bits)	0	30h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	1	31h	
82	..... Manufacturer part # (Module density)	6	36h	
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2	32h	
84	Manufacturer part # (Compositon component)	0	30h	
85	Manufacturer part # (Component revision)	D	44h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	1	31h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	G	47h	
90	Manufacturer part # (Minimum cycle time)	A	41h	
91	Manufacturer revision code (For PCB)	1	31h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	Module Supports this CLK Frequency	100MHz	64h	
127	Attributes for CLK frequency defined	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	-	FFh	

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