PC100 Unbuffered SDRAM DIMM(168pin) 6 Layer SPD Specification

Rev. 0.0

November 1999

• Revision History

[Revision 0.0] November 18, 1999
Merged PC100 SDRAM 6 Layer Unbuffered DIMMs based 64SD D-die, 128SD M/A/B-die, 256SD A-die.

• SPD Spec List

KMM366S824DT
KMM366S1623DT
KMM374S1623DT
KMM366S1724T
KMM366S1724BT
KMM366S3323T
KMM366S3323AT
KMM366S3323BT
KMM374S3323T
KMM374S3323AT
KMM374S3323BT
KMM366S6453AT
KMM374S6453AT

KMM366S824DT-G8/GH/GL

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4030DT-G8/GH/GL
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 32MB			08h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			DFh	05h	35h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	D			44h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S1623DT-G8/GH/GL

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : KM48S8030DT-G8/GH/GL
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			E0h	06h	36h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	D			44h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM374S1623DT-G8/GH/GL

- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : KM48S8030DT-G8/GH/GL
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module rows on this assembly	2 rows			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	10ns	10ns	12ns	A0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module row density	2 rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			F2h	18h	48h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	D			44h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)			44h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S1724T-G8/GH/GL

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : KM416S8030T-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			08h	0Eh	3Eh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	7			37h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	Blank			20h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	Blank (1st Gen.)			20h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S1724BT-G8/GH/GL

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : KM416S8030BT-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			08h	0Eh	3Eh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	7			37h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S3323T-G8/GH/GL

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : KM48S16030T-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			11h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	3			33h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	Blank			20h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	Blank (1st Gen.)			20h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S3323AT-G8/GH/GL

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : KM48S16030AT-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			11h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	3			33h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S3323BT-G8/GH/GL

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : KM48S16030BT-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			11h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	3			33h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM374S3323T-G8/GH/GL

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : KM48S16030T-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			23h	29h	59h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	3			33h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	Blank			20h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	Blank (1st Gen.)			20h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM374S3323AT-G8/GH/GL

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : KM48S16030AT-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			23h	29h	59h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	3			33h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM374S3323BT-G8/GH/GL

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : KM48S16030BT-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			23h	29h	59h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	3			33h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM366S6453AT-G8/GH/GL

- Organization : 64Mx64
- Composition : 32Mx8 *16
- Used component part # : KM48S32230AT-G8/GH/GL
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 8K / 64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	7.8us, support self refresh			82h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 256MB			40h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			34h	3Ah	6Ah	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	6			36h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	5			35h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.

KMM374S3253AT-G8/GH/GL

- Organization : 32Mx72
- Composition : 32Mx8 *9
- Used component part # : KM48S32230AT-G8/GH/GL
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K / 64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	7.8 us, support self refresh			82h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 256MB			40h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-H	-L	-8	-H	-L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			45h	4Bh	7Bh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	3			33h			
82	..... Manufacturer part # (Module density)	2			32h			
83	Manufacturer part # (Refresh, # of rows in Comp. & interface)	5			35h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	H	L	38h	48h	4Ch	
91	Manufacturer revision code (For PCB)	Blank(Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	-			FFh			

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.