

DRAM MODULE

KMM466F404CS2-L

KMM466F404CS2-L EDO Mode

4M x 64 DRAM SODIMM Using 4Mx16, 4K Refresh 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F404CS2-L is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F404CS2-L consists of four CMOS 4Mx16bits DRAMs in TSOP 400mil packages and a 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F404CS2-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
 - KMM466F404CS2-L(4096 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- CAS-before-RAS Refresh capability
- Self -refresh capability
- RAS-only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

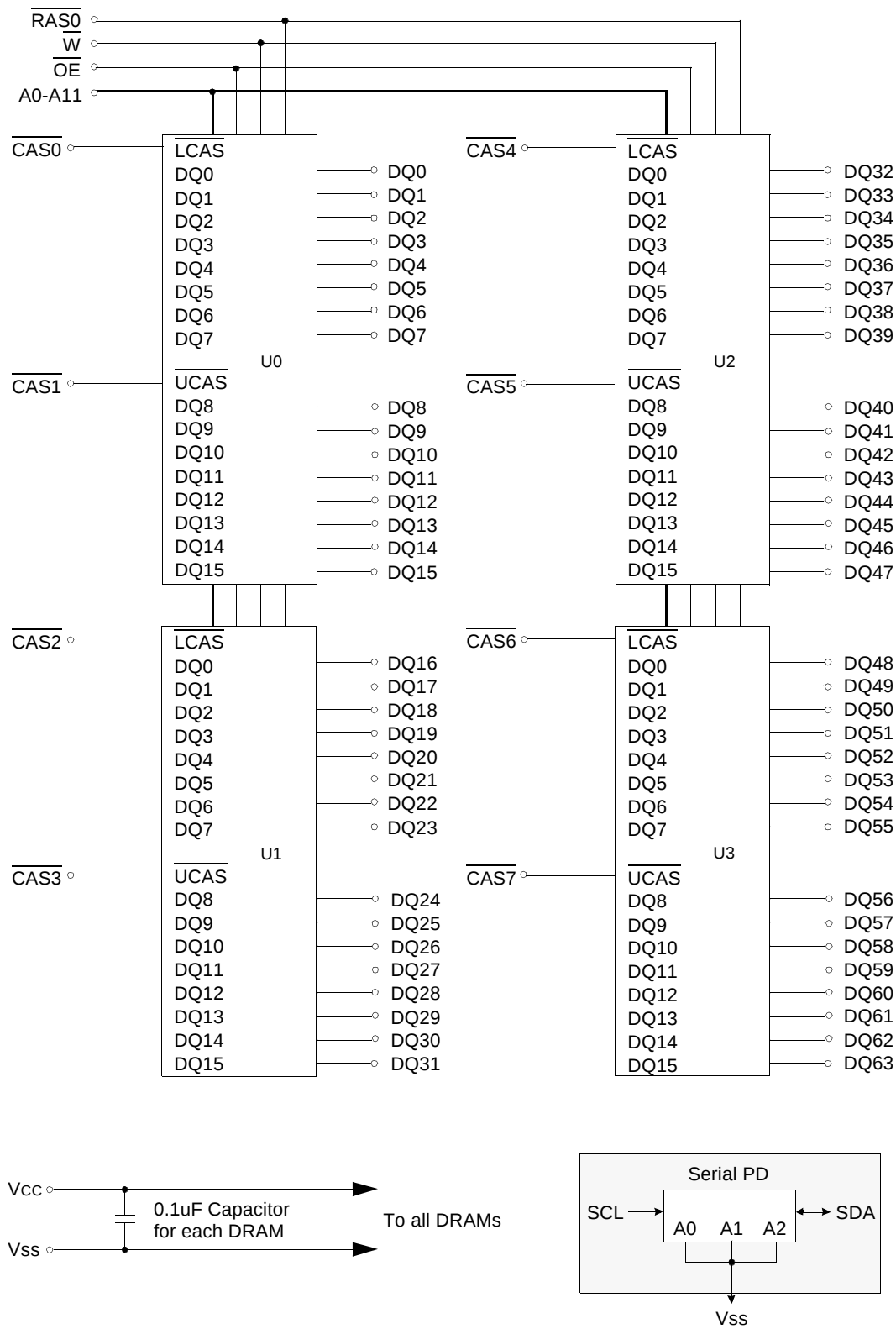
PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	W	68	RFU	115	CAS2	116	CAS6
21	Vss	22	Vss	69	RAS0	70	RFU	117	CAS3	118	CAS7
23	CAS0	24	CAS4	71	NC	72	RFU	119	Vss	120	Vss
25	CAS1	26	CAS5	73	OE	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

PIN NAMES

Pin Name	Function
A0 to A11	Address Inputs
DQ0 - DQ63	Data In/Out
W	Read/Write Enable
OE	Output Enable
RAS0	Row Address Strobe
CAS0 - CAS7	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
SDA	Serial Address / Data I/O
SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

FUNCTIONAL BLOCK DIAGRAM



DRAM MODULE

KMM466F404CS2-L

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _D	4	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F404CS2-L		Unit
		Min	Max	
I _{CC1}	-5	-	480	mA
	-6	-	440	mA
I _{CC2}	Don't care	-	4	mA
I _{CC3}	-5	-	480	mA
	-6	-	440	mA
I _{CC4}	-5	-	360	mA
	-6	-	320	mA
I _{CC5}	Don't care	-	0.8	mA
I _{CC6}	-5	-	480	mA
	-6	-	440	mA
I _{CC7}	Don't care	-	1.4	mA
I _{CCS}	Don't care	-	1.4	mA
I _{I(L)}	Don't care	-10	10	uA
I _{O(L)}	Don't care	-5	5	uA
V _{OH}	Don't care	2.4	-	V
V _{OL}	Don't care	-	0.4	V

I_{CC1} : Operating Current * (RAS, CAS, Address cycling @trc=min)

I_{CC2} : Standby Current (RAS=CAS=W=V_{IH})

I_{CC3} : RAS Only Refresh Current * (CAS=V_{IH}, RAS cycling @trc=min)

I_{CC4} : Extended Data Out Mode Current * (RAS=V_{IL}, CAS cycling : t_{HPC}=min)

I_{CC5} : Standby Current (RAS=CAS=W=V_{CC}-0.2V)

I_{CC6} : CAS-Before-RAS Refresh Current * (RAS and CAS cycling @trc=min)

I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, UCAS,LCAS=0.2V,

Din=Don't care, trc=31.25us, tras=trasmin~300ns

I_{CCS} : Self Refresh Current, RAS=UCAS=LCAS=V_{IL}, W=OE=A0~A11=V_{CC}-0.2V or 0.2V, DQ~DQ63=V_{CC}-0.2V or Open

I_{I(L)} : Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.



ELECTRONICS

DRAM MODULE

KMM466F404CS2-L

CAPACITANCE (TA = 25°C, VCC=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	CIN1	-	30	pF
Input capacitance[W, OE]	CIN2	-	38	pF
Input capacitance[RAS0]	CIN3	-	38	pF
Input capacitance[CAS0 - CAS7]	CIN4	-	17	pF
Input/Output capacitance[DQ0 - 63]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Read-modify-write cycle time	tRWC	128		153		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,9
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,9
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		ns	3
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	ns	3,11
Transition time(rise and fall)	tT	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	8		10		ns	
$\overline{\text{CAS}}$ hold time	tCSH	38		40		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	17	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	12	25	15	30	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	7		10		ns	
Column address set-up time	tASC	0		0		ns	12
Column address hold time	tCAH	7		10		ns	12
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	7
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	7
Write command set-up time	twCS	0		0		ns	6
Write command hold time	twCH	7		10		ns	6
Write command pulse width	tWP	7		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	8		10		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	7		10		ns	15
Data set-up time	tDS	0		0		ns	8,18
Data hold time	tDH	7		10		ns	8,18
Refresh period	tREF		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	33		38		ns	6,14
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	70		84		ns	6

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AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t _{AWD}	45		53		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t _{CPWD}	47		58		ns	6
$\overline{CAS}$ setup time (CAS-before-RAS refresh)	t _{CSR}	5		5		ns	16
$\overline{CAS}$ hold time (CAS-before-RAS refresh)	t _{CHR}	10		10		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t _{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t _{CPA}		28		35	ns	3
Hyper page mode cycle time	t _{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t _{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t _{CP}	7		10		ns	13
$\overline{RAS}$ pulse width (Hyper page cycle)	t _{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t _{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t _{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t _{WRH}	10		10		ns	
$\overline{OE}$ access time	t _{OEa}		13		15	ns	3
$\overline{OE}$ to data delay	t _{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t _{OEZ}	3	13	3	13	ns	
$\overline{OE}$ command hold time	t _{OEh}	5		5		ns	
Output data hold time	t _{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t _{REZ}	3	13	3	15	ns	11
Output buffer turn off delay from $\overline{W}$	t _{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t _{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t _{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t _{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t _{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t _{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t _{RASS}	100		100		us	19,20,21
$\overline{RAS}$ precharge time (C-B-R self refresh)	t _{RPS}	90		110		ns	19,20,21
$\overline{CAS}$ hold time (C-B-R self refresh)	t _{CHS}	-50		-50		ns	19,20,21

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPWD} \geq t_{CPWD}(\text{min})$. The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
9. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit access time is controlled by t_{AA} .
10. $t_{ASC} \geq 6\text{ns}$, Assume $t_T = 2.0\text{ns}$
11. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
12. t_{ASC} is referenced to the earlier $\overline{\text{CAS}}$ falling edge and t_{CAH} is referenced to the later $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling edge to the $\overline{\text{RAS}}$ falling edge.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising from $\overline{\text{RAS}}$ falling edge.
18. t_{DS} , t_{DH} is specified by the earlier $\overline{\text{CAS}}$ falling edge.
19. If $t_{RASS} \geq 100\mu\text{s}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
20. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
21. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6 μs interval $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ should be executed with in 15.6 μs immediately before and after self refresh in order to meet refresh specification.

The diagram illustrates the timing relationships for a memory device. The signals shown are:

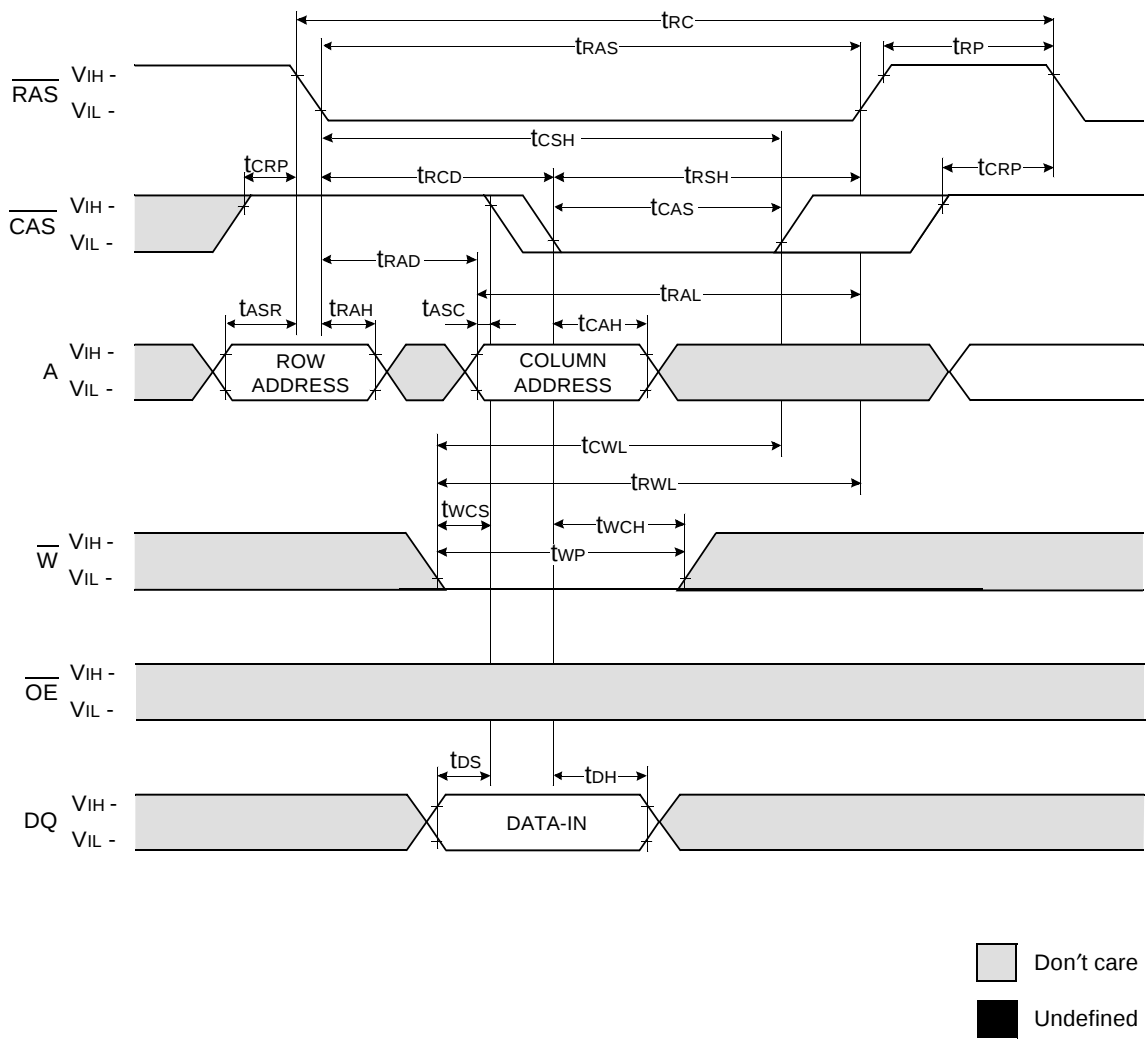
- RAS**: Row Address Strobe. Timing parameters include t_{RAS} (pulse width), t_{RC} (period), t_{RP} (pulse width), t_{CRP} (setup/hold), t_{CSH} (setup/hold), t_{RSH} (setup/hold), t_{RAD} (setup/hold), t_{RAH} (setup/hold), t_{ASC} (setup/hold), t_{CAH} (setup/hold), t_{RAL} (setup/hold).
- CAS**: Column Address Strobe. Timing parameters include t_{CRP} (setup/hold), t_{RCD} (setup/hold), t_{RSH} (setup/hold), t_{CAS} (setup/hold), t_{RAD} (setup/hold), t_{RAH} (setup/hold), t_{ASC} (setup/hold), t_{CAH} (setup/hold), t_{RAL} (setup/hold).
- A**: Address. Timing parameters include t_{ASR} (setup/hold), t_{AH} (setup/hold), t_{ASC} (setup/hold), t_{CAH} (setup/hold), t_{RAL} (setup/hold).
- W**: Write Enable. Timing parameters include t_{RCAS} (setup/hold), t_{RRH} (setup/hold), t_{RCH} (setup/hold), t_{AA} (setup/hold), t_{OEA} (setup/hold), t_{OLZ} (setup/hold), t_{CAC} (setup/hold), t_{CLZ} (setup/hold), t_{TRAC} (setup/hold), t_{WEZ} (setup/hold), t_{CEZ} (setup/hold), t_{OEZ} (setup/hold), t_{REZ} (setup/hold).
- OE**: Output Enable. Timing parameters include t_{AA} (setup/hold), t_{OEA} (setup/hold), t_{OLZ} (setup/hold), t_{CAC} (setup/hold), t_{CLZ} (setup/hold), t_{TRAC} (setup/hold), t_{WEZ} (setup/hold), t_{CEZ} (setup/hold), t_{OEZ} (setup/hold), t_{REZ} (setup/hold).
- DQ**: Data Bus. Timing parameters include t_{TRAC} (setup/hold), t_{WEZ} (setup/hold), t_{CEZ} (setup/hold), t_{OEZ} (setup/hold), t_{REZ} (setup/hold).

The diagram also shows the data bus state: **OPEN** (high impedance) and **DATA-OUT** (data output).

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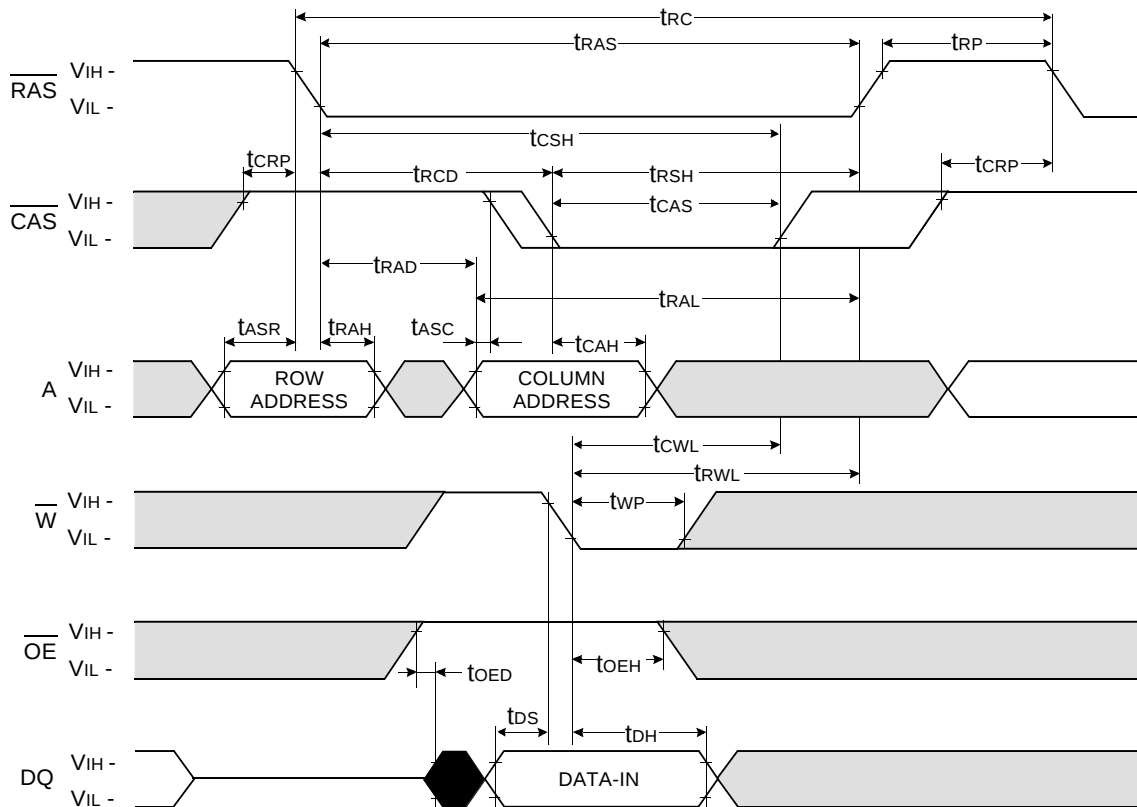
WRITE CYCLE (EARLY WRITE)

NOTE : Dout = OPEN



WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

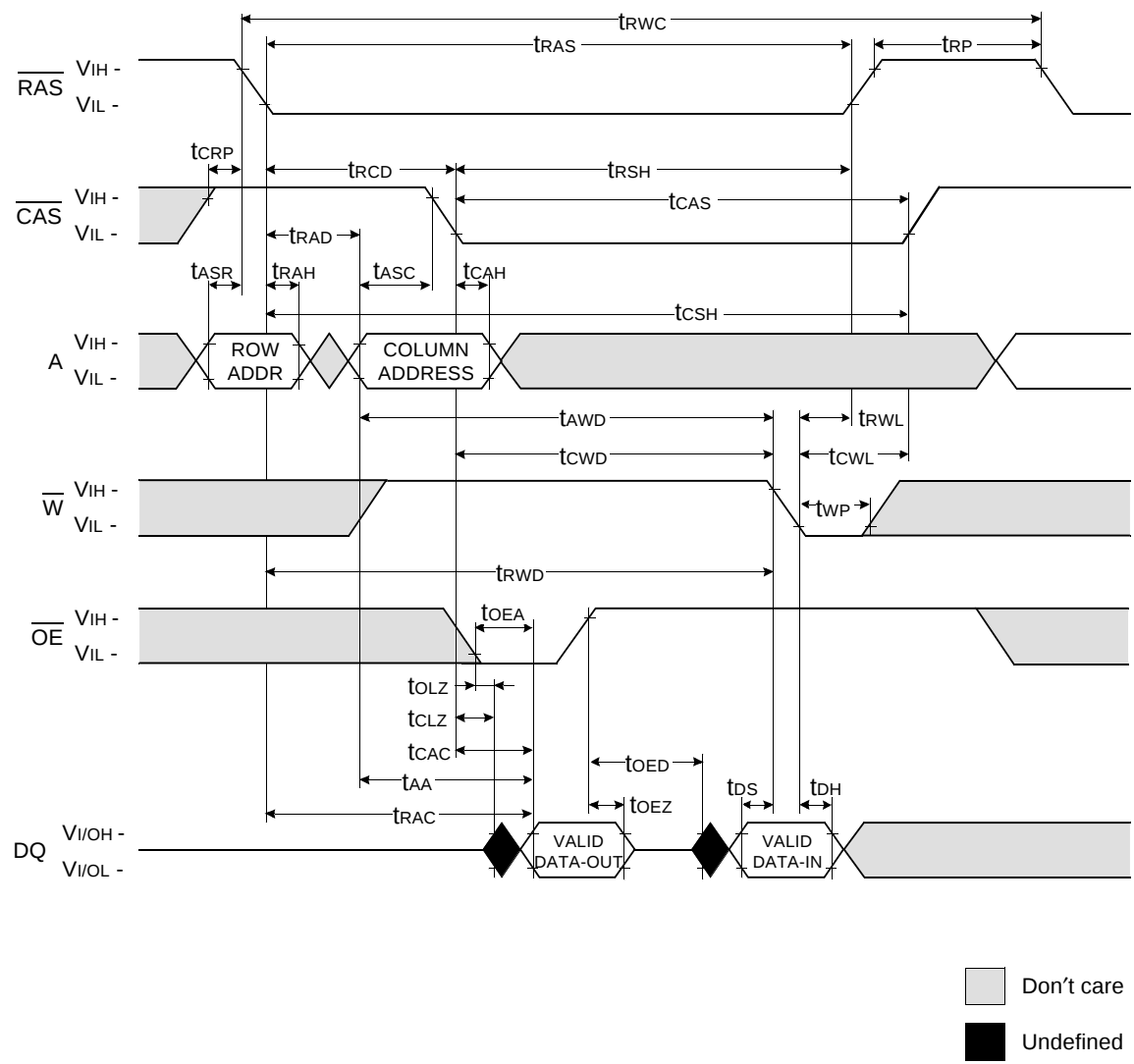
NOTE : DOUT = OPEN



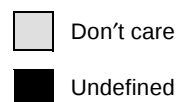
Don't care

Undefined

READ - MODIFY - WRITE CYCLE

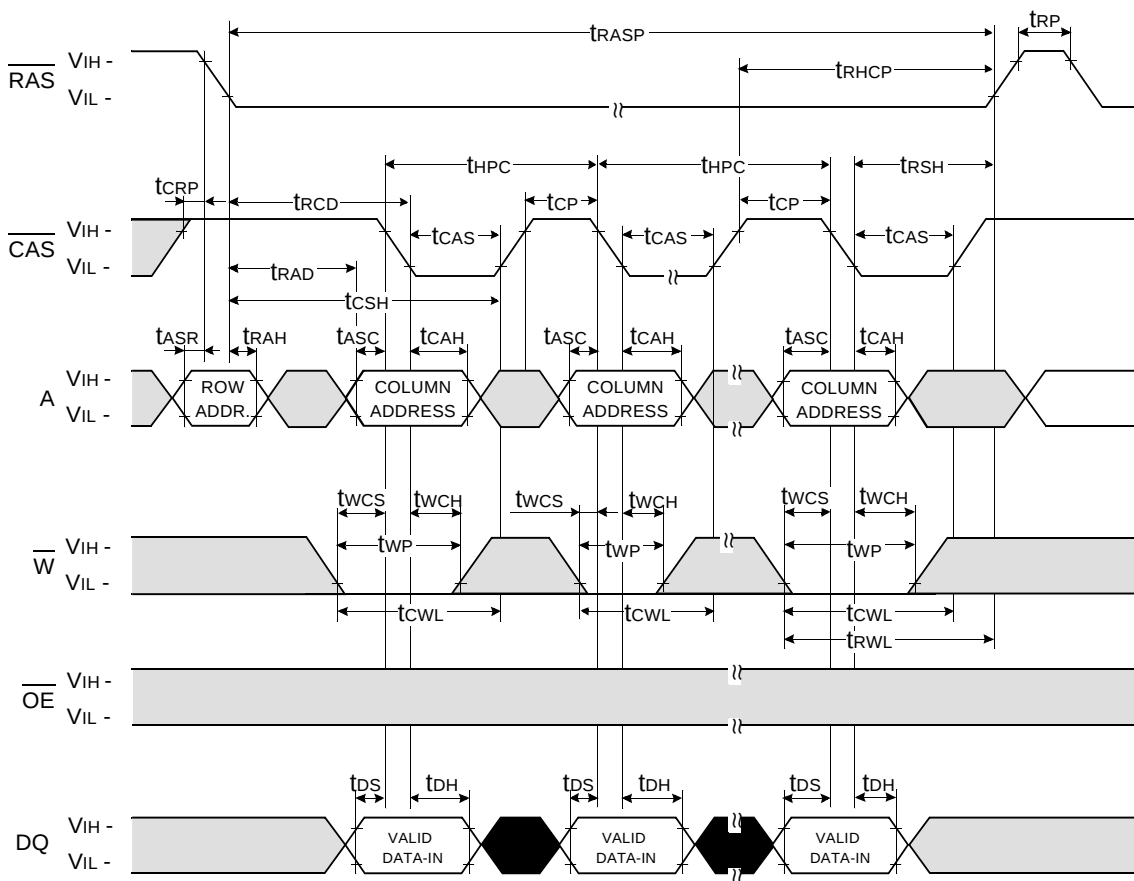


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

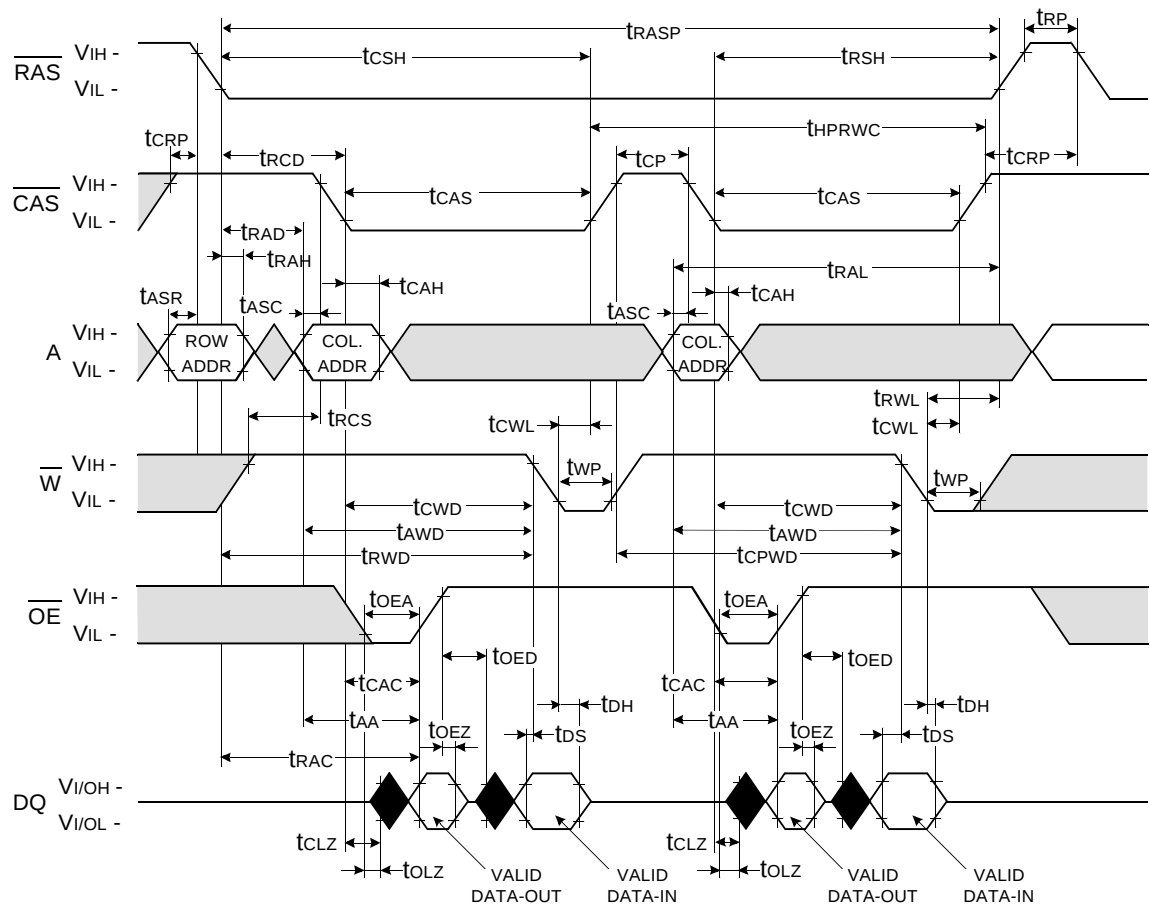
NOTE : DOUT = OPEN



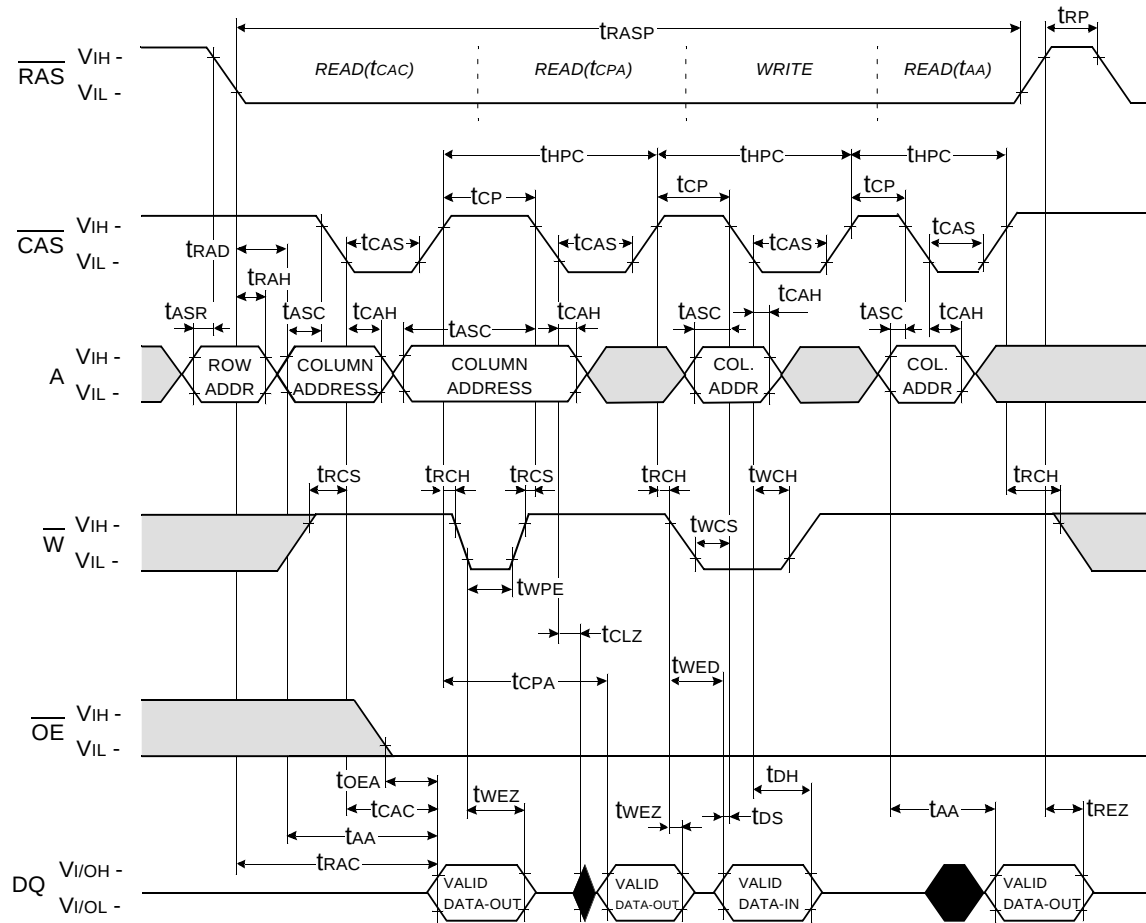
Don't care

Undefined

HYPER PAGE READ-MODIFY-WRITE CYCLE



HYPER PAGE READ AND WRITE MIXED CYCLE

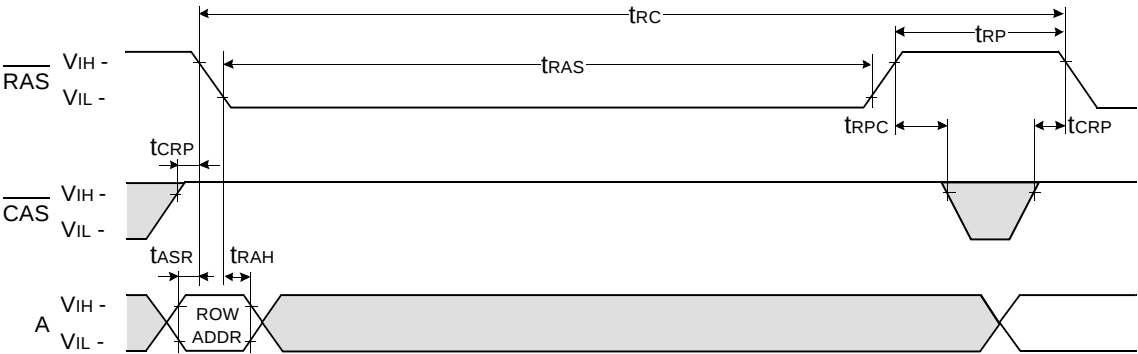


Don't care
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RAS - ONLY REFRESH CYCLE*

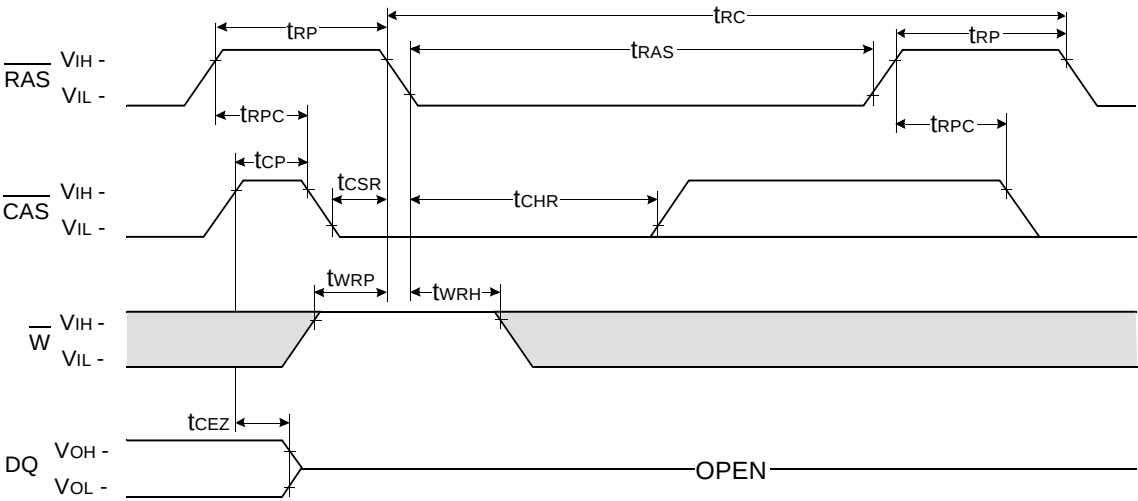
NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

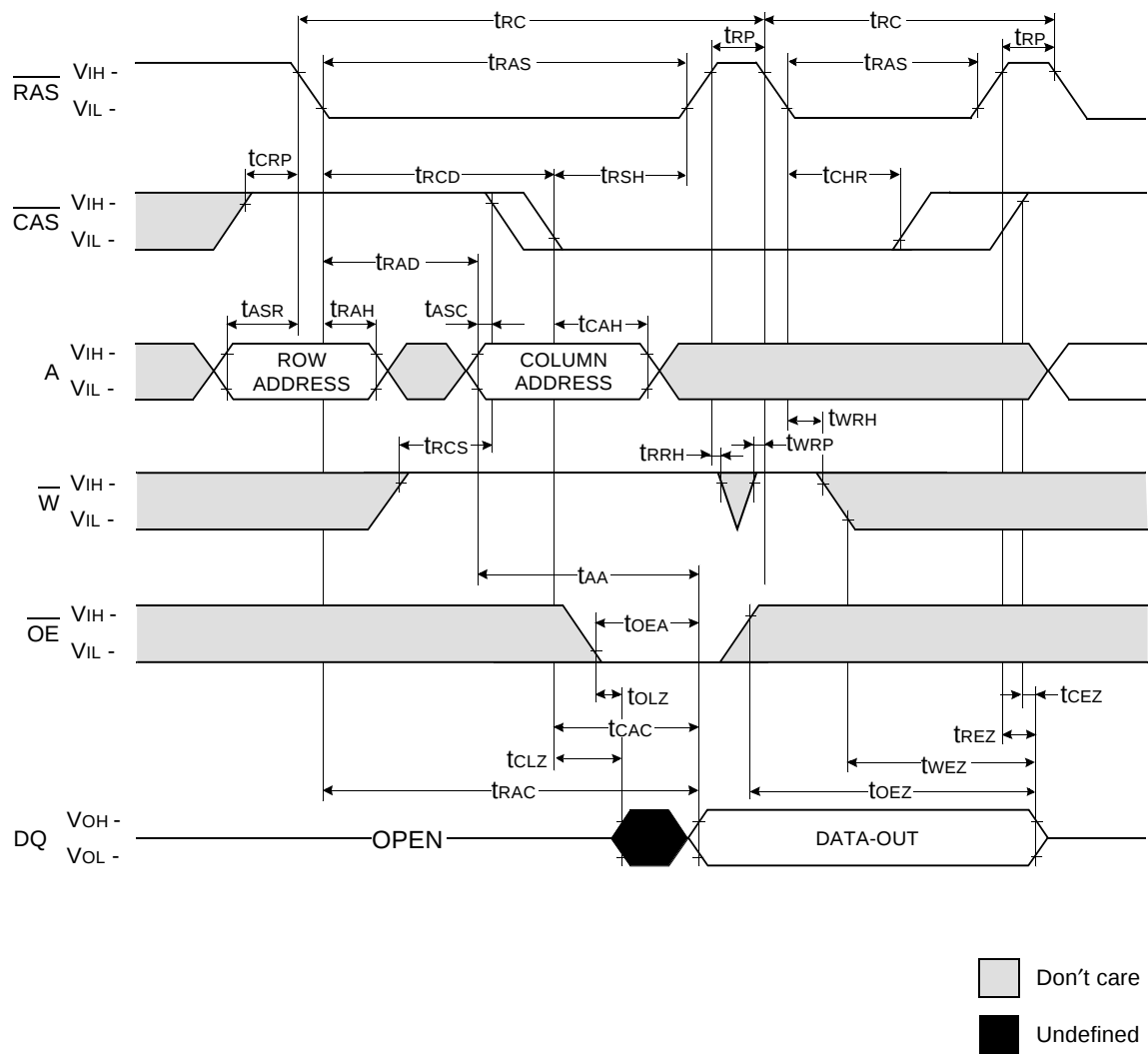


Don't care

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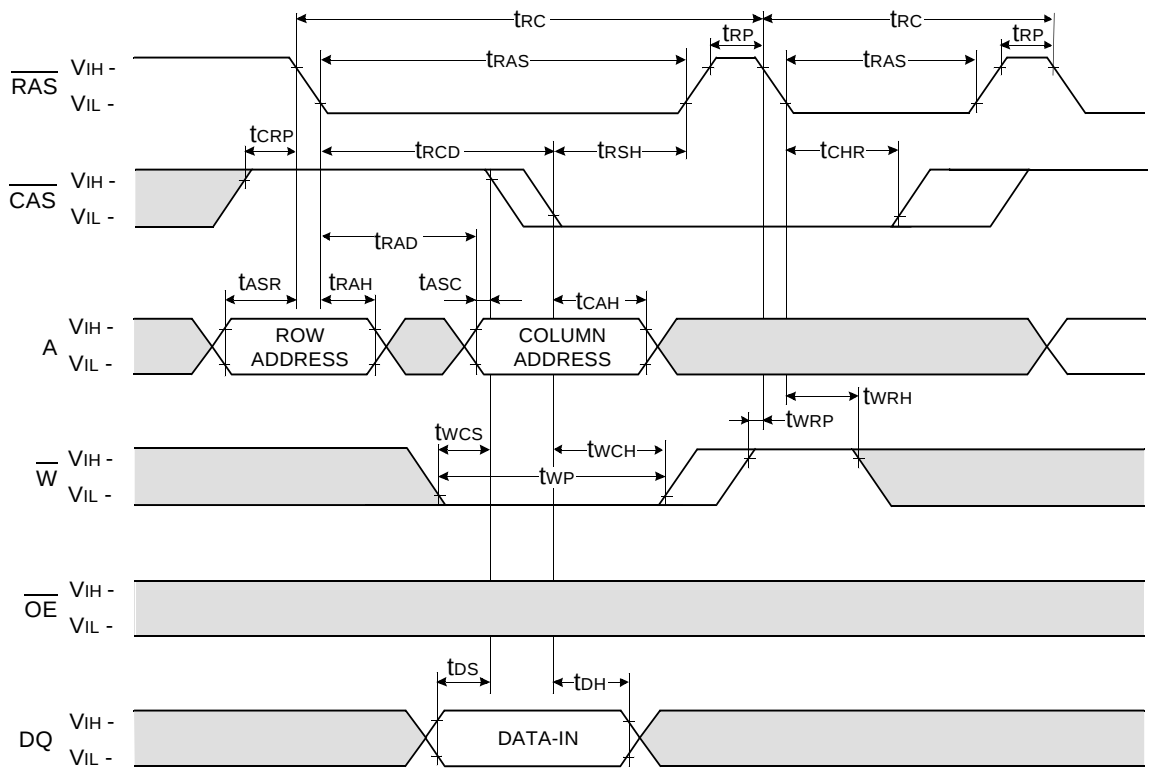
* In RAS-only refresh cycle of 64Mb A-die & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)



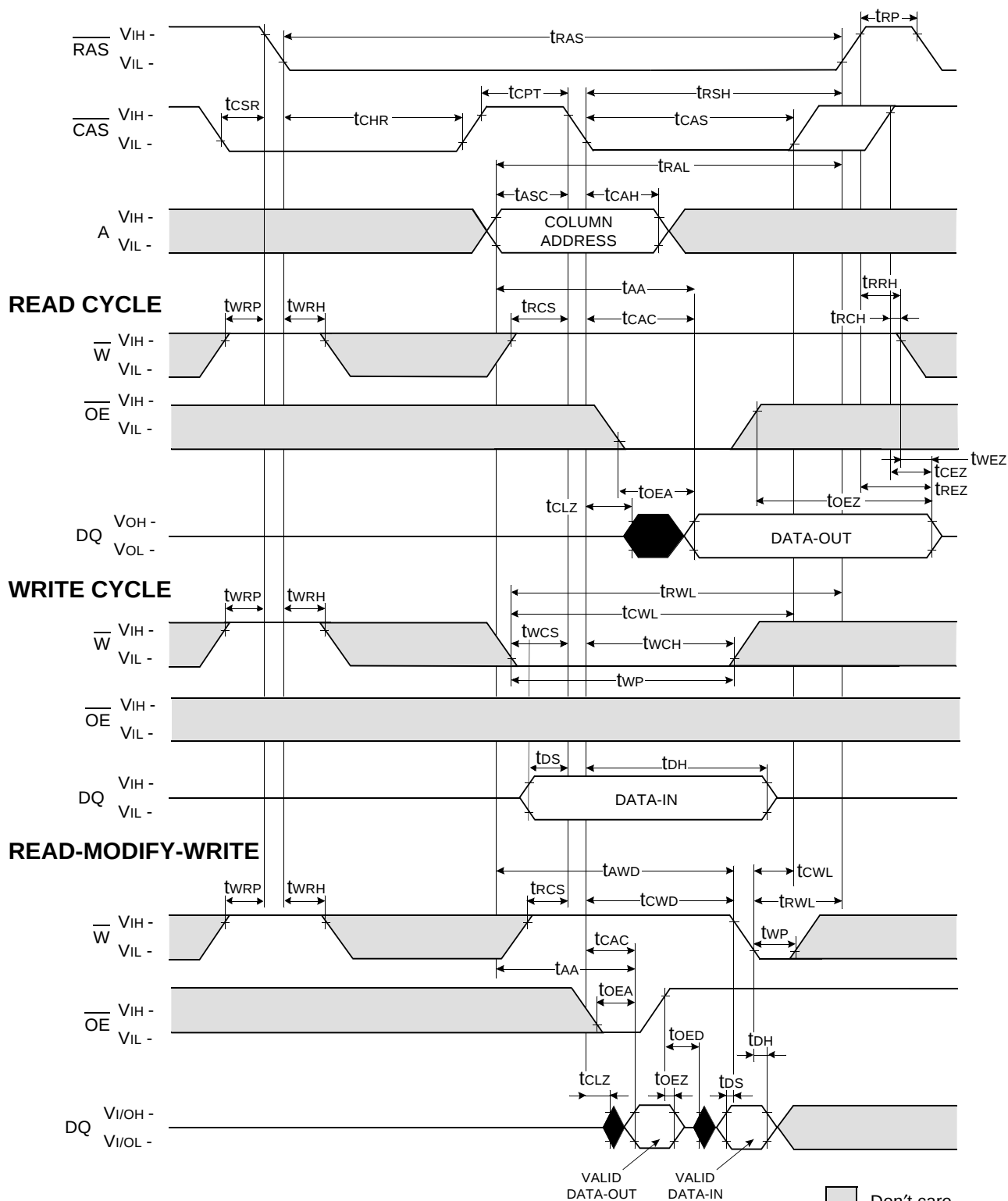
HIDDEN REFRESH CYCLE (WRITE)

NOTE : Dout = OPEN



Don't care
Undefined

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

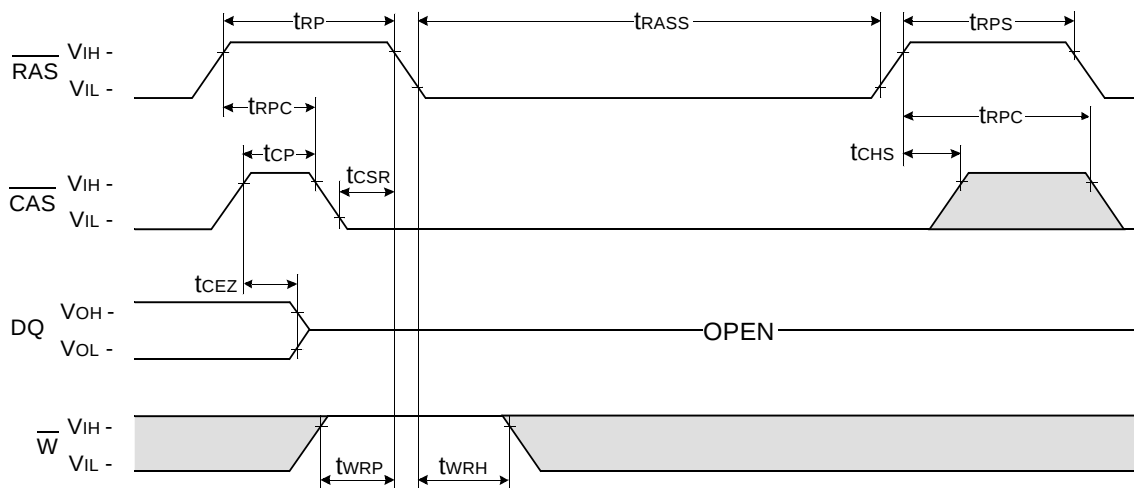


NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

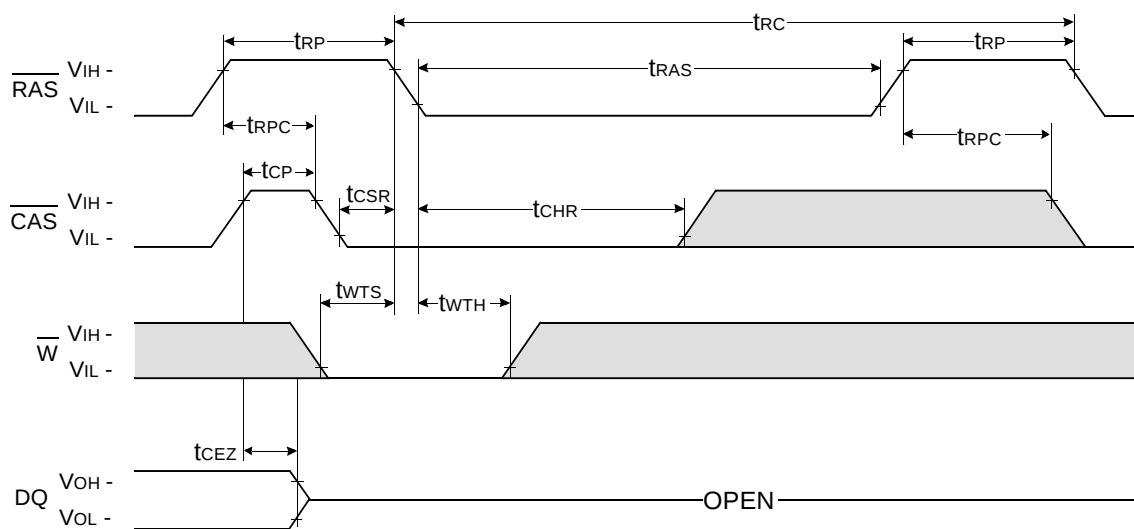
 Don't care

 Undefined

NOTE : $\overline{OE}, A$ = Don't care



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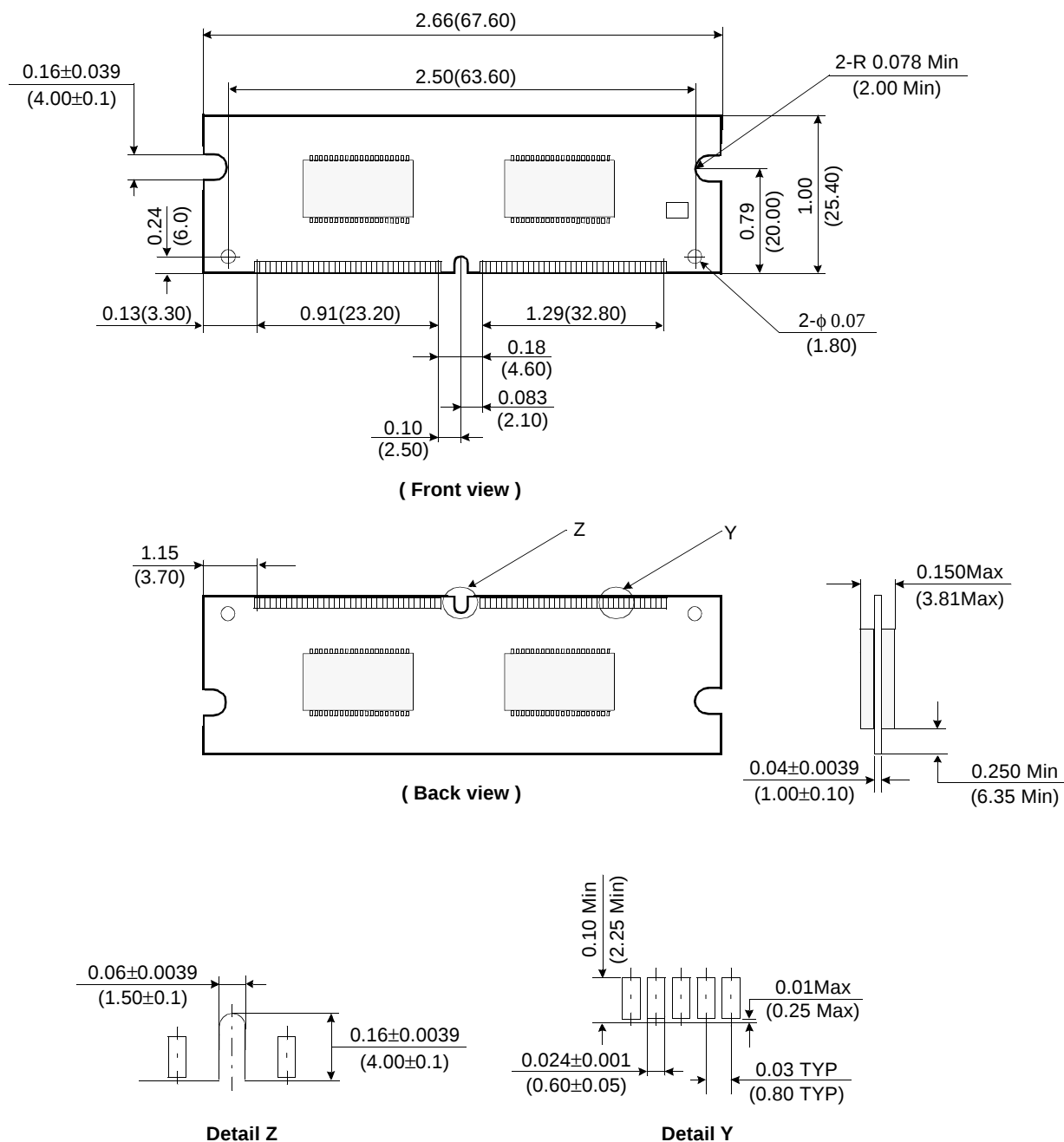
■ Undefined

DRAM MODULE

KMM466F404CS2-L

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOPII
 DRAM Part No. : KM416V4104CS-L