

4Byte 4Mx36 SIMM

(4Mx16 & Quad CAS 4Mx4 base)

Revision 0.0

June 1999



ELECTRONICS

Revision History

Version 0.0 (June 1999)

- The 4th. generation of 64Mb DRAM components are applied for this module.

DRAM MODULE

KMM5364005CSW/CSWG

KMM5364005CSW/CSWG EDO Mode

4M x 36 DRAM SIMM Using 4Mx16 & Quad CAS 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5364005C is a 4Mx36bits Dynamic RAM high density memory module. The Samsung KMM5364005C consists of two CMOS 4Mx16bits and one CMOS Quad CAS 4Mx4bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5364005C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
 - KMM5364005CSW(4K cycles/64ms Ref, TSOP, Solder)
 - KMM5364005CSWG(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- CAS-before-RAS & Hidden Refresh capability
- RAS-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	V _{SS}	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	V _{SS}
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	NC
10	V _{CC}	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	V _{CC}
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	V _{CC}	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	V _{SS}

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
W	Read/Write Enable
RAS0, RAS2	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
PD1 -PD4	Presence Detect
V _{CC}	Power(+5V)
V _{SS}	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

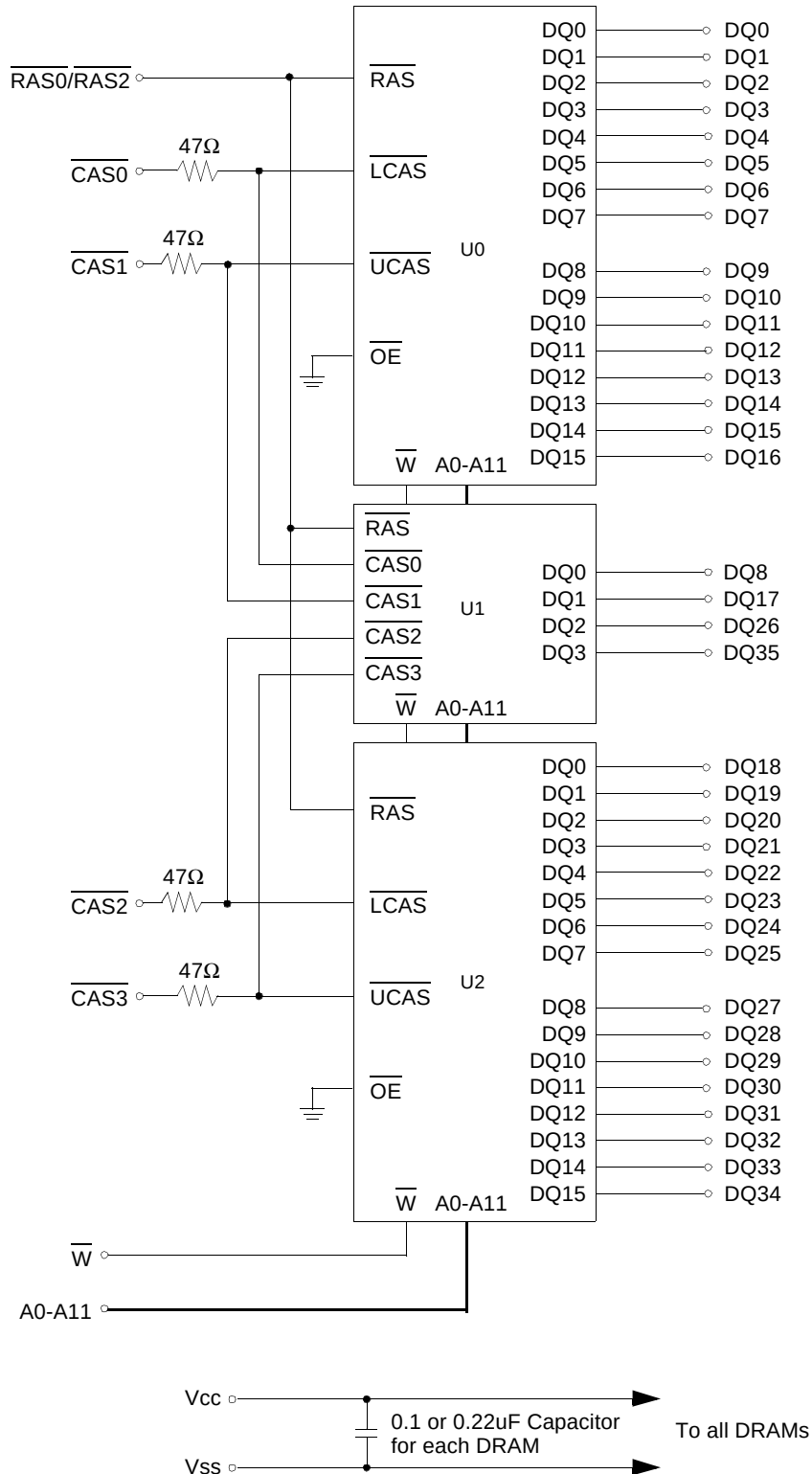
Pin	50NS	60NS
PD1	V _{SS}	V _{SS}
PD2	NC	NC
PD3	V _{SS}	NC
PD4	V _{SS}	NC

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DRAM MODULE

KMM5364005CSW/CSWG

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _d	3	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} ^{*1}	V
Input Low Voltage	V _{IL}	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤ 20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5364005CSW/CSWG		Unit
		Min	Max	
I _{CC1}	-5	-	330	mA
	-6	-	300	mA
I _{CC2}	Don't care	-	6	mA
I _{CC3}	-5	-	330	mA
	-6	-	300	mA
I _{CC4}	-5	-	260	mA
	-6	-	230	mA
I _{CC5}	Don't care	-	3	mA
I _{CC6}	-5	-	330	mA
	-6	-	300	mA
I _{I(L)}	Don't care	-10	10	uA
I _{O(L)}	Don't care	-5	5	uA
V _{OH}	Don't care	2.4	-	V
V _{OL}	Don't care	-	0.4	V

I_{CC1} : Operating Current * (RAS, CAS, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current (RAS=CAS=W=V_{IH})

I_{CC3} : RAS Only Refresh Current * (CAS=V_{IH}, RAS cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * (RAS=V_{IL}, CAS cycling : t_{HPC}=min)

I_{CC5} : Standby Current (RAS=CAS=W=V_{CC}-0.2V)

I_{CC6} : CAS-Before-RAS Refresh Current * (RAS and CAS cycling @t_{RC}=min)

I_{I(L)} : Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.



DRAM MODULE

KMM5364005CSW/CSWG

CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	CIN1	-	25	pF
Input capacitance[W]	CIN2	-	31	pF
Input capacitance[RAS0/RAS2]	CIN3	-	31	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	24	pF
Input/Output capacitance[DQ0 - 35]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : VIH/VIIL=2.6/0.8V, VOH/VOL=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Access time from RAS	tRAC		50		60	ns	3,4,10
Access time from CAS	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
CAS to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	13	3	13	ns	6,12
Transition time(rise and fall)	tT	1	50	1	50	ns	2
RAS precharge time	tRP	30		40		ns	
RAS pulse width	tRAS	50	10K	60	10K	ns	
RAS hold time	tRSH	13		15		ns	
CAS hold time	tCSH	38		45		ns	
CAS pulse width	tCAS	8	10K	10	10K	ns	4
RAS to CAS delay time	tRCD	20	37	20	45	ns	9
RAS to column address delay time	tRAD	15	25	15	30	ns	
CAS to RAS precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to RAS lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to CAS	tRCH	0		0		ns	8
Read command hold referenced to RAS	tRRH	0		0		ns	8
Write command set-up time	tWCS	0		0		ns	7
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to RAS lead time	tRWL	13		15		ns	
Write command to CAS lead time	tCWL	8		10		ns	
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	8		10		ns	9
Refresh period	tREF		64		64	ms	
CAS setup time (CAS-before-RAS refresh)	tCSR	5		5		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		ns	
RAS to CAS precharge time	tRPC	5		5		ns	
Access time from CAS precharge	tCPA		28		35	ns	3

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC} = 5.0V±10%. See notes 1,2.)

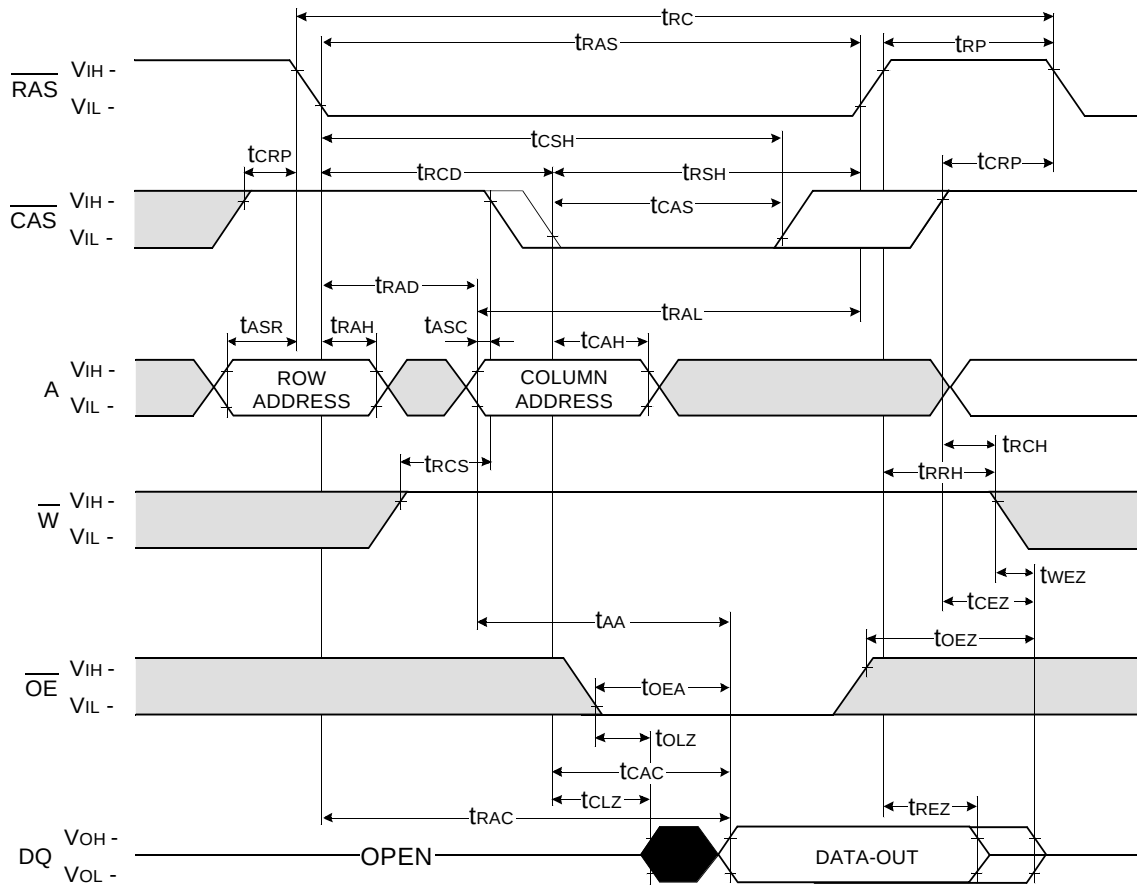
Test condition : V_{IH}/V_{IL}=2.6/0.8V, V_{OH}/V_{OL}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t _{HPC}	20		25		ns	11
CAS precharge time (Hyper page cycle)	t _{CP}	8		10		ns	
RAS pulse width (Hyper page cycle)	t _{RASP}	50	200K	60	200K	ns	
RAS hold time from CAS precharge	t _{RHCP}	30		35		ns	
W to RAS precharge time(C-B-R refresh)	t _{WRP}	10		10		ns	
W to RAS hold time(C-B-R refresh)	t _{WRH}	10		10		ns	
Output data hold time	t _{DOH}	5		5		ns	
Output buffer turn off delay from RAS	t _{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from W	t _{WEZ}	3	13	3	15	ns	6
W to data delay	t _{WED}	15		15		ns	
W pulse width	t _{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCD}≥t_{RCD}(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.
7. twcs is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.
11. t_{ASC}≥6ns, Assume t_T=2.0ns.
12. If RAS goes high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes high before RAS high going, the open circuit condition of the output is achieved by RAS going.

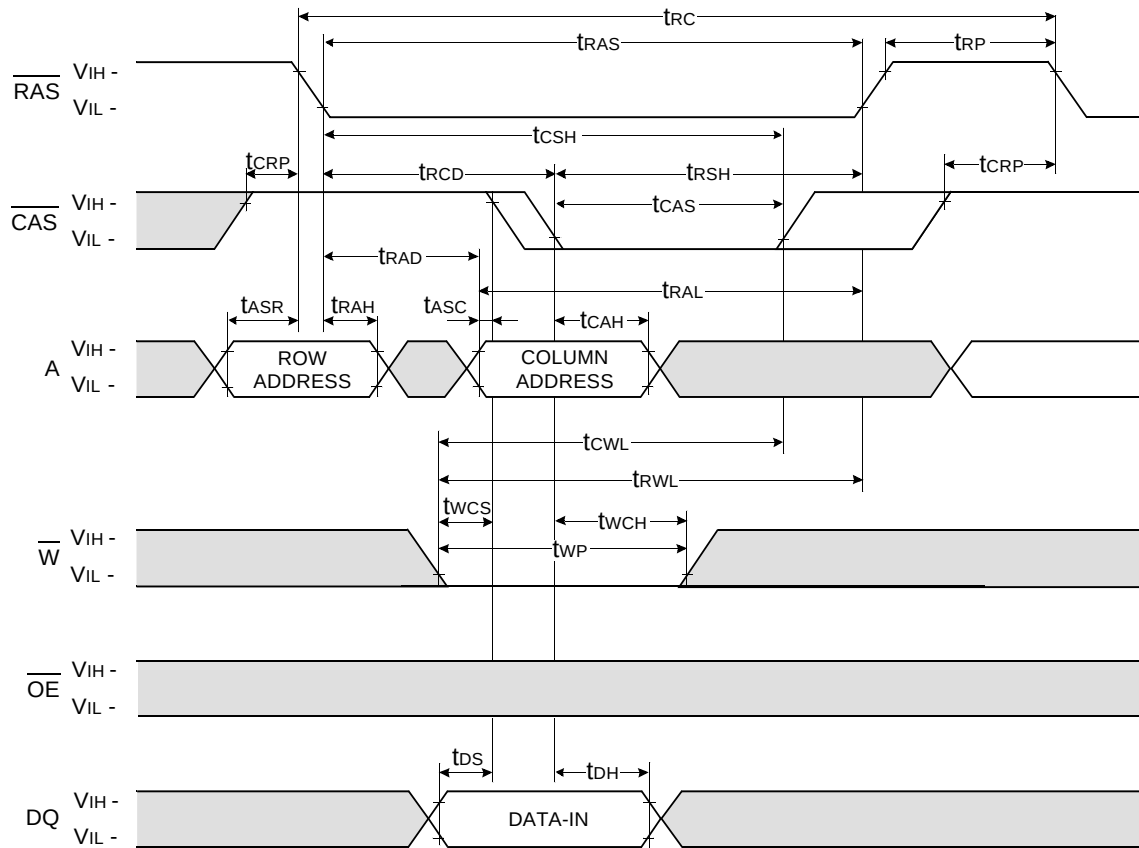
READ CYCLE



Don't care
Undefined

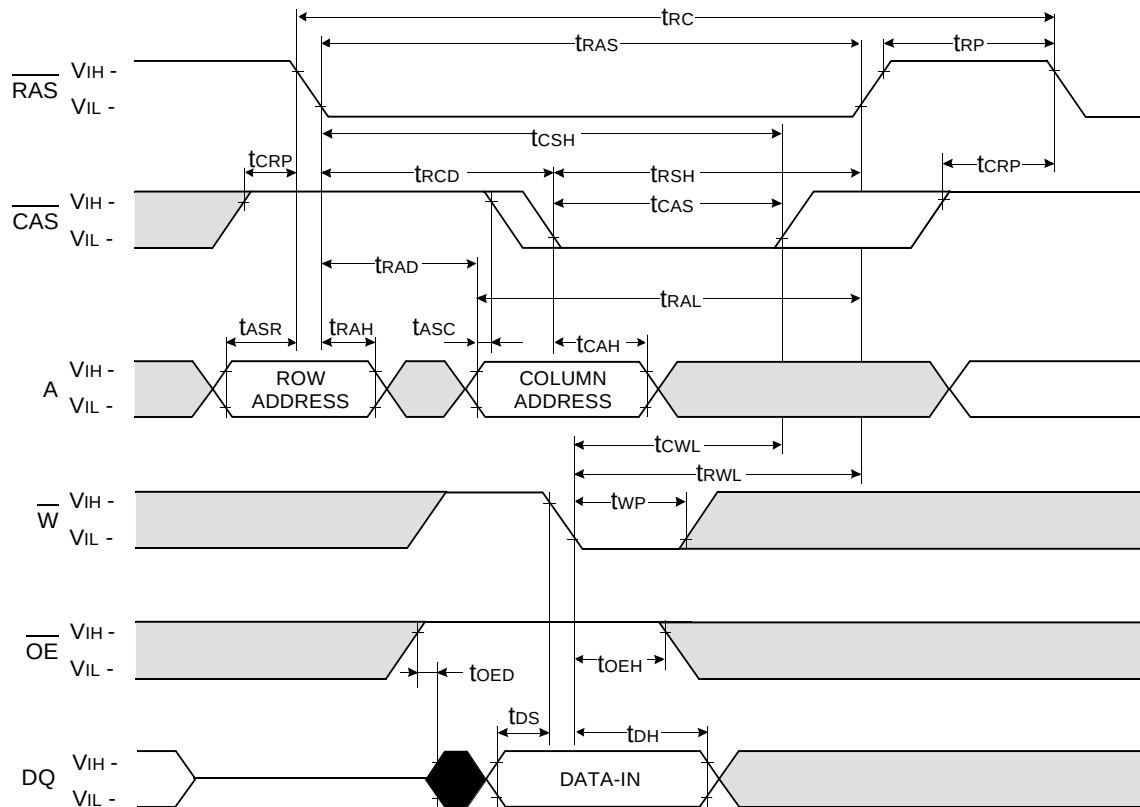
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

KMM5364005CSW/CSWG

Undefined

[illegible]

 Don't care

 Undefined

The diagram illustrates the timing relationships for a memory device. The signals shown are:

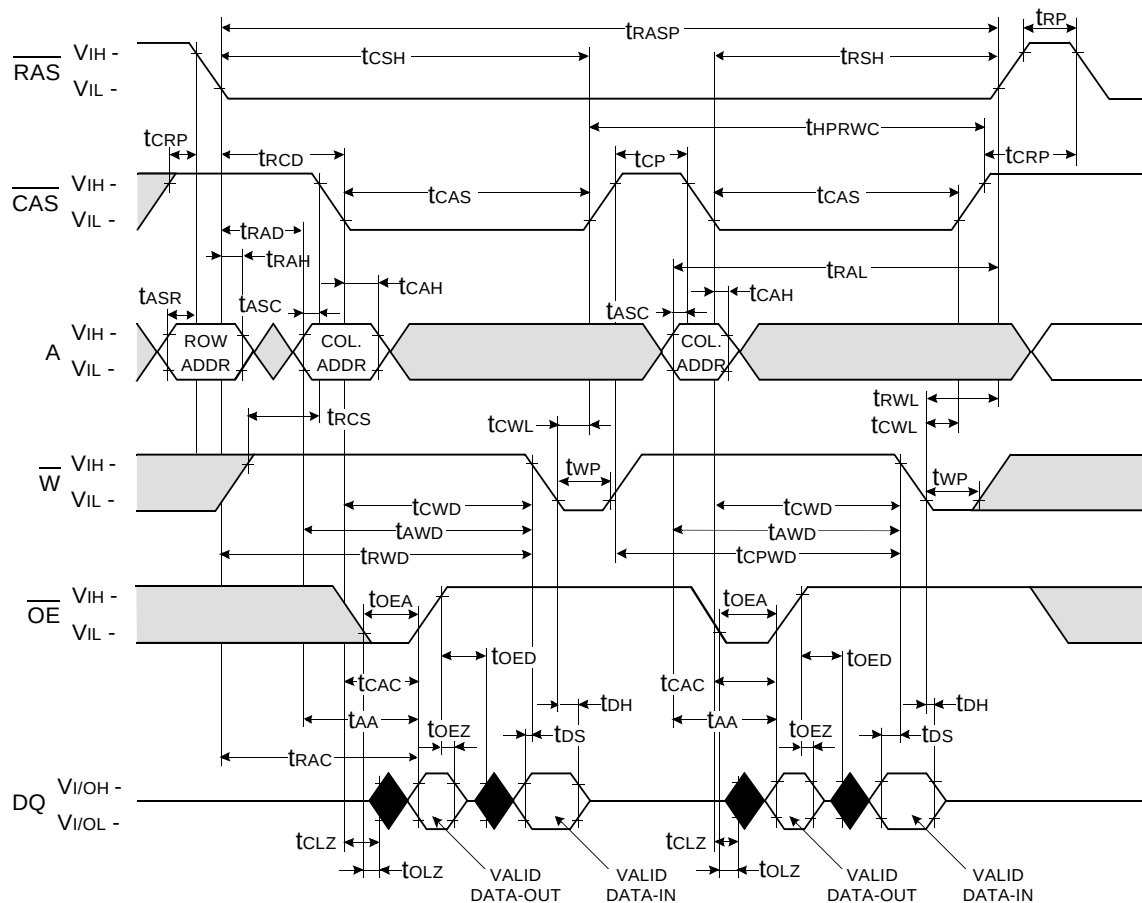
- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- A**: Address bus, showing ROW ADDRESS and COLUMN ADDRESS phases.
- W**: Write Enable, active low.
- OE**: Output Enable, active low.
- DQ**: Data bus, showing OPEN and DATA-OUT states.

Key timing parameters are indicated by arrows:

- t_{TRC}**: Row to Column delay.
- t_{RP}**: Row precharge time.
- t_{CRP}**: Column to Row precharge time.
- t_{CSH}**: Column Strobe High time.
- t_{RSH}**: Row Strobe High time.
- t_{CAS}**: Column Address Strobe time.
- t_{RAD}**: Row Address Delay.
- t_{ASR}**: Address Strobe Rise time.
- t_{RAH}**: Row Address Hold time.
- t_{ASC}**: Address Strobe Fall time.
- t_{CAH}**: Column Address Hold time.
- t_{RAL}**: Row Address Latency.
- t_{RCS}**: Row to Column Strobe delay.
- t_{AA}**: Array Access time.
- t_{OEA}**: Output Enable to Array Access delay.
- t_{OLZ}**: Output Latency time.
- t_{CAC}**: Column Address to Array Access delay.
- t_{CLZ}**: Column Latency time.
- t_{TRH}**: Tri-state High time.
- t_{RRH}**: Row to Row High time.
- t_{TCH}**: Tri-state to Column High time.
- t_{WEZ}**: Write Enable to Array Access delay.
- t_{CEZ}**: Column Enable to Array Access delay.
- t_{TOEZ}**: Tri-state to Output Enable delay.
- t_{TREZ}**: Tri-state to Row Enable delay.
- t_{TRC}**: Tri-state to Row to Column delay.

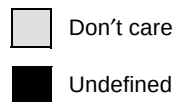


HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care
Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE



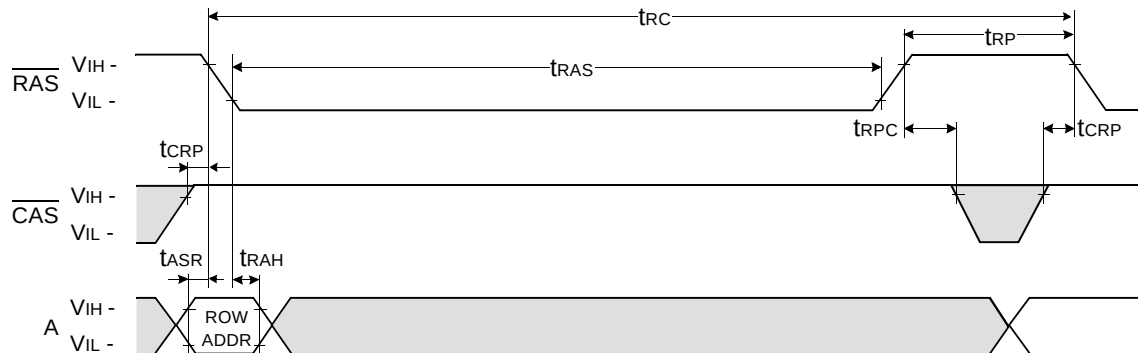
DRAM MODULE

KMM5364005CSW/CSWG

RAS - ONLY REFRESH CYCLE*

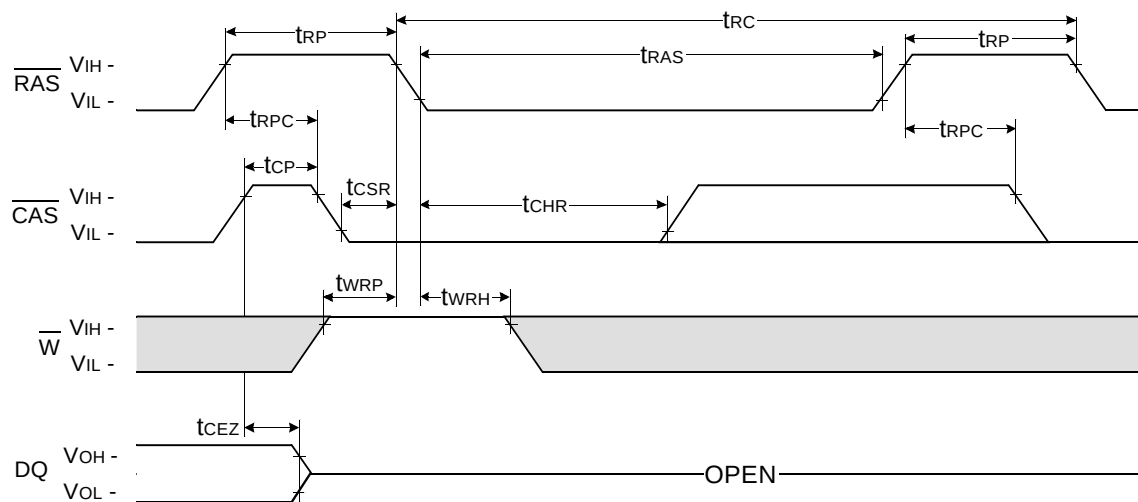
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

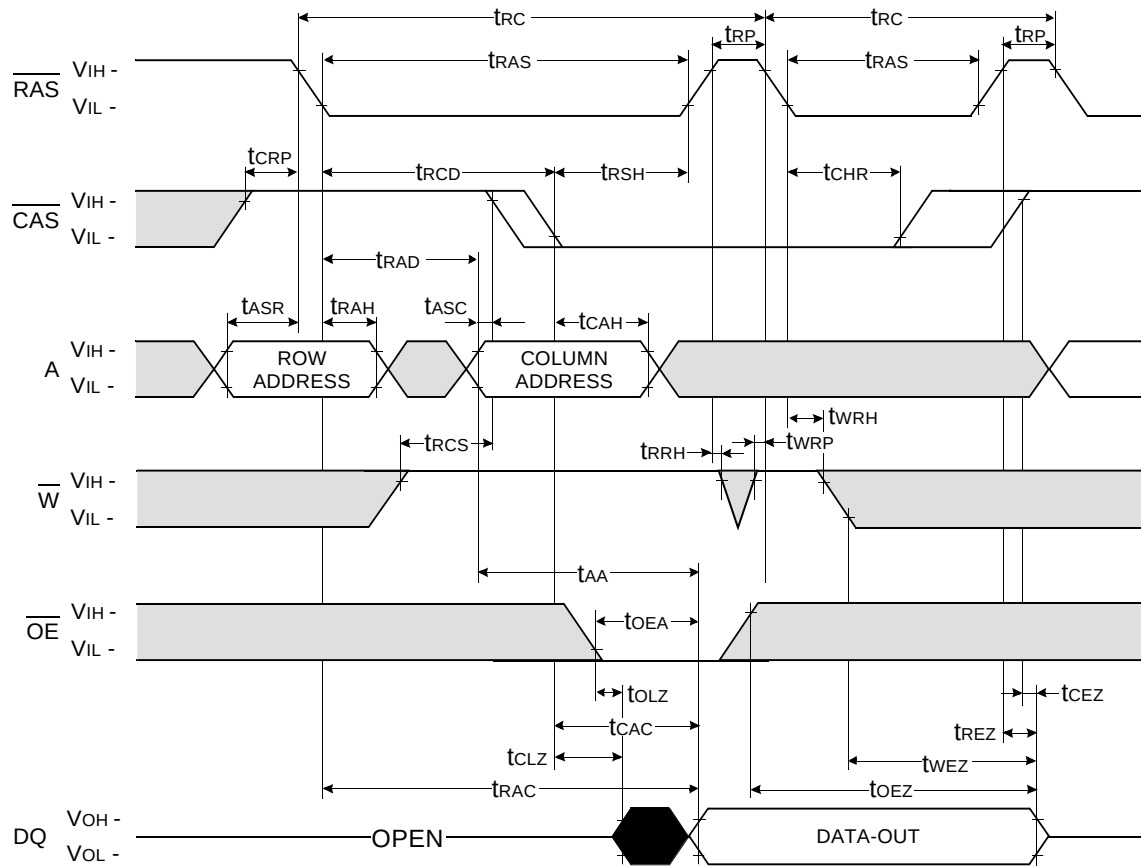
NOTE : $\overline{OE}$, A = Don't care

☐ Don't care

Undefined

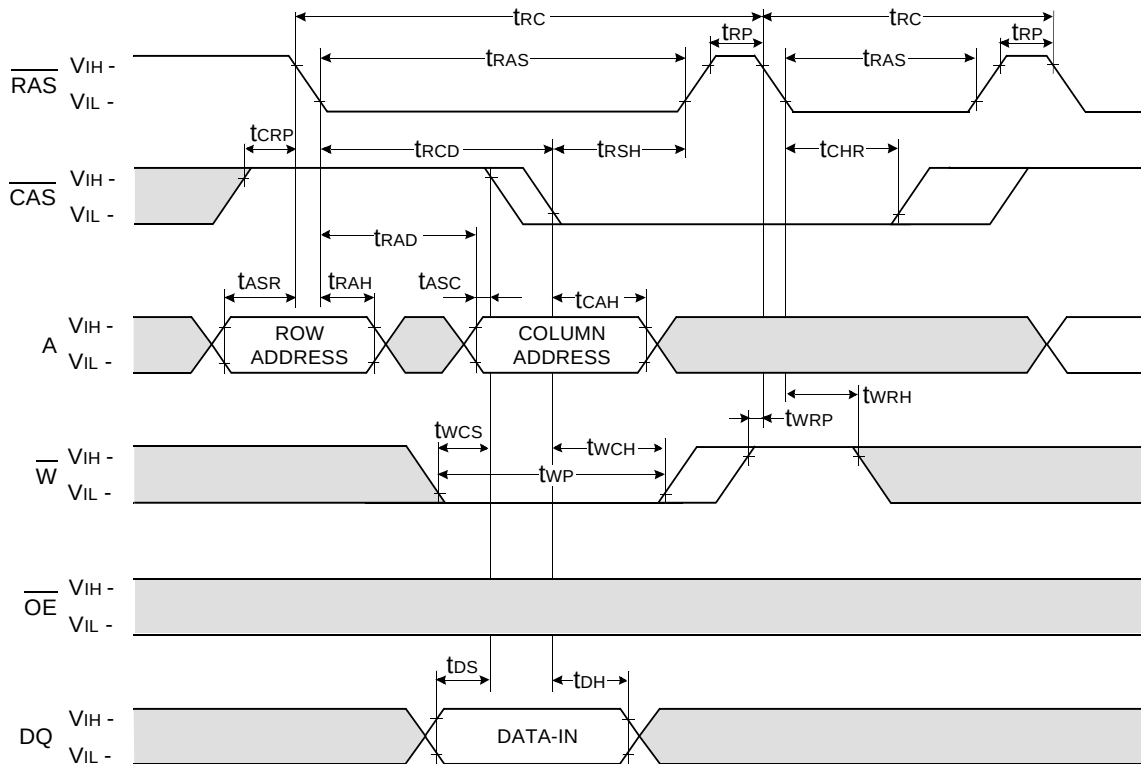
* In RAS-only refresh cycle of 64Mb A-dile & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



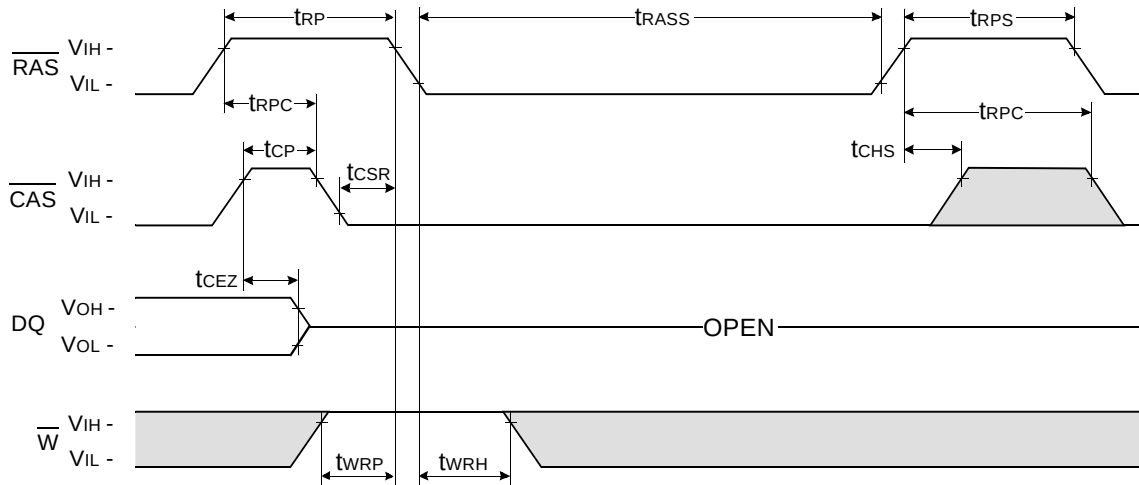
Don't care
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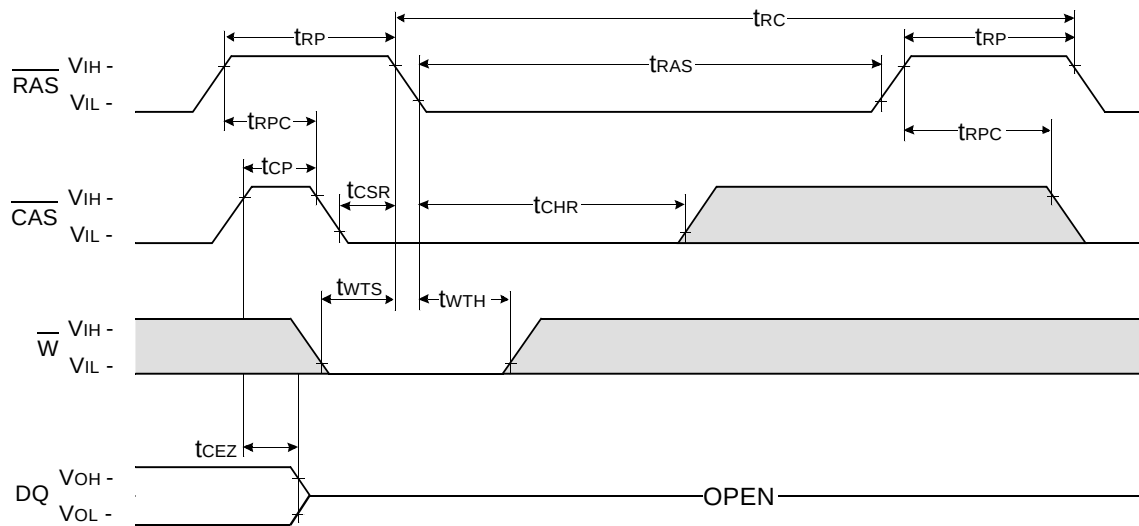
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



Don't care

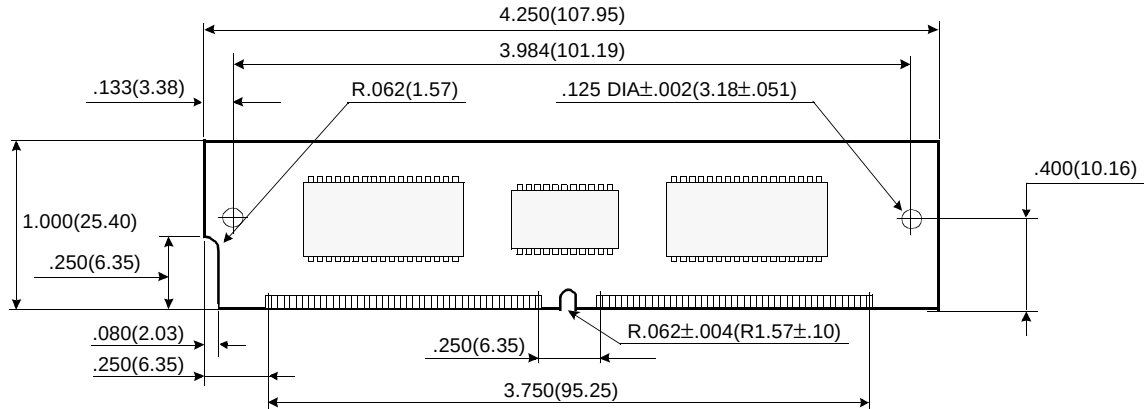
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DRAM MODULE

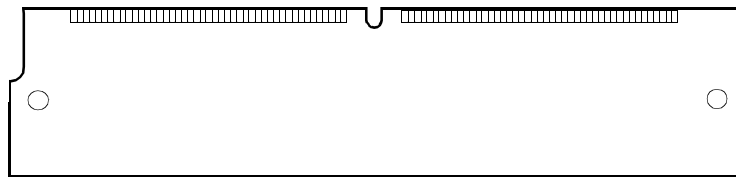
KMM5364005CSW/CSWG

PACKAGE DIMENSIONS

Units : Inches (millimeters)

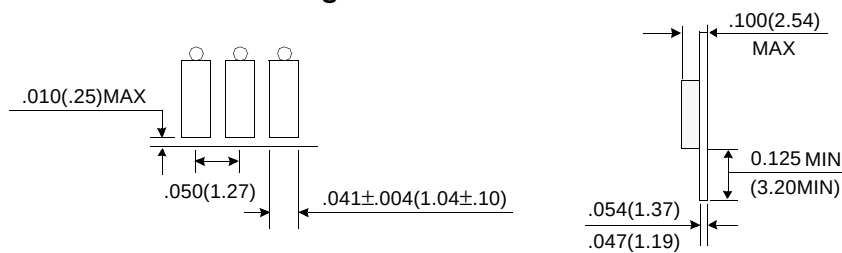


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 & Quad CAS 4Mx4 DRAM, TSOPII

DRAM Part No. : KMM5364005CSW/CSWG -- KM416C4104CS & KM44C4005CS(300 mil)