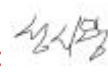


# KS0678

## 6 BIT 420 CHANNEL TFT-LCD SOURCE DRIVER

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Ver. 0.2

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| KS0678 Specification Revision History |                                          |          |
|---------------------------------------|------------------------------------------|----------|
| Version                               | Content                                  | Date     |
| 0.0                                   | Original                                 | Aug.1999 |
| 0.1                                   | The content of page 17 has been modified | Aug.1999 |
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## INTRODUCTION

The KS0678 is a 420 channel output, TFT-LCD source driver for 64 gray scale displays. Data input is based on digital input consisting of 6 bits by 6 dots, which can realize a full-color display of 260,000 colors by output of 64 values gamma-corrected.

This device has an internal D/A (Digital-to-Analog) converter for each output and 10 (5-by-2) external power supplies. Because the output dynamic range is as large as 4.8 - 7.8 Vp-p, it is unnecessary to operate level inversion of the LCD's common electrode. Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray scale voltages with different polarity can be output to the odd number output pins and the even output pins.

KS0678 can be adopted to larger panel, and SHL (shift direction selection) pin makes use of the LCD panel connection conveniently. Maximum operation clock frequency is 45 MHz at a 2.7 V logic operation. it can be applied to the TFT-LCD panel of SXGA+(1400 \* RGB) standards.

## FEATURES

- TFT active matrix LCD source driver LSI
- 64 Gary-scale is possible through 10 (5 by 2) external power supply and D/A converter
- Both dot inversion display and N-line inversion display are possible
- CMOS level input
- Compatible with gamma-correction
- Input data inversion function (DATPOL1, 2)
- Logic supply voltage: 2.7 - 3.6 V
- LCD driver supply voltage: 5.0 - 8.0 V
- Output dynamic range: 4.8 - 7.8 Vp-p
- Maximum operating frequency: fMAX = 45 MHz (internal data transmission rate at 2.7 V operation)
- Output: 420 outputs
- TCP

## BLOCK DIAGRAM

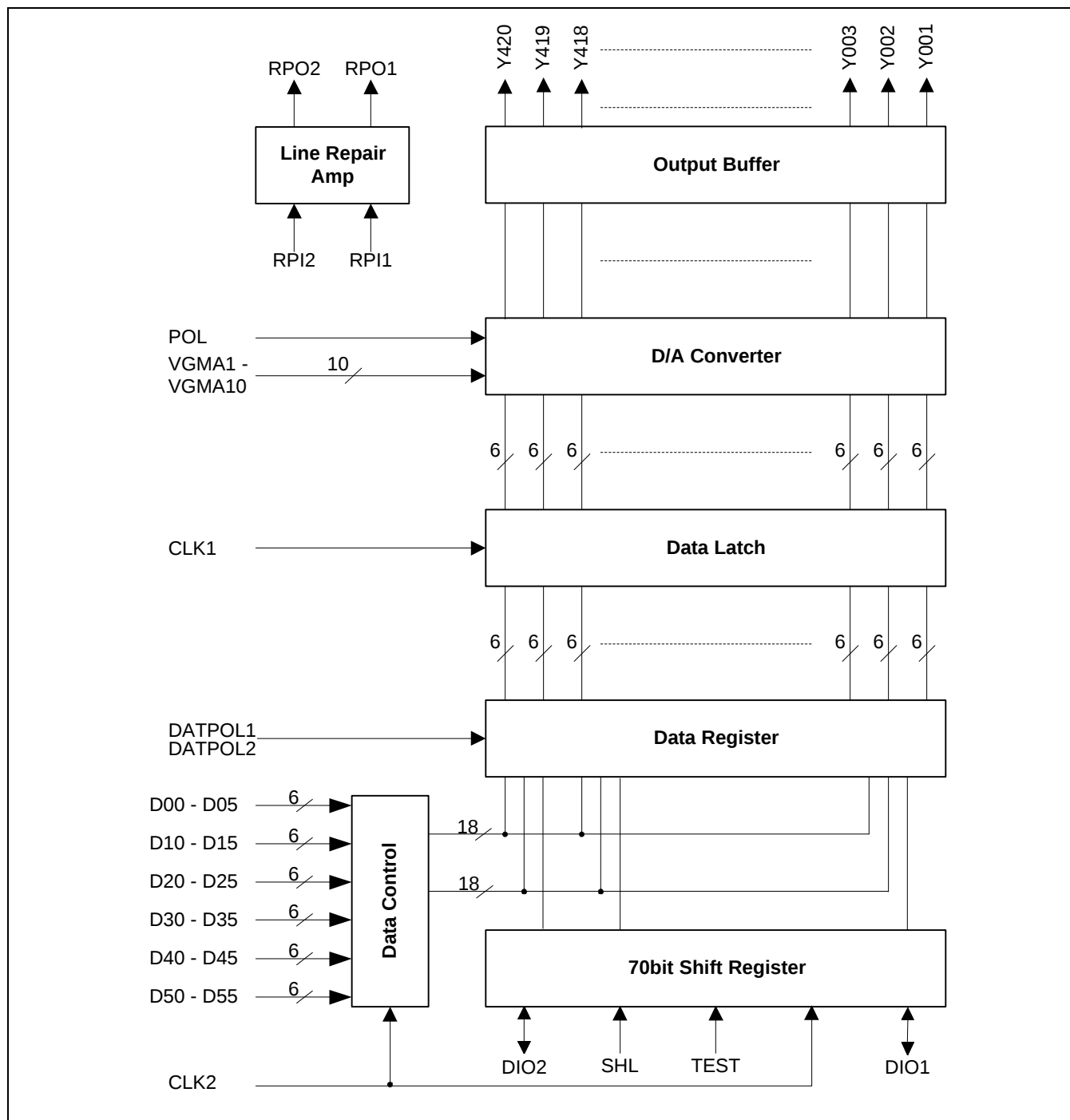


Figure 1. KS0678 Block Diagram

PIN ASSIGNMENTS

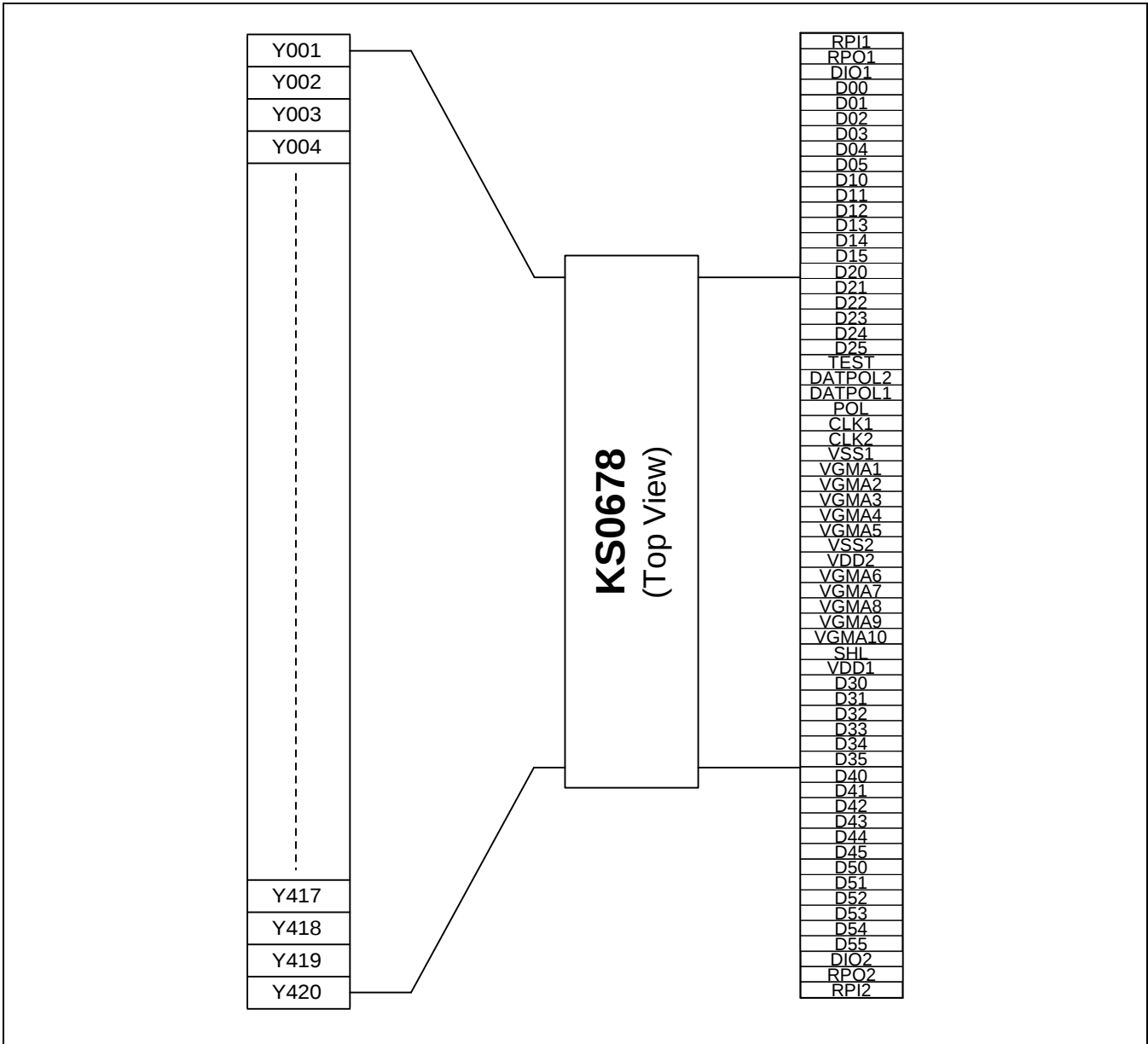


Figure 2. KS0678 Pin Assignments

## PIN DESCRIPTIONS

| Symbol                   | Pin Name                       | Description                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD1                     | Logic power supply             | 2.7 - 3.6 V                                                                                                                                                                                                                                                                                                                                                                                                       |
| VDD2                     | Driver power supply            | 5.0 - 8.0 V                                                                                                                                                                                                                                                                                                                                                                                                       |
| VSS1                     | Logic ground                   | Ground (0 V)                                                                                                                                                                                                                                                                                                                                                                                                      |
| VSS2                     | Driver ground                  | Ground (0 V)                                                                                                                                                                                                                                                                                                                                                                                                      |
| Y1 to Y420               | Driver outputs                 | The D/A converted 64 gray-scale analog voltage is output.                                                                                                                                                                                                                                                                                                                                                         |
| D0<0:5><br>- D5<0:5>     | Display data input             | The display data is input with a width of 36 bits, gray-scale data (6 bits) by 6 dots (R,G,B) DX0: LSB, DX5: MSB                                                                                                                                                                                                                                                                                                  |
| SHL                      | Shift direction control input  | This pin controls the direction of shift register in cascade connection. The shift direction of the shift registers is as follows.<br>SHL = H: DIO1 input, Y1 → Y420, DIO2 output<br>SHL = L: DIO2 input, Y420 → Y1, DIO1 output                                                                                                                                                                                  |
| DIO1                     | Start pulse input / output     | SHL = H: Used as the start pulse input pin.<br>SHL = L: Used as the start pulse output pin.                                                                                                                                                                                                                                                                                                                       |
| DIO2                     | Start pulse input / output     | SHL = H: Used as the start pulse output pin.<br>SHL = L: Used as the start pulse input pin.                                                                                                                                                                                                                                                                                                                       |
| DATPOL1<br>DATPOL2       | Data inversion input           | DATPOL1, 2 = L: Display data is not inverted<br>DATPOL1 = H: Display data of D0<0:5> - D2<0:5> is inverted<br>DATPOL2 = H: Display data of D3<0:5> - D5<0:5> is inverted                                                                                                                                                                                                                                          |
| POL                      | Polarity input                 | POL = H: The reference voltage for odd number outputs are VGMA1 – VGMA5 and those for even number outputs are VGMA6 – VGMA10.<br>POL = L: The reference voltage for odd number outputs are VGMA6 – VGMA10 and those for even number outputs are VGMA1 – VGMA5.                                                                                                                                                    |
| CLK2                     | Shift clock input              | Refer to the shift register's shift clock input. The display data is loaded to the data register at the rising edge of CLK2.                                                                                                                                                                                                                                                                                      |
| CLK1                     | Latch input                    | Latches the contents of the data register at rising edge and transfers them to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the "Relationships between CLK1 start pulse (DIO1, DIO2) and blanking period" of the switching characteristic waveform. Outputs the G/S data at falling edge. |
| VGMA1<br>–<br>VGMA10     | Gamma corrected power supplies | Input the gamma corrected power supplies from external source.<br>VDD2 > VGMA1 > VGMA2 > ..... > VGMA9 > VGMA10 > VSS2<br>Keep gray-scale power supply unchanged during the gray-scale voltage output.                                                                                                                                                                                                            |
| RPI1, RPO1<br>RPI2, RPO2 | Line-repair AMP input / output | The Structure of the line-repair amp is the same as that of the analog output.<br>RPI1 (RPI2) → impedance changed → RPO1 (RPO2)                                                                                                                                                                                                                                                                                   |
| TEST                     | Test input                     | TEST = L: Normal operation mode<br>TEST = H: Test mode (OP AMP CUT-OFF, Rpd = 15kΩ)                                                                                                                                                                                                                                                                                                                               |

## OPERATION DESCRIPTION

### DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into internal latch on the rising edge of CLK2, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the next rising edge of CLK2. Once all the data of 420 channels are loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd rising edge of CLK2 after the rising edge of DIO1 (or DIO2).

### EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

(1) SHL = "L"

Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

(2) SHL = "H"

Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

### RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 10 (5 by 2) gamma corrected power supplies (VGMA1 - VGMA10). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 5-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 5 gamma corrected voltages of VGMA1 - VGMA5 and VGMA6 - VGMA10.

|         |           |           |           |       |           |           |           |
|---------|-----------|-----------|-----------|-------|-----------|-----------|-----------|
| SHL = H |           |           |           |       |           |           |           |
| OUTPUT  | Y1        | Y2        | Y3        | ..... | Y418      | Y419      | Y420      |
| -       | First     |           |           | →     | Last      |           |           |
| DATA    | D00 - D05 | D10 - D15 | D20 - D25 | ..... | D30 - D35 | D40 - D45 | D50 - D55 |

|         |           |           |           |       |           |           |           |
|---------|-----------|-----------|-----------|-------|-----------|-----------|-----------|
| SHL = L |           |           |           |       |           |           |           |
| OUTPUT  | Y1        | Y2        | Y3        | ..... | Y418      | Y419      | Y420      |
| -       | Last      |           |           | ←     | First     |           |           |
| DATA    | D00 - D05 | D10 - D15 | D20 - D25 | ..... | D30 - D35 | D40 - D45 | D50 - D55 |

Figure 3. Relationship between Shift Direction and Output Data

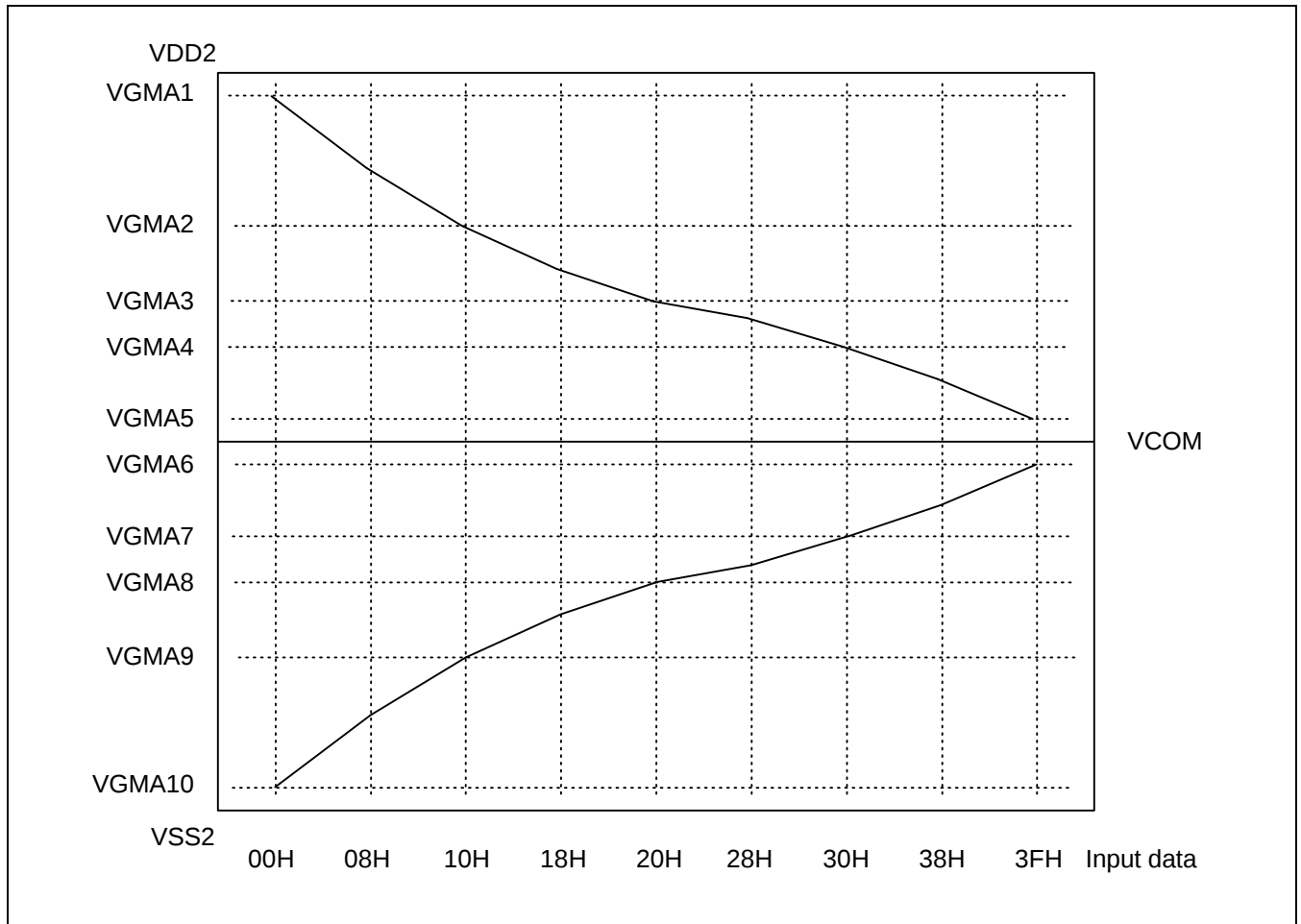


Figure 4. Gamma Correction Curve

Table 1. Resistor Strings (R0 - R62, unit:  $\Omega$ )

| Name | Value | Name | Value | Name | Value | Name | Value |
|------|-------|------|-------|------|-------|------|-------|
| R0   | 500   | R16  | 330   | R32  | 175   | R48  | 210   |
| R1   | 500   | R17  | 330   | R33  | 175   | R49  | 220   |
| R2   | 500   | R18  | 330   | R34  | 170   | R50  | 230   |
| R3   | 500   | R19  | 320   | R35  | 170   | R51  | 240   |
| R4   | 500   | R20  | 300   | R36  | 165   | R52  | 250   |
| R5   | 500   | R21  | 280   | R37  | 165   | R53  | 260   |
| R6   | 500   | R22  | 270   | R38  | 165   | R54  | 270   |
| R7   | 500   | R23  | 260   | R39  | 165   | R55  | 290   |
| R8   | 500   | R24  | 250   | R40  | 170   | R56  | 300   |
| R9   | 500   | R25  | 240   | R41  | 170   | R57  | 310   |
| R10  | 500   | R26  | 230   | R42  | 170   | R58  | 320   |
| R11  | 500   | R27  | 220   | R43  | 175   | R59  | 340   |
| R12  | 450   | R28  | 210   | R44  | 175   | R60  | 340   |
| R13  | 450   | R29  | 200   | R45  | 175   | R61  | 340   |
| R14  | 400   | R30  | 190   | R46  | 180   | R62  | 340   |
| R15  | 370   | R31  | 180   | R47  | 200   |      |       |

Table 2. Relationship between Input Data and Output Voltage Value

| Input data | DX5 | DX4 | DX3 | DX2 | DX1 | DX0 | G/S  | Output voltage                               |
|------------|-----|-----|-----|-----|-----|-----|------|----------------------------------------------|
| 00H        | 0   | 0   | 0   | 0   | 0   | 0   | VH0  | VGMA1                                        |
| 01H        | 0   | 0   | 0   | 0   | 0   | 1   | VH1  | $VGMA1 + (VGMA2 - VGMA1) \times 500 / 7670$  |
| 02H        | 0   | 0   | 0   | 0   | 1   | 0   | VH2  | $VGMA1 + (VGMA2 - VGMA1) \times 1000 / 7670$ |
| 03H        | 0   | 0   | 0   | 0   | 1   | 1   | VH3  | $VGMA1 + (VGMA2 - VGMA1) \times 1500 / 7670$ |
| 04H        | 0   | 0   | 0   | 1   | 0   | 0   | VH4  | $VGMA1 + (VGMA2 - VGMA1) \times 2000 / 7670$ |
| 05H        | 0   | 0   | 0   | 1   | 0   | 1   | VH5  | $VGMA1 + (VGMA2 - VGMA1) \times 2500 / 7670$ |
| 06H        | 0   | 0   | 0   | 1   | 1   | 0   | VH6  | $VGMA1 + (VGMA2 - VGMA1) \times 3000 / 7670$ |
| 07H        | 0   | 0   | 0   | 1   | 1   | 1   | VH7  | $VGMA1 + (VGMA2 - VGMA1) \times 3500 / 7670$ |
| 08H        | 0   | 0   | 1   | 0   | 0   | 0   | VH8  | $VGMA1 + (VGMA2 - VGMA1) \times 4000 / 7670$ |
| 09H        | 0   | 0   | 1   | 0   | 0   | 1   | VH9  | $VGMA1 + (VGMA2 - VGMA1) \times 4500 / 7670$ |
| 0AH        | 0   | 0   | 1   | 0   | 1   | 0   | VH10 | $VGMA1 + (VGMA2 - VGMA1) \times 5000 / 7670$ |
| 0BH        | 0   | 0   | 1   | 0   | 1   | 1   | VH11 | $VGMA1 + (VGMA2 - VGMA1) \times 5500 / 7670$ |
| 0CH        | 0   | 0   | 1   | 1   | 0   | 0   | VH12 | $VGMA1 + (VGMA2 - VGMA1) \times 6000 / 7670$ |
| 0DH        | 0   | 0   | 1   | 1   | 0   | 1   | VH13 | $VGMA1 + (VGMA2 - VGMA1) \times 6450 / 7670$ |
| 0EH        | 0   | 0   | 1   | 1   | 1   | 0   | VH14 | $VGMA1 + (VGMA2 - VGMA1) \times 6900 / 7670$ |
| 0FH        | 0   | 0   | 1   | 1   | 1   | 1   | VH15 | $VGMA1 + (VGMA2 - VGMA1) \times 7300 / 7670$ |
| 10H        | 0   | 1   | 0   | 0   | 0   | 0   | VH16 | VGMA2                                        |
| 11H        | 0   | 1   | 0   | 0   | 0   | 1   | VH17 | $VGMA2 + (VGMA3 - VGMA2) \times 330 / 4140$  |
| 12H        | 0   | 1   | 0   | 0   | 1   | 0   | VH18 | $VGMA2 + (VGMA3 - VGMA2) \times 660 / 4140$  |
| 13H        | 0   | 1   | 0   | 0   | 1   | 1   | VH19 | $VGMA2 + (VGMA3 - VGMA2) \times 990 / 4140$  |
| 14H        | 0   | 1   | 0   | 1   | 0   | 0   | VH20 | $VGMA2 + (VGMA3 - VGMA2) \times 1310 / 4140$ |
| 15H        | 0   | 1   | 0   | 1   | 0   | 1   | VH21 | $VGMA2 + (VGMA3 - VGMA2) \times 1610 / 4140$ |
| 16H        | 0   | 1   | 0   | 1   | 1   | 0   | VH22 | $VGMA2 + (VGMA3 - VGMA2) \times 1890 / 4140$ |
| 17H        | 0   | 1   | 0   | 1   | 1   | 1   | VH23 | $VGMA2 + (VGMA3 - VGMA2) \times 2160 / 4140$ |
| 18H        | 0   | 1   | 1   | 0   | 0   | 0   | VH24 | $VGMA2 + (VGMA3 - VGMA2) \times 2420 / 4140$ |
| 19H        | 0   | 1   | 1   | 0   | 0   | 1   | VH25 | $VGMA2 + (VGMA3 - VGMA2) \times 2670 / 4140$ |
| 1AH        | 0   | 1   | 1   | 0   | 1   | 0   | VH26 | $VGMA2 + (VGMA3 - VGMA2) \times 2910 / 4140$ |
| 1BH        | 0   | 1   | 1   | 0   | 1   | 1   | VH27 | $VGMA2 + (VGMA3 - VGMA2) \times 3140 / 4140$ |
| 1CH        | 0   | 1   | 1   | 1   | 0   | 0   | VH28 | $VGMA2 + (VGMA3 - VGMA2) \times 3360 / 4140$ |
| 1DH        | 0   | 1   | 1   | 1   | 0   | 1   | VH29 | $VGMA2 + (VGMA3 - VGMA2) \times 3570 / 4140$ |
| 1EH        | 0   | 1   | 1   | 1   | 1   | 0   | VH30 | $VGMA2 + (VGMA3 - VGMA2) \times 3770 / 4140$ |
| 1FH        | 0   | 1   | 1   | 1   | 1   | 1   | VH31 | $VGMA2 + (VGMA3 - VGMA2) \times 3960 / 4140$ |

NOTE:  $VDD2 > VGMA1 > VGMA2 > VGMA3 > VGMA4 > VGMA5$

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

| Input data | DX5 | DX4 | DX3 | DX2 | DX1 | DX0 | G/S  | Output voltage                               |
|------------|-----|-----|-----|-----|-----|-----|------|----------------------------------------------|
| 20H        | 1   | 0   | 0   | 0   | 0   | 0   | VH32 | VGMA3                                        |
| 21H        | 1   | 0   | 0   | 0   | 0   | 1   | VH33 | $VGMA3 + (VGMA4 - VGMA3) \times 175 / 2765$  |
| 22H        | 1   | 0   | 0   | 0   | 1   | 0   | VH34 | $VGMA3 + (VGMA4 - VGMA3) \times 350 / 2765$  |
| 23H        | 1   | 0   | 0   | 0   | 1   | 1   | VH35 | $VGMA3 + (VGMA4 - VGMA3) \times 520 / 2765$  |
| 24H        | 1   | 0   | 0   | 1   | 0   | 0   | VH36 | $VGMA3 + (VGMA4 - VGMA3) \times 690 / 2765$  |
| 25H        | 1   | 0   | 0   | 1   | 0   | 1   | VH37 | $VGMA3 + (VGMA4 - VGMA3) \times 855 / 2765$  |
| 26H        | 1   | 0   | 0   | 1   | 1   | 0   | VH38 | $VGMA3 + (VGMA4 - VGMA3) \times 020 / 2765$  |
| 27H        | 1   | 0   | 0   | 1   | 1   | 1   | VH39 | $VGMA3 + (VGMA4 - VGMA3) \times 1185 / 2765$ |
| 28H        | 1   | 0   | 1   | 0   | 0   | 0   | VH40 | $VGMA3 + (VGMA4 - VGMA3) \times 1350 / 2765$ |
| 29H        | 1   | 0   | 1   | 0   | 0   | 1   | VH41 | $VGMA3 + (VGMA4 - VGMA3) \times 1520 / 2765$ |
| 2AH        | 1   | 0   | 1   | 0   | 1   | 0   | VH42 | $VGMA3 + (VGMA4 - VGMA3) \times 1690 / 2765$ |
| 2BH        | 1   | 0   | 1   | 0   | 1   | 1   | VH43 | $VGMA3 + (VGMA4 - VGMA3) \times 1860 / 2765$ |
| 2CH        | 1   | 0   | 1   | 1   | 0   | 0   | VH44 | $VGMA3 + (VGMA4 - VGMA3) \times 2035 / 2765$ |
| 2DH        | 1   | 0   | 1   | 1   | 0   | 1   | VH45 | $VGMA3 + (VGMA4 - VGMA3) \times 2210 / 2765$ |
| 2EH        | 1   | 0   | 1   | 1   | 1   | 0   | VH46 | $VGMA3 + (VGMA4 - VGMA3) \times 2385 / 2765$ |
| 2FH        | 1   | 0   | 1   | 1   | 1   | 1   | VH47 | $VGMA3 + (VGMA4 - VGMA3) \times 2565 / 2765$ |
| 30H        | 1   | 1   | 0   | 0   | 0   | 0   | VH48 | VGMA4                                        |
| 31H        | 1   | 1   | 0   | 0   | 0   | 1   | VH49 | $VGMA4 + (VGMA5 - VGMA4) \times 210 / 4260$  |
| 32H        | 1   | 1   | 0   | 0   | 1   | 0   | VH50 | $VGMA4 + (VGMA5 - VGMA4) \times 430 / 4260$  |
| 33H        | 1   | 1   | 0   | 0   | 1   | 1   | VH51 | $VGMA4 + (VGMA5 - VGMA4) \times 660 / 4260$  |
| 34H        | 1   | 1   | 0   | 1   | 0   | 0   | VH52 | $VGMA4 + (VGMA5 - VGMA4) \times 900 / 4260$  |
| 35H        | 1   | 1   | 0   | 1   | 0   | 1   | VH53 | $VGMA4 + (VGMA5 - VGMA4) \times 1150 / 4260$ |
| 36H        | 1   | 1   | 0   | 1   | 1   | 0   | VH54 | $VGMA4 + (VGMA5 - VGMA4) \times 1410 / 4260$ |
| 37H        | 1   | 1   | 0   | 1   | 1   | 1   | VH55 | $VGMA4 + (VGMA5 - VGMA4) \times 1680 / 4260$ |
| 38H        | 1   | 1   | 1   | 0   | 0   | 0   | VH56 | $VGMA4 + (VGMA5 - VGMA4) \times 1970 / 4260$ |
| 39H        | 1   | 1   | 1   | 0   | 0   | 1   | VH57 | $VGMA4 + (VGMA5 - VGMA4) \times 2270 / 4260$ |
| 3AH        | 1   | 1   | 1   | 0   | 1   | 0   | VH58 | $VGMA4 + (VGMA5 - VGMA4) \times 2580 / 4260$ |
| 3BH        | 1   | 1   | 1   | 0   | 1   | 1   | VH59 | $VGMA4 + (VGMA5 - VGMA4) \times 2900 / 4260$ |
| 3CH        | 1   | 1   | 1   | 1   | 0   | 0   | VH60 | $VGMA4 + (VGMA5 - VGMA4) \times 3240 / 4260$ |
| 3DH        | 1   | 1   | 1   | 1   | 0   | 1   | VH61 | $VGMA4 + (VGMA5 - VGMA4) \times 3580 / 4260$ |
| 3EH        | 1   | 1   | 1   | 1   | 1   | 0   | VH62 | $VGMA4 + (VGMA5 - VGMA4) \times 3920 / 4260$ |
| 3FH        | 1   | 1   | 1   | 1   | 1   | 1   | VH63 | VGMA5                                        |

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

| Input data | DX5 | DX4 | DX3 | DX2 | DX1 | DX0 | G/S  | Output voltage                                 |
|------------|-----|-----|-----|-----|-----|-----|------|------------------------------------------------|
| 00H        | 0   | 0   | 0   | 0   | 0   | 0   | VL0  | VGMA10                                         |
| 01H        | 0   | 0   | 0   | 0   | 0   | 1   | VL1  | $VGMA10 + (VGMA9 - VGMA10) \times 500 / 7670$  |
| 02H        | 0   | 0   | 0   | 0   | 1   | 0   | VL2  | $VGMA10 + (VGMA9 - VGMA10) \times 1000 / 7670$ |
| 03H        | 0   | 0   | 0   | 0   | 1   | 1   | VL3  | $VGMA10 + (VGMA9 - VGMA10) \times 1500 / 7670$ |
| 04H        | 0   | 0   | 0   | 1   | 0   | 0   | VL4  | $VGMA10 + (VGMA9 - VGMA10) \times 2000 / 7670$ |
| 05H        | 0   | 0   | 0   | 1   | 0   | 1   | VL5  | $VGMA10 + (VGMA9 - VGMA10) \times 2500 / 7670$ |
| 06H        | 0   | 0   | 0   | 1   | 1   | 0   | VL6  | $VGMA10 + (VGMA9 - VGMA10) \times 3000 / 7670$ |
| 07H        | 0   | 0   | 0   | 1   | 1   | 1   | VL7  | $VGMA10 + (VGMA9 - VGMA10) \times 3500 / 7670$ |
| 08H        | 0   | 0   | 1   | 0   | 0   | 0   | VL8  | $VGMA10 + (VGMA9 - VGMA10) \times 4000 / 7670$ |
| 09H        | 0   | 0   | 1   | 0   | 0   | 1   | VL9  | $VGMA10 + (VGMA9 - VGMA10) \times 4500 / 7670$ |
| 0AH        | 0   | 0   | 1   | 0   | 1   | 0   | VL10 | $VGMA10 + (VGMA9 - VGMA10) \times 5000 / 7670$ |
| 0BH        | 0   | 0   | 1   | 0   | 1   | 1   | VL11 | $VGMA10 + (VGMA9 - VGMA10) \times 5500 / 7670$ |
| 0CH        | 0   | 0   | 1   | 1   | 0   | 0   | VL12 | $VGMA10 + (VGMA9 - VGMA10) \times 6000 / 7670$ |
| 0DH        | 0   | 0   | 1   | 1   | 0   | 1   | VL13 | $VGMA10 + (VGMA9 - VGMA10) \times 6450 / 7670$ |
| 0EH        | 0   | 0   | 1   | 1   | 1   | 0   | VL14 | $VGMA10 + (VGMA9 - VGMA10) \times 6900 / 7670$ |
| 0FH        | 0   | 0   | 1   | 1   | 1   | 1   | VL15 | $VGMA10 + (VGMA9 - VGMA10) \times 7300 / 7670$ |
| 10H        | 0   | 1   | 0   | 0   | 0   | 0   | VL16 | VGMA9                                          |
| 11H        | 0   | 1   | 0   | 0   | 0   | 1   | VL17 | $VGMA9 + (VGMA8 - VGMA9) \times 330 / 4140$    |
| 12H        | 0   | 1   | 0   | 0   | 1   | 0   | VL18 | $VGMA9 + (VGMA8 - VGMA9) \times 660 / 4140$    |
| 13H        | 0   | 1   | 0   | 0   | 1   | 1   | VL19 | $VGMA9 + (VGMA8 - VGMA9) \times 990 / 4140$    |
| 14H        | 0   | 1   | 0   | 1   | 0   | 0   | VL20 | $VGMA9 + (VGMA8 - VGMA9) \times 1310 / 4140$   |
| 15H        | 0   | 1   | 0   | 1   | 0   | 1   | VL21 | $VGMA9 + (VGMA8 - VGMA9) \times 1610 / 4140$   |
| 16H        | 0   | 1   | 0   | 1   | 1   | 0   | VL22 | $VGMA9 + (VGMA8 - VGMA9) \times 1890 / 4140$   |
| 17H        | 0   | 1   | 0   | 1   | 1   | 1   | VL23 | $VGMA9 + (VGMA8 - VGMA9) \times 2160 / 4140$   |
| 18H        | 0   | 1   | 1   | 0   | 0   | 0   | VL24 | $VGMA9 + (VGMA8 - VGMA9) \times 2420 / 4140$   |
| 19H        | 0   | 1   | 1   | 0   | 0   | 1   | VL25 | $VGMA9 + (VGMA8 - VGMA9) \times 2670 / 4140$   |
| 1AH        | 0   | 1   | 1   | 0   | 1   | 0   | VL26 | $VGMA9 + (VGMA8 - VGMA9) \times 2910 / 4140$   |
| 1BH        | 0   | 1   | 1   | 0   | 1   | 1   | VL27 | $VGMA9 + (VGMA8 - VGMA9) \times 3140 / 4140$   |
| 1CH        | 0   | 1   | 1   | 1   | 0   | 0   | VL28 | $VGMA9 + (VGMA8 - VGMA9) \times 3360 / 4140$   |
| 1DH        | 0   | 1   | 1   | 1   | 0   | 1   | VL29 | $VGMA9 + (VGMA8 - VGMA9) \times 3570 / 4140$   |
| 1EH        | 0   | 1   | 1   | 1   | 1   | 0   | VL30 | $VGMA9 + (VGMA8 - VGMA9) \times 3770 / 4140$   |
| 1FH        | 0   | 1   | 1   | 1   | 1   | 1   | VL31 | $VGMA9 + (VGMA8 - VGMA9) \times 3960 / 4140$   |

NOTE: VGMA6 &gt; VGMA7 &gt; VGMA8 &gt; VGMA9 &gt; VGMA10 &gt; VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

| Input data | DX5 | DX4 | DX3 | DX2 | DX1 | DX0 | G/S  | Output voltage                               |
|------------|-----|-----|-----|-----|-----|-----|------|----------------------------------------------|
| 20H        | 1   | 0   | 0   | 0   | 0   | 0   | VL32 | VGMA8                                        |
| 21H        | 1   | 0   | 0   | 0   | 0   | 1   | VL33 | $VGMA8 + (VGMA7 - VGMA8) \times 175 / 2765$  |
| 22H        | 1   | 0   | 0   | 0   | 1   | 0   | VL34 | $VGMA8 + (VGMA7 - VGMA8) \times 350 / 2765$  |
| 23H        | 1   | 0   | 0   | 0   | 1   | 1   | VL35 | $VGMA8 + (VGMA7 - VGMA8) \times 520 / 2765$  |
| 24H        | 1   | 0   | 0   | 1   | 0   | 0   | VL36 | $VGMA8 + (VGMA7 - VGMA8) \times 690 / 2765$  |
| 25H        | 1   | 0   | 0   | 1   | 0   | 1   | VL37 | $VGMA8 + (VGMA7 - VGMA8) \times 855 / 2765$  |
| 26H        | 1   | 0   | 0   | 1   | 1   | 0   | VL38 | $VGMA8 + (VGMA7 - VGMA8) \times 1020 / 2765$ |
| 27H        | 1   | 0   | 0   | 1   | 1   | 1   | VL39 | $VGMA8 + (VGMA7 - VGMA8) \times 1185 / 2765$ |
| 28H        | 1   | 0   | 1   | 0   | 0   | 0   | VL40 | $VGMA8 + (VGMA7 - VGMA8) \times 1350 / 2765$ |
| 29H        | 1   | 0   | 1   | 0   | 0   | 1   | VL41 | $VGMA8 + (VGMA7 - VGMA8) \times 1520 / 2765$ |
| 2AH        | 1   | 0   | 1   | 0   | 1   | 0   | VL42 | $VGMA8 + (VGMA7 - VGMA8) \times 1690 / 2765$ |
| 2BH        | 1   | 0   | 1   | 0   | 1   | 1   | VL43 | $VGMA8 + (VGMA7 - VGMA8) \times 1860 / 2765$ |
| 2CH        | 1   | 0   | 1   | 1   | 0   | 0   | VL44 | $VGMA8 + (VGMA7 - VGMA8) \times 2035 / 2765$ |
| 2DH        | 1   | 0   | 1   | 1   | 0   | 1   | VL45 | $VGMA8 + (VGMA7 - VGMA8) \times 2210 / 2765$ |
| 2EH        | 1   | 0   | 1   | 1   | 1   | 0   | VL46 | $VGMA8 + (VGMA7 - VGMA8) \times 2385 / 2765$ |
| 2FH        | 1   | 0   | 1   | 1   | 1   | 1   | VL47 | $VGMA8 + (VGMA7 - VGMA8) \times 2565 / 2765$ |
| 30H        | 1   | 1   | 0   | 0   | 0   | 0   | VL48 | VGMA7                                        |
| 31H        | 1   | 1   | 0   | 0   | 0   | 1   | VL49 | $VGMA7 + (VGMA6 - VGMA7) \times 210 / 4260$  |
| 32H        | 1   | 1   | 0   | 0   | 1   | 0   | VL50 | $VGMA7 + (VGMA6 - VGMA7) \times 430 / 4260$  |
| 33H        | 1   | 1   | 0   | 0   | 1   | 1   | VL51 | $VGMA7 + (VGMA6 - VGMA7) \times 660 / 4260$  |
| 34H        | 1   | 1   | 0   | 1   | 0   | 0   | VL52 | $VGMA7 + (VGMA6 - VGMA7) \times 900 / 4260$  |
| 35H        | 1   | 1   | 0   | 1   | 0   | 1   | VL53 | $VGMA7 + (VGMA6 - VGMA7) \times 1150 / 4260$ |
| 36H        | 1   | 1   | 0   | 1   | 1   | 0   | VL54 | $VGMA7 + (VGMA6 - VGMA7) \times 1410 / 4260$ |
| 37H        | 1   | 1   | 0   | 1   | 1   | 1   | VL55 | $VGMA7 + (VGMA6 - VGMA7) \times 1680 / 4260$ |
| 38H        | 1   | 1   | 1   | 0   | 0   | 0   | VL56 | $VGMA7 + (VGMA6 - VGMA7) \times 1970 / 4260$ |
| 39H        | 1   | 1   | 1   | 0   | 0   | 1   | VL57 | $VGMA7 + (VGMA6 - VGMA7) \times 2270 / 4260$ |
| 3AH        | 1   | 1   | 1   | 0   | 1   | 0   | VL58 | $VGMA7 + (VGMA6 - VGMA7) \times 2580 / 4260$ |
| 3BH        | 1   | 1   | 1   | 0   | 1   | 1   | VL59 | $VGMA7 + (VGMA6 - VGMA7) \times 2900 / 4260$ |
| 3CH        | 1   | 1   | 1   | 1   | 0   | 0   | VL60 | $VGMA7 + (VGMA6 - VGMA7) \times 3240 / 4260$ |
| 3DH        | 1   | 1   | 1   | 1   | 0   | 1   | VL61 | $VGMA7 + (VGMA6 - VGMA7) \times 3580 / 4260$ |
| 3EH        | 1   | 1   | 1   | 1   | 1   | 0   | VL62 | $VGMA7 + (VGMA6 - VGMA7) \times 3920 / 4260$ |
| 3FH        | 1   | 1   | 1   | 1   | 1   | 1   | VL63 | VGMA6                                        |

## ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

| Parameter                   | Symbol     | Ratings            | Unit |
|-----------------------------|------------|--------------------|------|
| Logic supply voltage        | VDD1       | -0.3 to 5.5        | V    |
| Driver supply voltage       | VDD2       | -0.3 to 9.0        | V    |
| Input voltage               | VGMA1 - 10 | -0.3 to VDD2 + 0.3 | V    |
|                             | RPI1, RPI2 | -0.3 to VDD2 + 0.3 |      |
|                             | Others     | -0.3 to VDD1 + 0.3 |      |
| Output voltage              | DIO1, 2    | -0.3 to VDD1 + 0.3 | V    |
|                             | Y1 to Y420 | -0.3 to VDD2 + 0.3 |      |
|                             | RPO1, RPO2 | -0.3 to VDD2 + 0.3 |      |
| Operating power dissipation | Pd         | 150                | mW   |
| Operation temperature       | Top        | -20 to 75          | °C   |
| Storage temperature         | Tstg       | -55 to 125         | °C   |

### CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 - VGMA10

or VDD1 & VDD2 → control signal input & VGMA1 - VGMA10

Turn off power order: VGMA1 - VGMA10 → VDD2 → control signal input → VDD1

## RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = -20 to 75 °C, VSS1 = VSS2 = 0 V)

| Parameter                  | Symbol         | Min.         | Typ. | Max.       | Unit   |
|----------------------------|----------------|--------------|------|------------|--------|
| Logic supply voltage       | VDD1           | 2.7          | 3.0  | 3.6        | V      |
| Driver supply voltage      | VDD2           | 5.0          | 7.0  | 8.0        | V      |
| Gamma corrected voltage    | VGMA1 - VGMA5  | 0.5 VDD2     | -    | VDD2 - 0.1 | V      |
|                            | VGMA6 - VGMA10 | VSS2 + 0.1   | -    | 0.5 VDD2   | V      |
| Driver part output voltage | Vyo            | VSS2 + 0.1   | -    | VDD2 - 0.1 | V      |
| Maximum clock frequency    | fmax           | VDD1 = 2.7 V |      | 45         | MHz    |
| Output load capacitance    | CL             | -            | -    | 150        | pF/PIN |

## DC CHARACTERISTICS

**Table 5. DC Characteristics (Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 5.0 to 8.0 V, VSS1 = VSS2 = 0 V)**

| Parameter                         | Symbol               | Condition                                                                                                                     | Min.             | Typ. | Max.             | Unit |
|-----------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------|------------------|------|------------------|------|
| High level input voltage          | VIH                  | SHL, CLK2, D00 - D55,<br>CLK1, POL, DATPOL1,<br>DATPOL2, DIO1 (DIO2)                                                          | 0.7VDD1          | -    | VDD1             | V    |
| Low level input voltage           | VIL                  |                                                                                                                               | 0                | -    | 0.3VDD1          |      |
| Input leakage current             | IL                   |                                                                                                                               | -1               | -    | 1                | μA   |
| Input Capacitance                 | Cin                  |                                                                                                                               | -                | 5    | 10               | pF   |
| High level output voltage         | VOH                  | DIO1 (DIO2), IO = -1.0 mA                                                                                                     | VDD1-0.5         | -    | -                | V    |
| Low level output voltage          | VOL                  | DIO1 (DIO2), IO = +1.0 mA                                                                                                     | -                | -    | 0.5              |      |
| Resistor                          | R0 - R62             | Refer to Table 1. Resistor Strings                                                                                            | $R_n \times 0.7$ | -    | $R_n \times 1.3$ | Ω    |
| Driver output current             | IVOH1                | VDD2 = 8.0 V,<br>Vx = 2.5 V, Vyo = 7.5 V <sup>(1)</sup>                                                                       | -                | -1.0 | -0.5             | mA   |
|                                   | IVOL1                | VDD2 = 8.0 V,<br>Vx = 5.5 V, Vyo = 0.5 V <sup>(1)</sup>                                                                       | 0.5              | 1.0  | -                | mA   |
| Line-repair Driver output current | IVOH2                | VDD2 = 8.0 V,<br>Vx = 2.5 V, Vyo = 7.5 V <sup>(1)</sup>                                                                       | -                | -3.0 | -1.5             | mA   |
|                                   | IVOL2                | VDD2 = 8.0 V,<br>Vx = 5.5 V, Vyo = 0.5 V <sup>(1)</sup>                                                                       | 1.5              | 3.0  | -                | mA   |
| Output voltage deviation          | ΔVO                  | Input data : 00H to 3FH                                                                                                       | -                | ±10  | ±20              | mV   |
| Output RMS voltage deviation      | dVrms <sup>(2)</sup> | Input data : 00H to 3FH                                                                                                       | -                | ±5   | ±15              |      |
| Output voltage range              | Vyo                  | Input data : 00H to 3FH                                                                                                       | VSS2 + 0.1       | -    | VDD2 - 0.1       | V    |
| Logic part dynamic current        | IDD1                 | VDD1 = 3.0 V <sup>(3)</sup>                                                                                                   | -                | 4.0  | 5.5              | mA   |
| Driver part dynamic current       | IDD2                 | VDD1 = 3.0 V,<br>VDD2 = 8.0 V,<br>VGMA1 = 7.5 V,<br>VGMA5 = 4.5 V,<br>VGMA6 = 3.5 V,<br>VGMA10 = 0.5 V <sup>(3) (4) (5)</sup> | -                | 4.0  | 7.0              |      |

### NOTES:

1. Vyo is the output voltage of analog output pins Y1 to Y420. Vx is the voltage applied to analog output pins Y1 to Y420.
2. dVrms is a maximum deviation value from ideal difference between high output and low output at the same gray scale.
3. CLK1 period is defined to be 15 μs at fCLK2 = 30.5 MHz, data pattern = 101010 (checkerboard pattern), Ta = 25 °C
4. The current consumption per driver when SXGA+ single-sided mounting (10 drivers) is connected in cascade
5. No load

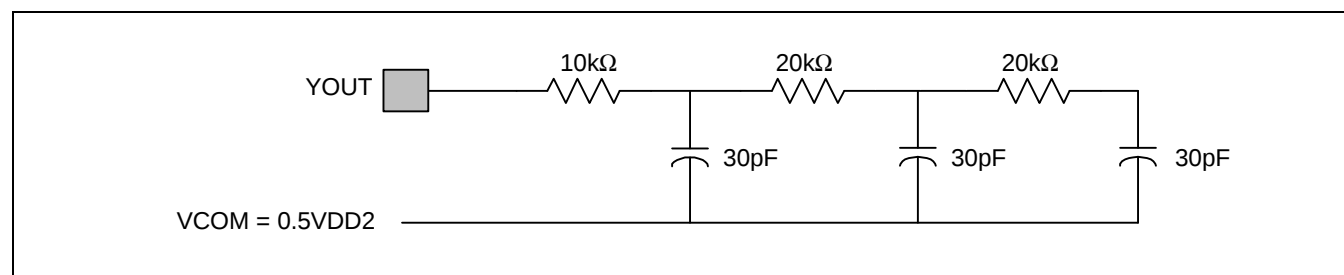
## AC CHARACTERISTICS

**Table 6. AC Characteristics** ( $T_a = -20$  to  $75\text{ }^{\circ}\text{C}$ ,  $V_{DD1} = 2.7$  to  $3.6\text{ V}$ ,  $V_{DD2} = 5.0$  to  $8.0\text{ V}$ ,  $V_{SS1} = V_{SS2} = 0\text{ V}$ )

| Parameter                 | Symbol                   | Condition                                                  | Min. | Typ. | Max. | Unit          |
|---------------------------|--------------------------|------------------------------------------------------------|------|------|------|---------------|
| Clock pulse width         | PWCLK                    | -                                                          | 22   | -    | -    | ns            |
| Clock pulse low period    | PWCLK(L)                 | -                                                          | 6    | -    | -    |               |
| Clock pulse high period   | PWCLK(H)                 | -                                                          | 6    | -    | -    |               |
| Data setup time           | t <sub>SETUP1</sub>      | Refer to NOTE1                                             | 2    | -    | -    |               |
| Data hold time            | t <sub>HOLD1</sub>       | Refer to NOTE1                                             | 2    | -    | -    |               |
| Start pulse setup time    | t <sub>SETUP2</sub>      | Refer to NOTE1                                             | 2    | -    | -    |               |
| Start pulse hold time     | t <sub>HOLD2</sub>       | Refer to NOTE1                                             | 2    | -    | -    |               |
| DATPOL-CLK2 setup time    | t <sub>SETUP4</sub>      | Refer to NOTE1                                             | 2    | -    | -    |               |
| DATPOL-CLK2 hold time     | t <sub>HOLD4</sub>       | Refer to NOTE1                                             | 2    | -    | -    |               |
| Start pulse delay time    | t <sub>PLH1</sub>        | CL = 20pF                                                  | -    | -    | 12   |               |
| CLK1 setup time           | t <sub>SETUP3</sub>      | -                                                          | 1    | -    | -    | CLK2 period   |
| Driver output delay time1 | t <sub>PHL1</sub>        | Refer to NOTE2, 4                                          | -    | -    | 4    | $\mu\text{s}$ |
| Driver output delay time2 | t <sub>PHL2</sub>        | Refer to NOTE3, 4                                          | -    | -    | 8    |               |
| CLK1 pulse high period    | PWCLK1                   | -                                                          | 0.2  | -    | -    |               |
| Data invalid period       | t <sub>INV</sub>         | DIO1 (2) $\uparrow \rightarrow$ CLK2 $\uparrow$            | 1    |      |      | CLK2 period   |
| Last data timing          | t <sub>LDT</sub>         | -                                                          | 1    | -    | -    |               |
| CLK1-CLK2 time            | t <sub>CLK1 - CLK2</sub> | CLK1 $\uparrow \rightarrow$ CLK2 $\uparrow$                | 8    | -    | -    | ns            |
| POL-CLK1 time             | t <sub>POL - CLK1</sub>  | POL $\uparrow$ or $\downarrow \rightarrow$ CLK1 $\uparrow$ | 6    | -    | -    | ns            |

### NOTES:

1. Input condition ( $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ )
2. The value is specified when the drive voltage value reaches the target output voltage level of 90%
3. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
4. Yout Load Condition



**Figure 5. Yout Load Condition**

# WAVEFORMS (VIH = 0.7 VDD1, VIL = 0.3 VDD1)

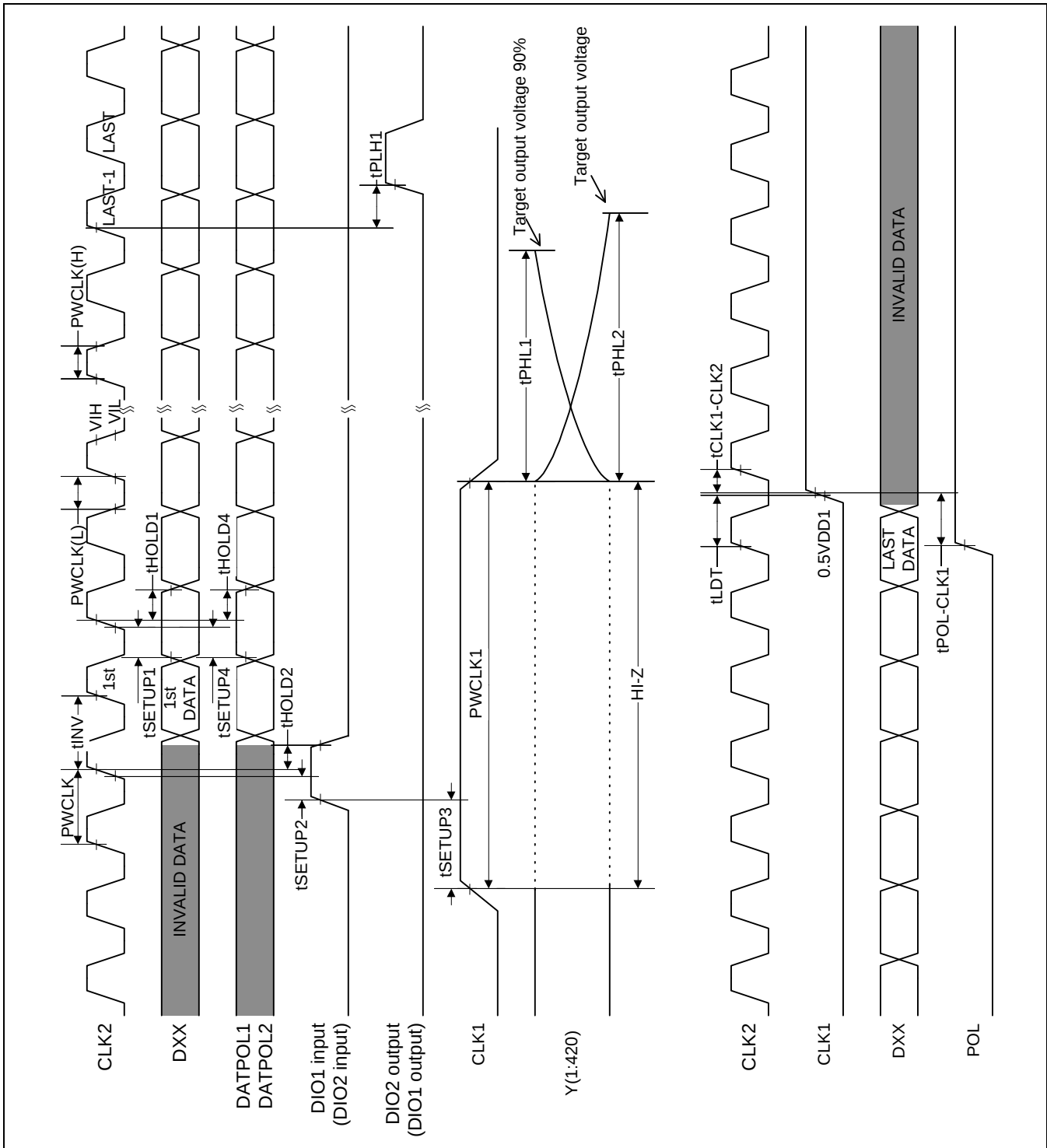
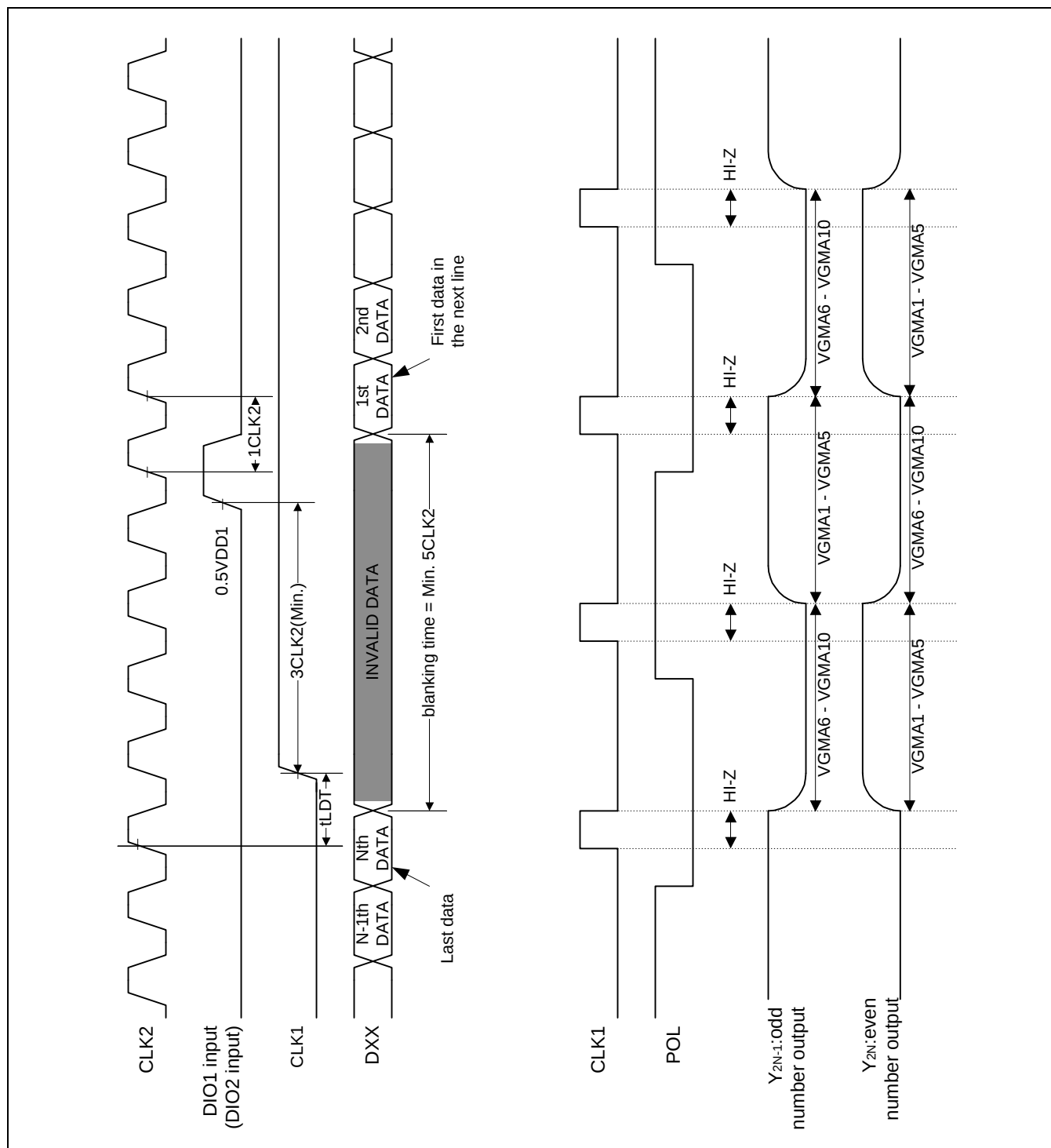


Figure 6. Waveforms

## RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD



### Figure 7. Waveforms