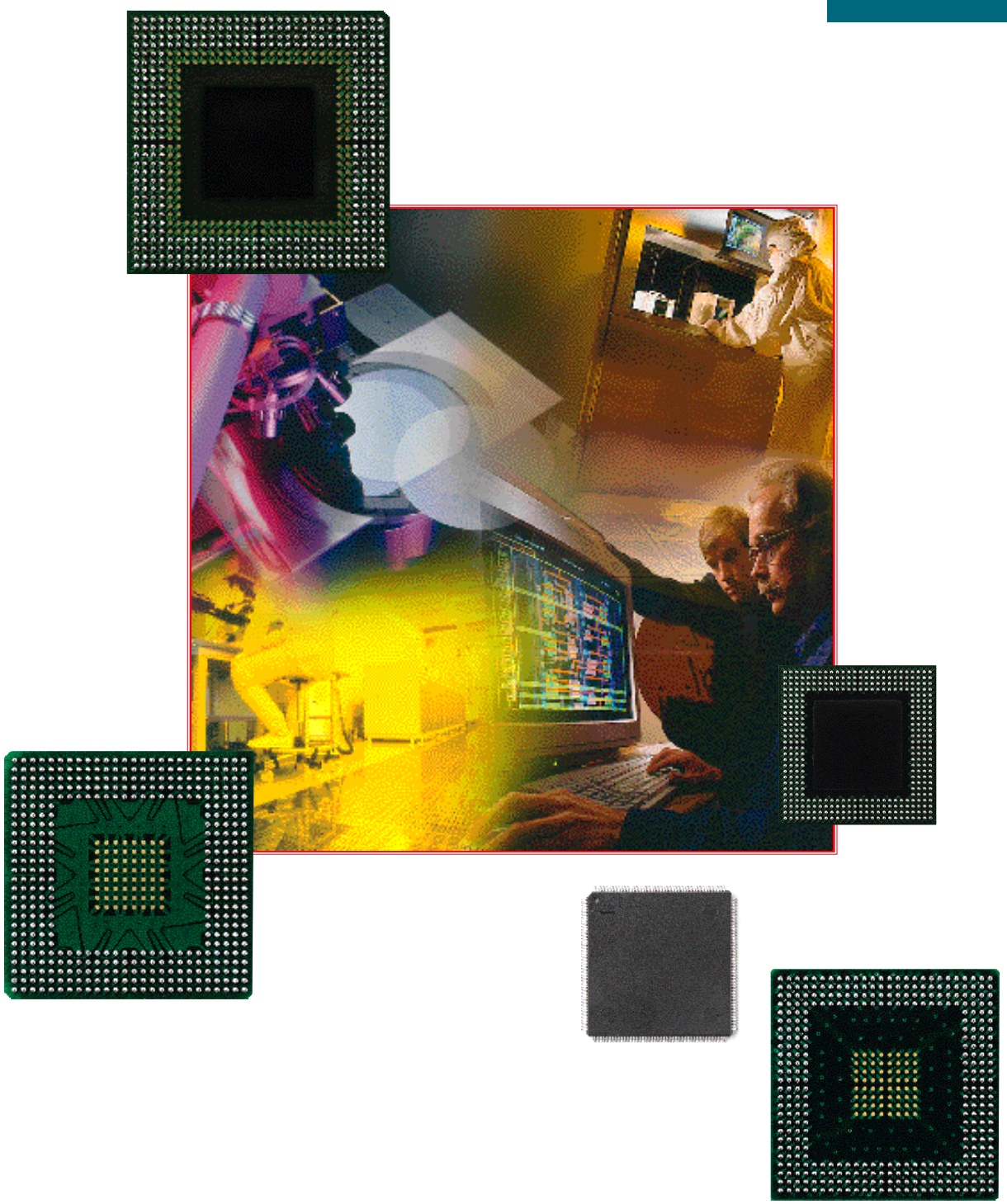
HIGH-DENSITY

KZ250GH
KZ250EH

CMOS GATE ARRAYS



KAWASAKI LSI

Overview

With the KZ250GH/KZ250EH CMOS Series, Kawasaki LSI offers a flexible 0.65micron generation of gate arrays and embedded arrays. These devices provide optimal solutions to meet your cost and performance needs for single 5V or 3.3V solutions, or 5V/3V mixed voltage solutions combined with quick turnaround. The technology is ideal for medium complexity, high-volume applications in the computing and communications markets that require up to a 100MHz system clock at 5V and 60MHz at 3.3V.

To achieve integration densities up to 500K gates, these gate arrays use Kawasaki LSI's DLM (Double Layer Metal) or TLM (Triple Layer Metal) CMOS process technology with a 0.43µm N-channel effective length. Using Kawasaki LSI's tight metal grid size and unique cell architecture, you can now achieve very high density, high performance, and very low power dissipation–comparable to standard-cell products. This Series also makes available I/O buffers that support PCI, USB and PECL standards.

The KZ250GH/KZ250EH Series offers a wide selection of compileable memories, so you can optimize your design by choosing the best solution to satisfy your requirements. For high-performance, design convenience and fast time to market, the Series offers value-added analog functions (PLL, A/D Converter, D/A Converter, etc.), CPU (and its peripheral) cores, JPEG core and CAM (Content Addressable Memory) core. You can also maximize chip-level and system-level performance for complex chips using the Kawasaki LSI design methodology, which includes a large library of accurately characterized cells; synthesis that can optimize for speed, power or area; clock distribution schemes; test insertion; and physical layouts driven from a floor planner on industry-standard tools.

Quality and Reliability

Kawasaki LSI is committed to supplying high-quality products with reliability levels meeting or exceeding semiconductor industry standards. Quality is designed in from the earliest stages of product development and is an integral part of engineering and manufacturing in volume production. The benefit of this focus to the customer is that Kawasaki LSI delivers modeling libraries on multiple tools that provide excellent correlation to the actual silicon performance and result in designs that physically work according to the simulations. Also, rigid qualification tests are performed on each product introduced to ensure that exacting industry standards of reliability are met.

In production, Kawasaki LSI continually strives to improve quality, lower costs and speed delivery–by process automation, operator education, and Statistical Process Control.

Kawasaki LSI has been ISO9001 qualified on semiconductor manufacturing and design since 1994.

Key Features

- Fastest time-to-market with 18 High-Density Gate Array Masterslices
- Supports system clocks up to 100MHz
- Cost-effective solution for 5V designs up to 500K gates
- Embedded Arrays offered for complex designs with large memories
- Customized array options available for high-volume applications
- Universal PCI buffers available; and support for USB buffers
- High I/O drive up to 16mA, including slew-rate-controlled buffers
- Accurately characterized macrocell library for effective logic synthesis
- Look-up table timing supported on industry-standard platforms
- Clock skew management; PLL and clock distribution methodologies
- Testability tools such as SCAN TEST, IDDQ, and JTAG
- Six types of metal-programmable SRAM compilers
- High-density all-layer memory compilers; up to 7.25K bits/mm^2 for RAM
- Plastic flat pack (QFP), Ball Grid Array (BGA) and Pin Grid Array (PGA) packages available
- Power dissipation of 1.5 µW/MHz/gate@3.3V (average gate, standard condition)

Core Library

The KZ250GH/KZ250EH Series library offers more than 300 robust macrocells, providing a variety of high-performance synthesizing options. The macrocells are composed of different sized transistors, enabling you to optimize for speed, power and density. The macrocells have input slew-rate-dependent loading and offset delay, and non-linear output load-dependent delay parameters to produce accurate characterized timings, resulting in the maximum performance achievable from the process technology. The core library is supplied for many industry-standard tools, including Verilog HDL, VHDL, Synopsys, Mentor, ViewLogic and others.

I/O LIBRARY

The I/Os in this Series are powered at 5V or 3.3V supply. Options such as slew-rate-controlled CMOS and TTL output buffers driving up to 16mA, open-drain outputs, inputs with pull-up and pull-down resistors, Schmitt triggers, and combinations of bi-directional buffers are available.

The KZ250GH/KZ250EH Series also supports low-voltage swing I/Os. Kawasaki LSI's PCI bus I/O buffer is an optimal solution for interfacing to industry-standard PCI buses. A Universal PCI Buffer is available for end-user choice of 5V or 3.3V system voltage. Standards such as Pseudo-ECL (PECL) and Universal Serial Bus (USB) are also supported.

MEMORIES

Metal-Programmable Memory

The KZ250GH/KZ250EH Series has two types of metal-programmable memory compilers: High-Density (HD) RAM compiler and Low-Power (LP) RAM compiler. HD RAMs feature very high performance, including more than 100MHz operation, offering high density up to 3.5K bits/mm^2. HD RAMs are suitable for applications that need high-performance, high-density memories. The total capacity of an HD RAM is up to 36K bits per block and is available in Synchronous and Asynchronous options.

LP RAMs feature high performance and very low power. The total capacity of an LP RAM is limited to 16K bits. LP RAMs are suitable, for example, to the needs of register files. Table 1 shows the performance and specifications of HD and LP RAMs.

Table 1 KZ250GH Metal-Programmable Memories

		Total Bits	Word	Bit	Density	Access Time
High-Density	1-p Async.	64~36K	64~4K	1~36	~3,440 bits/mm^2	4.6ns*
	1-p Sync.	64~36K	64~4K	1~36	~3,320 bits/mm^2	5.2ns*
	2-p Async.	64~36K	32~4K	1~36	~1,670 bits/mm^2	5.5ns*
	2-p Sync.	64~36K	32~4K	1~36	~1,670 bits/mm^2	5.8ns*
Low-Power	1-p Async.	1~16K	1~128	1~128	~1,630 bits/mm^2	4.0ns**
	2-p Async.	1~16K	1~128	1~128	~1,630 bits/mm^2	3.8ns**

*Access time is for 512-word x 8-bit configuration in typical condition.
**Access time is for 32-word x 8-bit configuration in typical condition.

All-Layer Memory

In the KZ250EH Series, higher density embedded memories are provided by all-layer memory compilers. All-layer memories feature extremely high density, large capacity, and high performance, while offering low power dissipation. The largest compileable RAM is 72K bits, and 256K bits for ROM. The bit density of 7.25K bits/mm^2 for the single-port RAM is high for ASIC memories in comparable technologies.

These Kawasaki LSI all-layer memories are tuned for high-performance, memory-intensive applications such as graphics, image processing, ATM switches, compute system logic, and networking.

ASIC DRAM is offered as one of the all-layer memories; the density of 14K bits/mm^2 is two times higher than that of the all-layer single-port RAM. A 50MHz (worst-case condition) high-speed page mode operation is achievable. Table 2 shows the performance specifications of all-layer memories.

Table 2 KZ250EH All-Layer Memories

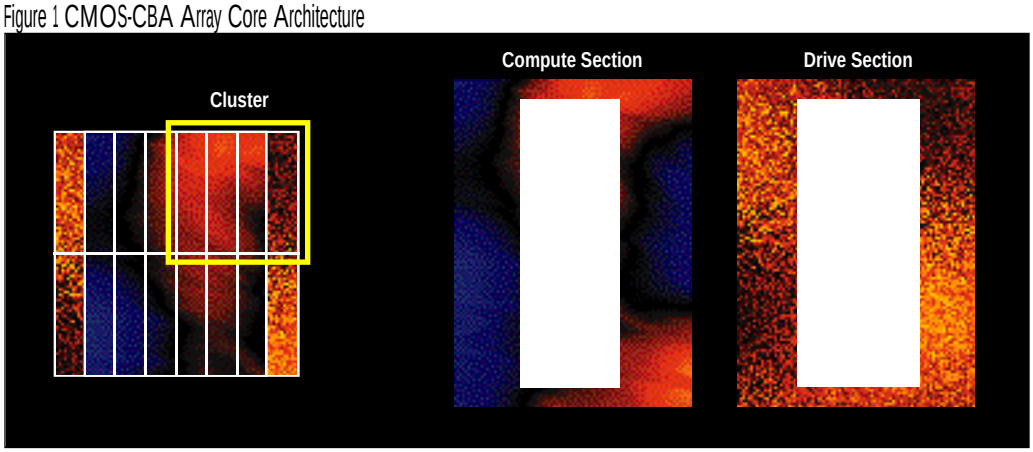
		Total Bits	Word	Bit	Density	Access Time
SRAM	1-p Sync.	16~72K	16~8K	1~36	~7,250 bits/mm^2	5.3ns*
	1-p Async.	32~72K	32~8K	1~36	~7,140 bits/mm^2	7.2ns*
	2-p Sync.	16~72K	16~8K	1~36	~4,260 bits/mm^2	5.4ns*
ROM	1-p Sync.	16~256K	16~64K	1~128	~25,600 bits/mm^2	5.4ns*
DRAM	1-p Sync.	256K	8K	16 x 2 bank	14,200 bits/mm^2	55/15ns**

*The numbers are for 512-word x 8-bit configuration in typical condition.
**The numbers are row access time/column access time under worst case conditions.

Array Architecture

The core cell of the KZ250GH/KZ250EH Series, shown in Figure 1, is based on the CMOS-CBA® architecture licensed by Synopsys, Inc. It consists of two different unit cells, named compute cell and drive cell. A compute cell contains four small PMOS and four small NMOS transistors that are optimized for building logic and memory. A drive cell contains two large PMOS and two large NMOS transistors that provide sufficient drive for global nets or large fanout. Macrocells are built mixing these two unit cells. Three compute cells and one drive cell in a cluster have been determined by statistical analysis to provide an optimal density capability for many design styles. Four clusters are indicated in Fig. 1. Since a compute cell has low input capacitance and consumes less power, the performance of the KZ250GH/KZ250EH Series is very similar to that achieved with standard cell technologies. With this optimized cell architecture, KZ250GH/KZ250EH arrays achieve a gate density of up to 3,000 usable gates/mm^2.

Figure 1 CMOS-CBA Array Core Architecture



Array Family

Table 3 shows the 18 base arrays in the KZ250GH/KZ250EH Series. Array utilization depends on design, and typically varies from 28 to 40% in DLM (Double Layer Metal) technology, and from 45 to 60% in TLM (Triple Layer Metal) technology. A compute cell or a drive cell is counted as a gate. This unique cell architecture results in a higher integration density compared to conventional gate-array technology composed of four transistor cells. Kawasaki LSI offers an option to compile and fabricate a custom sized array for a specific high-volume design.

Table 3 KZ250GH Masterslice Selection

Array Index	Pad Count (by Pad Pitch)			Raw Gates	Usable Gates	
	Very Fine	Fine	Standard		DLM	TLM
003	112	112	108	28,900	11,600	17,300
004	136	136	128	42,400	17,000	25,500
006	160	160	152	61,500	24,600	36,900
007	180	176	168	74,000	29,600	44,400
009	196	192	184	92,400	36,100	54,100
012	232	228	216	123,900	46,600	69,800
015	252	244	232	147,400	54,100	81,100
017	268	260	248	169,700	61,000	91,500
019	284	276	264	193,600	68,200	102,400
022	304	296	280	219,000	75,700	113,600
024	316	308	292	240,100	81,800	122,700
027	336	324	308	268,300	89,800	134,700
030	352	340	324	298,100	98,000	147,000
038	408	392	372	381,900	120,100	180,200
042	428	412	388	419,800	129,700	194,600
051	460	444	420	512,600	152,400	230,700
069	536	512	488	685,500	191,900	308,500
099	640	616	584	988,000	276,600	444,600

Typical design both for DLM and TLM
A compute cell or a drive cell is counted as a gate.

MEGAFUNCTIONS AND ANALOG FUNCTIONS

Kawasaki LSI does offer a number of Megafunctions other than the compiled memories, which can be supported in the KZ250GH/KZ250EH Series to minimize design time and maximize performance of complex system chips. The KC80 is a very high-performance CPU core that is binary-compatible with the Zilog Z80. A JPEG core is also available for imaging and data compression applications. Kawasaki LSI also offers an Address Processor Core or Content Addressable Memory (CAM) for high-performance broadband network and internetworking applications.

There are a number of analog functions that are under development for video signal processing applications, system clock management and frequency synthesis. These functions include 8-bit A/D converters, 8-bit D/A converters, operational amplifiers, comparators, Phase Locked Loops (PLL) and Voltage Controlled Oscillators (VCO).

PHASE LOCKED LOOP (PLL)

As system clock frequencies increase, clock skew must be minimized between different chips in a system to maximize system performance. Kawasaki LSI's KZ250GH/KZ250EH Series offers the PLL function, which synchronizes the ASIC's internal clock to the external system clock to minimize the skew between chips on a board. The frequency of the internal clock can be a multiple of the external clock. The specification and range of the PLL in KZ250GH/KZ250EH technology is indicated in Table 4.

Table 4 KZ250GH/KZ250EH PLL Specifications

CHARACTERISTICS	SPECIFICATIONS
Operating Frequency	15MHz~148MHz
Maximum Input Phase Tolerance	± 50ppm
Maximum Jitter	-100ps~100ps
Maximum Phase Error	-400ps~400ps
Duty Cycle	45%~55%

CLOCK DISTRIBUTION

It is important to minimize not only chip-to-chip level system clock skew, but also chip-level clock skew on a die for maximum system performance. Kawasaki LSI provides several clocking methodologies to minimize on-chip clock skew. You can choose from various implementations, and also combine them to satisfy your design requirements. The specifications for each clock distribution scheme are indicated in Table 5.

Clock Buffer

This method is most popular and has been well utilized in older technologies. It is simple and effective in cases where the number of clocked elements are less than a few hundred, or the clock skew requirement is not severe. In the KZ250GH/KZ250EH Series, up to 200 flip-flops (depends on frequency) can be driven in a single stage with special buffers for clocking.

Clock Tree Synthesis (CTS)

Clock Tree Synthesis is an automatic way to build a clock tree by balancing the far end delay with local buffers at the most appropriate physical location. The clock tree is synthesized with low driving inverters or buffers. CTS is efficient when the number of clocked instances is very large or the clock skew requirement is tight.

Clock Trunk with CTS

The clock trunk is a wide metal line which is connected to a special clock driver. It provides lower skew and a shorter delay than a clock buffer or CTS. In the KZ250GH/KZ250EH Series, a strong clock driver can be built with multiple special buffers for clocking, or can be configured with an I/O clock driver, which typically uses 2 to 3 I/O pads.

Table 5 Recommended Maximum Loading and Specifications for Clock Distribution Methodology

	NUMBEROF CLOCKED INSTANCES	TARGETED CLOCK SKEW	TARGETED CLOCK INSERTION DELAY
CLOCK BUFFER	≤200	≤500ps~1,000ps	≤2~3ns (typical)
CLOCK TREE SYNTHESIS (CTS)	≤3,000	≤300ps~500ps	≤2~4ns (typical)
CLOCK TRUNKWITH CTS	≤5,000	≤300ps~500ps	≤1~2ns (typical)

Packages

Kawasaki LSI supports an extensive family of packaging solutions to meet your applications requirements. The extent of the packaging solutions, for thru-hole and surface mount, from low pin-count DIP to very high pin-count BGA, are shown in Table 6.

Kawasaki LSI's specific die/package matrix of devices in production is constantly being updated. Please contact your Kawasaki LSI sales office and Applications Engineering for specific information regarding your requirement.

Table 6 KZ250GH/KZ250EH Package Offerings

Package	Pin Count										
SDIP	42	64									
PQFP	44	64	80	100	120*	144*	160*	176*	208*	240*	304*
TQFP (1.4 mm thick body)	64	80	100	144							
PBGA	256	304	352	420	480	576					
TBGA	256	304	352	420	480	576	672				
PGA	144	180	208	256	280						

*Drop-in heat spreader available for high power dissipation

Test Methodology

To ensure a high-quality device, it is important to implement testing with high fault coverage. Kawasaki LSI's test methodology for the KZ250GH/KZ250EH Series includes the following test solutions.

Internal Full Scan Testing

Internal Full Scan Testing is one of the most powerful test methodologies for automatically developing test vectors, achieving more than 95% stuck-at fault coverage for large synchronous designs. This methodology is supported using Synopsys' Test Compiler, which automatically performs testability rule checking, scan chain insertion and ATPG (Automatic Test Pattern Generation).

IDDQ Testing

IDDQ Testing is an effective methodology which detects various types of silicon defects without area or performance overhead. This methodology is supported by measuring the device's quiescent power-supply current on functional vectors selected by CM-iTest from CrossCheck, Inc. This test provides an easy way to improve the fault coverage of an ad-hoc test strategy.

JTAG (IEEE 1149.1 Boundary Scan Testing)

JTAG is supported by inserting the boundary scan circuits into the system logic and providing test vectors and BSDL for the boundary scan logic. The TAP controller and associated logic is transparently inserted into the customer's netlist.

Process Monitoring

Process monitoring is performed by adding an AC measurement circuit into the device and measuring the AC delay. This AC measurement verifies that the device can operate at a required frequency.

Fault Simulation

Fault simulation is supported using the Cadence Verifault-XL simulator, which allows you to rapidly obtain fault coverage information for the applied test vectors.

Table 7 Kawasaki LSI's Test Solutions

Capability	LSI Availability Status	Customer Development Time	LSI Service Development Time	ATPG Availability	Target Fault Coverage	Performance Penalty	Silicon Overhead
Internal Scan	Now	<1 week	<1 week	Now	>95%	5-15%	5-12%
IDDQ	Now	Design Development	1-4 weeks	In Development	>90% Low Speed	None	None
JTAG	Now	<1 day	<1 day	Now	>95%	0.4-1.0ns	400 + BSR* Gates
Process Monitoring	Now	<1 day	2-3 days	Not Required	N/A	None	<200 Gates
Fault Simulation	Now	Design Development	Design Development	Not Required	>95%	None	None

*BSR = 21 x input pin + 21 x output pin (2state) + 42 x output pin (3state) + 46 x bi-directional pin

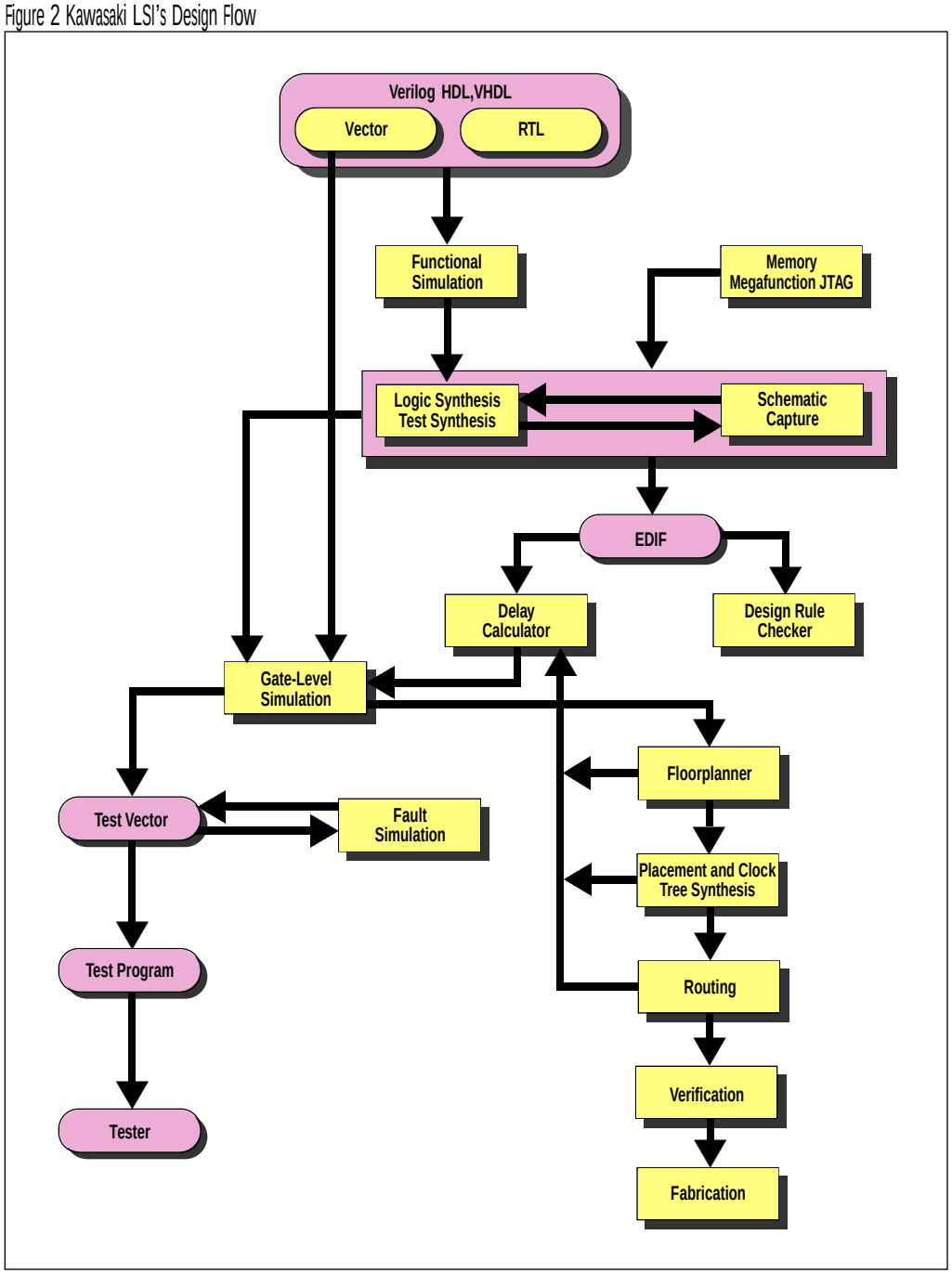
DESIGN SYSTEM

Kawasaki LSI's integrated top-down design flow is shown in Fig. 2. It allows you to start either with VHDL or Verilog-HDL, or from the gate level, and choose from a wide assortment of schematic capture programs within Kawasaki LSI's design environment. Kawasaki LSI supports popular EDA tools, from companies such as Synopsys, Cadence, Mentor Graphics and ViewLogic.

Kawasaki LSI's Design Rule Checker and Delay Calculator can read EDIF netlists. Thus you have a choice of either VSS with an FTGS library, Verilog, QuickSim II, ViewSim, or another VHDL simulator with VITAL libraries, to read the delay files generated by the Delay Calculator for gate-level simulation. An accurate delay calculation method is provided, accounting for not only output-load-dependent delay, but also input-slew-rate-dependent offset delay, input-slew-rate-dependent loading delay and interconnect delay due to the wire RC. This advanced calculation methodology, coupled with control of the physical layout, results in implementation of the highest performance designs in 0.5micron technology.

The interfaces to these tools are industry-standard formats such as VHDL, EDIF, SDF, PDEF and WGL, making it very easy for designers to migrate their designs to Kawasaki LSI's technologies. The design sign-off golden simulator is Verilog, and verification is done using Dracula tools.

Figure 2 Kawasaki LSI's Design Flow



ELECTRICAL CHARACTERISTICS

Tables 8 through 10 show the electrical characteristics of the KZ250GH/KZ250EH Series.

Table 8 Recommended Operating Conditions

PARAMETER	SYMBOL	RATING	UNITS
Power Supply Voltage	VDD	4.75~5.25	V
		4.5~5.5	V
		3.0~3.6	V
Ambient Temperature	Ta	-40~+85	°C

Table 9 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNITS
Power Supply Voltage	VDD	-0.6~+7.0	V
Input Voltage	VIN	-0.6~VDD+0.6	V
Output Current	IOUT	40	mA
Storage Temperature	TSTG	-55~+125	°C

Table 10 DC Electrical Characteristics (VDD=5.0V±0.5V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Vih	High-Input Voltage	TTL	2.0	–	–	V
		CMOS	3.5	–	–	V
Vil	Low-Input Voltage	TTL	–	–	0.8	V
		CMOS	–	–	1.5	V
V+	High-Input Voltage	TTL-Schmitt	–	1.66	2.15	V
		CMOS-Schmitt	–	3.2	4.0	V
V-	Low-Input Voltage	TTL-Schmitt	0.6	1.13	–	V
		CMOS-Schmitt	0.9	1.61	–	V
Vh	Hysteresis Voltage	TTL-Schmitt	0.3	–	–	V
		CMOS-Schmitt	0.9	–	–	V
Iih	High-Input Current	VIN=VDD	-10	–	+10	µA
Iil	Low-Input Current	VIN=VSS	-10	–	+10	µA
Voh	High-Output Voltage	Ioh=-2~-16mA	3.5	–	–	V
Vol	Low-Output Voltage	Iol=2~16mA	–	–	0.4	V
Ioz	3-State Leak Current	Voh=VSS	-10	–	+10	µA
		Vol=VDD	-10	–	+10	µA
Ipu	Active Pull-Up Current	VIN=VSS	-25	-95	-250	µA
Ipd	Active Pull-Down Current	VIN=VDD	25	95	250	µA
Idds	Static Stand-By Current	–	–	–	100*	µA

*The number is design-dependent.

Table 11 DC Electrical Characteristics (VDD=3.3V±0.3V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Vih	High-Input Voltage	TTL	1.65	–	–	V
		CMOS	2.15			V
Vil	Low-Input Voltage	TTL	–	–	0.65	V
		CMOS			0.95	V
V+	High-Input Voltage	TTL-Schmitt	–	1.32	1.75	V
		CMOS-Schmitt		2.17	2.65	V
V-	Low-Input Voltage	TTL-Schmitt	0.45	0.86	–	V
		CMOS-Schmitt	0.5	1.03	–	V
Vh	Hysteresis Voltage	TTL-Schmitt	0.25	–	–	V
		CMOS-Schmitt	0.56	–	–	V
Iih	High-Input Current	VIN=VDD	-10	–	+10	µA
Iil	Low-Input Current	VIN=VSS	-10	–	+10	µA
Voh	High-Output Voltage	Ioh=-2~-16mA	2.4	–	–	V
Vol	Low-Output Voltage	Iol=2~16mA	–	–	0.4	V
Ioz	3-State Leak Current	Voh=VSS	-10	–	+10	µA
		Vol=VDD	-10	–	+10	µA
Ipu	Active Pull-Up Current	VIN=VSS	-12	-34	-100	µA
Ipd	Active Pull-Down Current	VIN=VDD	12	34	100	µA
Idds	Static Stand-By Current	–	–	–	100*	µA

*The number is design-dependent.

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