KA7500B

SMPS Controller

Features

- Internal regulator provides a stable 5V reference supply trimmed to 5%
- Uncommitted output TR for 200mA sink or source current
- Output control for push-pull or single-ended operation
- Variable duty cycle by dead time control (pin 4) Complete PWM control circuit
- On-chip oscillator with master or slave operation
- Internal circuit prohibits double pulse at either output

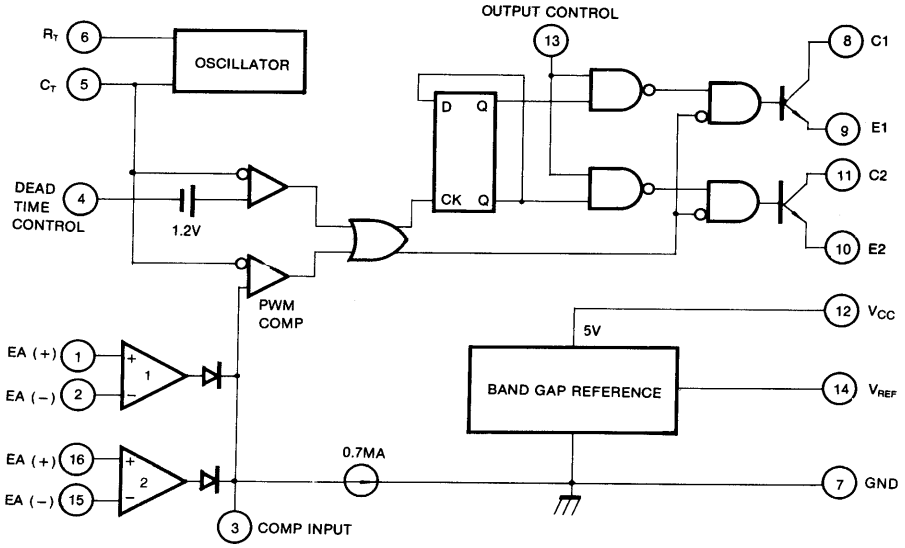
Description

The KA7500B is used for the control circuit of the PWM switching regulator. The KA7500B consists of 5V reference voltage circuit, two error amplifiers, flip flop, an output control circuit, a PWM comparator, a dead time comparator and an oscillator. This device can be operated in the switching frequency of 1 KHz to 300 KHz.

16-DIP

16-SOP

Internal Block Diagram



Rev. 5.0

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	42	V
Collector Supply Voltage	V_C	42	V
Output Current	I_O	250	mA
Amplifier Input Voltage	V_{IN}	V_{CC} + 0.3	V
Power Dissipation (T_A = 25°C)	P_D	1 (KA7500B) 0.9 (KA7500BD)	W
Operating Temperature Range	T_{OPR}	0 ~ +70	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	°C

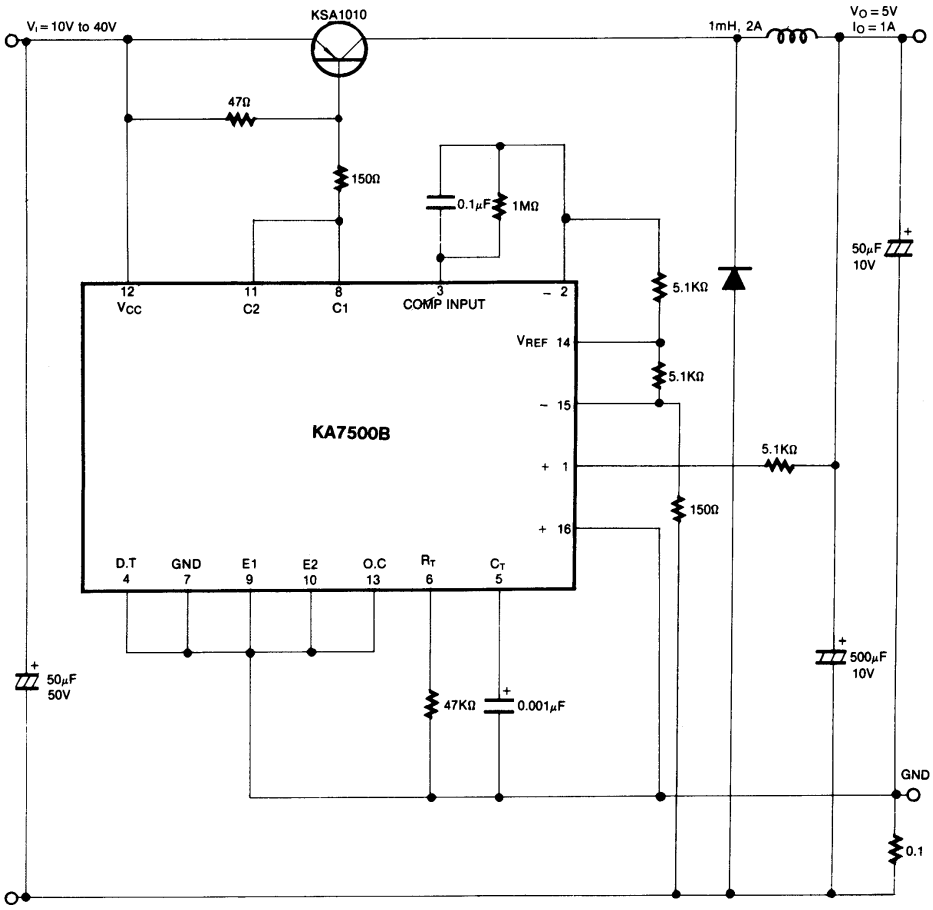
Electrical Characteristics

(V_{CC} = 20V, f = 10KHz, T_A = 0°C to + 70°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	I_{REF} = 1mA	4.75	5.0	5.25	V
Line Regulation	ΔV_{REF}	V_{CC} = 7V to 40V	-	2.0	25	mV
Temperature Coefficient of V_{REF}	$\Delta V_{REF}/\Delta T$	T_A = 0°C to 70°C	-	0.01	0.03	%/°C
Load Regulation	ΔV_{REF}	I_{REF} = 1mA to 10mA	-	1.0	15	mV
Short-Circuit Output Currnet	I_{SC}	V_{REF} = 0V	10	35	50	mA
OSCILLATOR SECTION						
Oscillation Frequency	f	C_T = 0.01μF, R_T = 12KΩ	-	10	-	KHz
Frequency Change with Temperature	$\Delta f/\Delta T$	C_T = 0.01μF, R_T = 12KΩ	-	-	2	%
DEAD TIME CONTROL SECTION						
Input Bias Current	I_{BIAS}	V_{CC} = 15V, 0V≤V_4≤5.25V	-	-2.0	-10	μA
Maximum Duty Cycle	$D_{(MAX)}$	V_{CC} = 15V, V_4 = 0V O.C Pin = V_{REF}	45	-	-	%
Input Threshold Voltage	V_{ITH}	Zero Duty Cycle	-	3.0	3.3	V
		Max. Duty Cycle	0	-	-	
ERROR AMP SECTION						
Input Offset Voltage	V_{IO}	V_3 = 2.5V	-	2.0	10	mV
Input Offset Current	I_{IO}	V_3 = 2.5V	-	25	250	mA
Input Bias Current	I_{BIAS}	V_3 = 2.5V	-	0.2	1.0	μA
Common Mode Input Voltage	V_{CM}	7V ≤ V_{CC} ≤ 40V	-0.3	-	V_{CC}	V
Open-Loop Voltage Gain	G_{VO}	0.5V ≤ V_3 ≤3 .5V	70	95	-	dB
Unit-Gain Bandwidth	BW	-	-	650	-	KHz
PWM COMPARATOR SECTION						
Input Threshold Voltage	V_{ITH}	Zero Duty Cycle	-	4	4.5	V
Input Sink Currnet	I_{SINK}	V_3=0.7V	-0.3	-0.7	-	mV
OUTPUT SECTION						
Output Saturation Voltage Common Emitter	$V_{CE(SAT)}$	V_E = 0, I_C = 200mA	-	1.1	1.3	V
Common Collector	$V_{CC(SAT)}$	V_C = 15V, I_E = -200mA	-	1.5	2.5	
Collector Off-State Currnet	$I_{C(OFF)}$	V_{CC} = 40V, V_{CE} = 40V	-	2	100	μA
Emitter Off-State Current	$I_{E(OFF)}$	V_{CC} = V_C = 40V, V_E = 0	-	-	-100	
TOTAL DEVICE						
Supply Current	I_{CC}	Pin 6 = V_{REF}, V_{CC} = 15V	-	6	10	mA
OUTPUT SWITCHING CHARACTERISTIC						
Rise Time	t_R	-	-	-	-	-
Common Emitter	-	-	-	100	200	ns
Common Collector	-	-	-	100	200	
Fall Time	t_F	-	-	-	-	-
Common Emitter	-	-	-	25	100	ns
Common Collector	-	-	-	40	100	

Typical Application

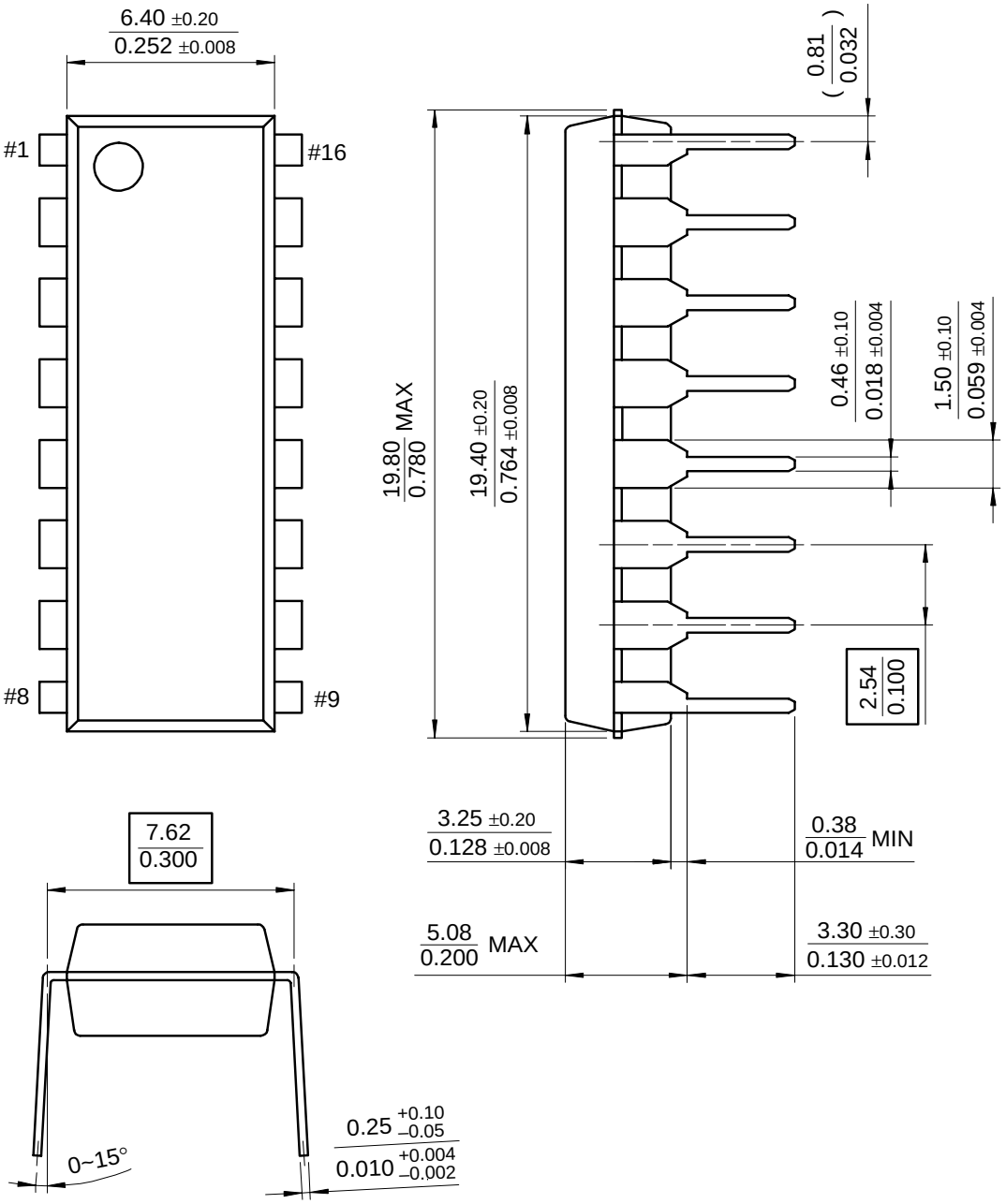
Pulse Width Modulated Step-down Converter



Mechanical Dimensions

Package

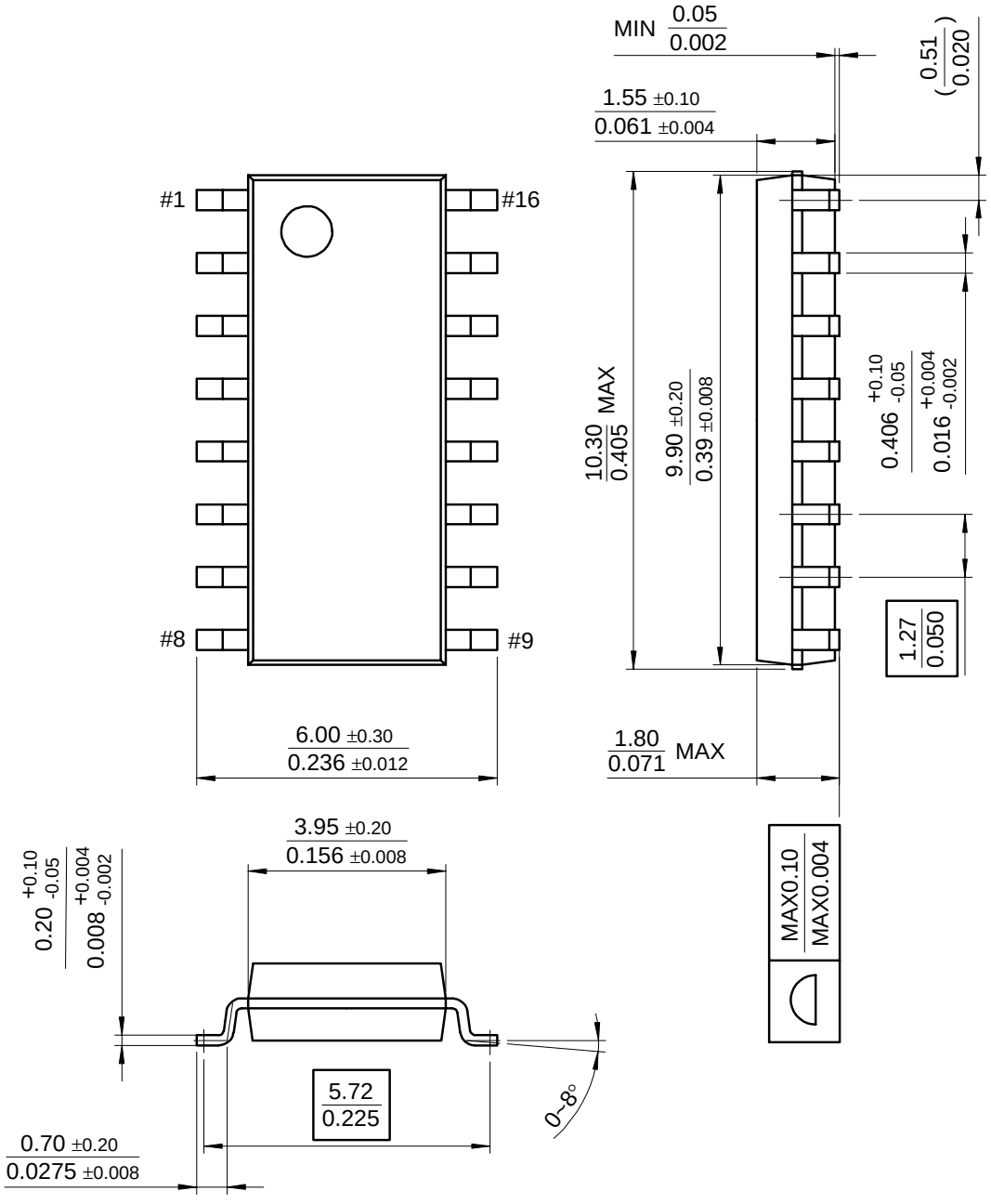
16-DIP



Mechanical Dimensions (Continued)

Package

16-SOP



Ordering Information

Product Number	Package	Operating Temperature
KA7500B	16 DIP	0 ~ + 70°C
KA7500BD	16 SOP	

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