Network-DRAM Specification
Version 0.2

Revision History

Version 0.0 (Oct. / 5 / 2001)

- First Release

Version 0.1 (Dec. / 15 / 2001)

- The product name is changed to Network-DRAM

Version 0.2 (Jan. / 21 / 2002)

- M-version is renamed to C-version
- Specify DC operating condition values
- Added Power Up Sequence and Power Down(CL=4) Timing Diagrams

<Notice>

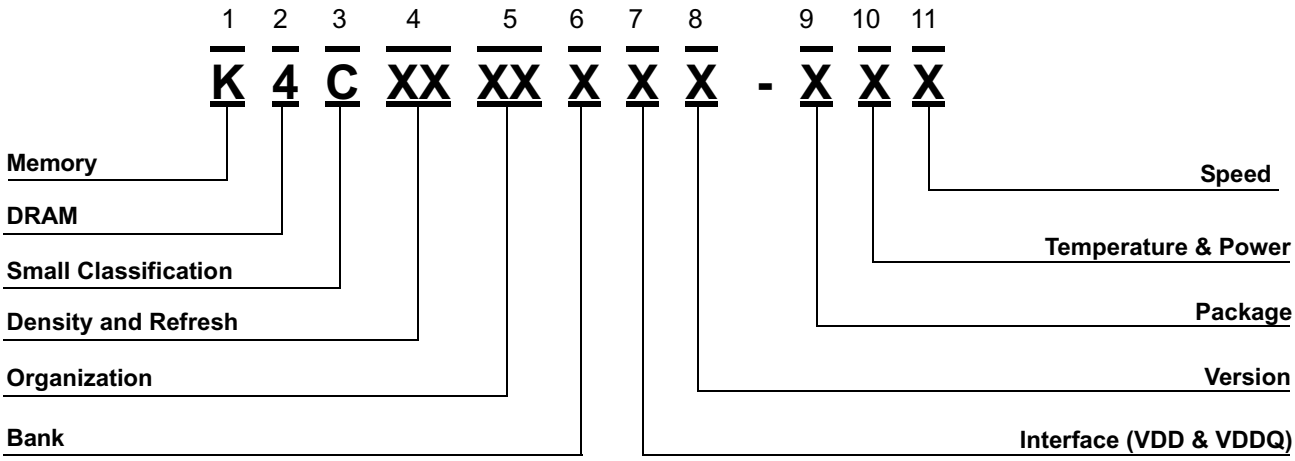
- Network-DRAM is a trademark of Samsung Electronics Co., LTD.

- Network-DRAM is fully compatible with FCRAM

Note : FCRAM is a Trademark of Fujitsu Limited, Japen

General Information

Organization	B (200MHz)	A (167MHz)
256Mx8	K4C560838C-TCB	K4C560838C-TCA
256Mx16	K4C561638C-TCB	K4C561638C-TCA



1. SAMSUNG Memory : K

2. DRAM : 4

3. Small Classification
C : Network-DRAM

4. Density & Refresh
56 : 256M 8K/64ms

5. Organization

08 : x8
16 : x16

6. Bank
3 : 4 Bank

7. Interface (VDD & VDDQ)
8: SSTL-2(2.5V, 2.5V)

8. Version
C : 4th Generation

9. Package
T : TSOP II (400mil x 875mil)

10. Temperature & Power
C : (Commercial, Normal)

11. Speed
A : 167MHz (334Mbps/pin, CL=4)
B : 200MHz (400Mbps/pin, CL=4)

Key Feature

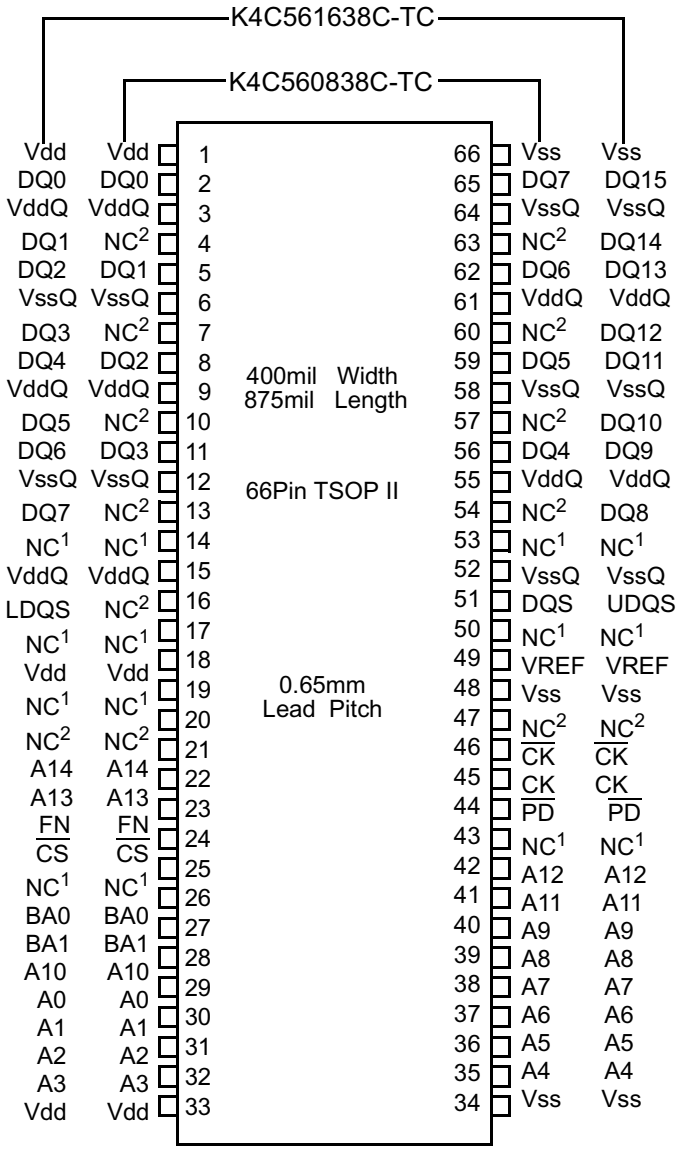
Item		K4C560838/1638C-TC	
		B (200MHz)	A (167MHz)
t_{CK} Clock Cycle Time (Min.)	CL=3	5.5ns	6.5ns
	CL=4	5ns	6ns
t_{RC} Random Read/Write Cycle Time (Min.)		25ns	30ns
t_{RAC} Random Access Time (Max.)		22ns	26ns
I_{DD1S} Operating Current (Single bank) (Max.)		324mA	317mA
I_{DD2P} Power Down Current (Max.)		2mA	2mA
I_{DD6} Self-Refresh Current(Max.)		3mA	3mA

- Fully Synchronous Operation
  - Double Data Rate (DDR)
    - Data input/output are synchronized with both edges of DQS.
  - Differential Clock (CK and $\overline{CK}$)inputs
    - $\overline{CS}$, FN and all address input signals are sampled on the positive edge of CK.
    - Output data (DQs and DQS) is referenced to the crossings of CK and $\overline{CK}$.
- Fast clock cycle time of 5ns minimum Clock : 200MHz maximum
  Data : 400Mbps/pin maximum
- Quad independent banks operation
- Fast cycle and short latency
- Bidirectional data strobe signal
- Distributed Auto-Refresh cycle in 7.8us
- Self-Refresh
- Power Down Mode
- Variable Write Length Control
- Write Latency = $\overline{CAS}$ Latency - 1
- Programmable $\overline{CAS}$ Latency and Burst Length
  $\overline{CAS}$ Latency = 3, 4
  Burst Length = 2, 4
- Organization K4C561638C-TC : 4,194,304 words x4 banks x 16
  K4C560838C-TC : 8,388,608 words x4 banks x 8
- Power supply voltage Vdd : 2.5 ± 0.15V
  VddQ : 2.5 ± 0.15V
- 2.5V CMOS I/O comply with SSTL-2 (Strong / Normal / Weaker / Weakest)
- Package 400X875mil, 66pin TSOP II, 0.65mm pin pitch (TSOP II 66-P-400-0.65)

Pin Names

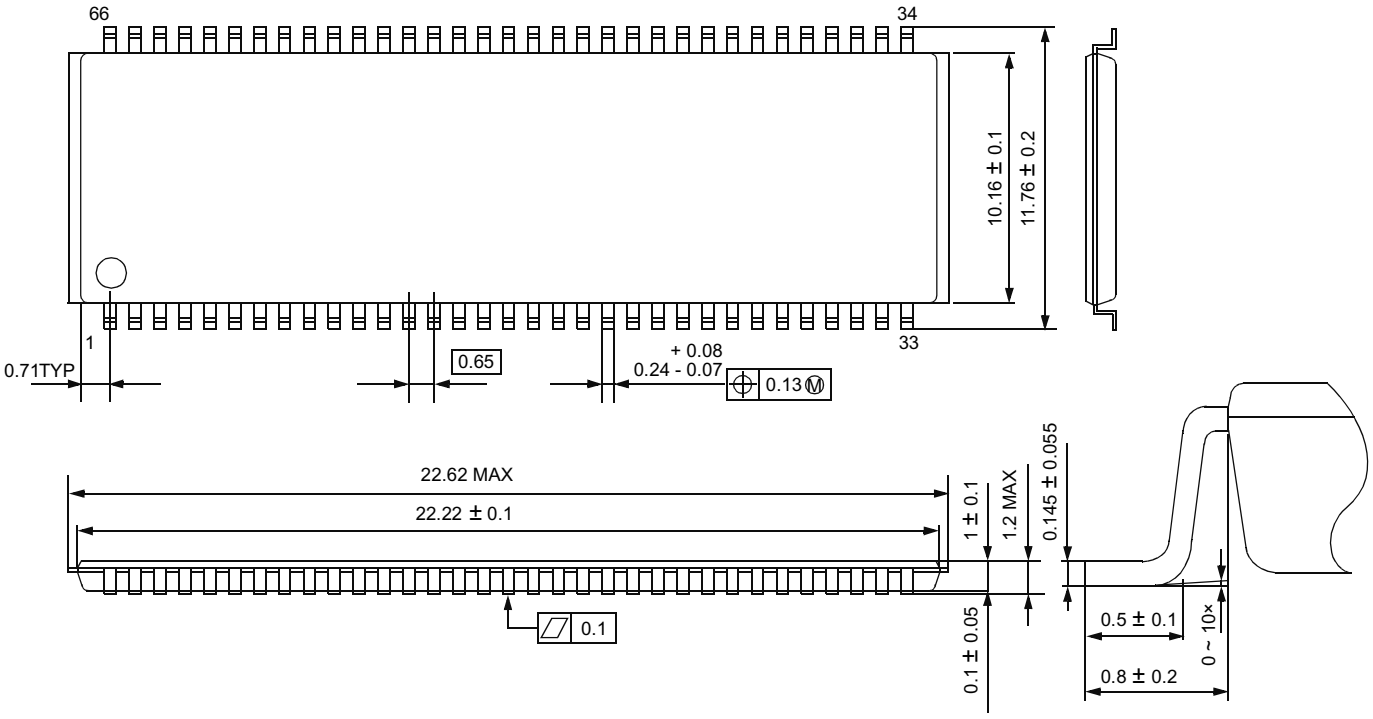
Pin	Name
A0 to A14	Address Input
BA0, BA1	Bank Address
DQ0 to DQ7 (x8)	Data Input/Output
DQ0 to DQ15 (x16)	
$\overline{CS}$	Chip Select
FN	Function Control
$\overline{PD}$	Power Down Control
CK, ($\overline{CK}$)	Clock Input
DQS (X8)	
UDQS/LDQS (X16)	Write/Read Data Strobe
Vdd	
Vss	Ground
VddQ	Power (+2.5V) (for I/O buffer)
VssQ	Ground (for I/O buffer)
V_{REF}	Reference Voltage
NC1,NC2	No Connection

Pin Assignment (Top View)

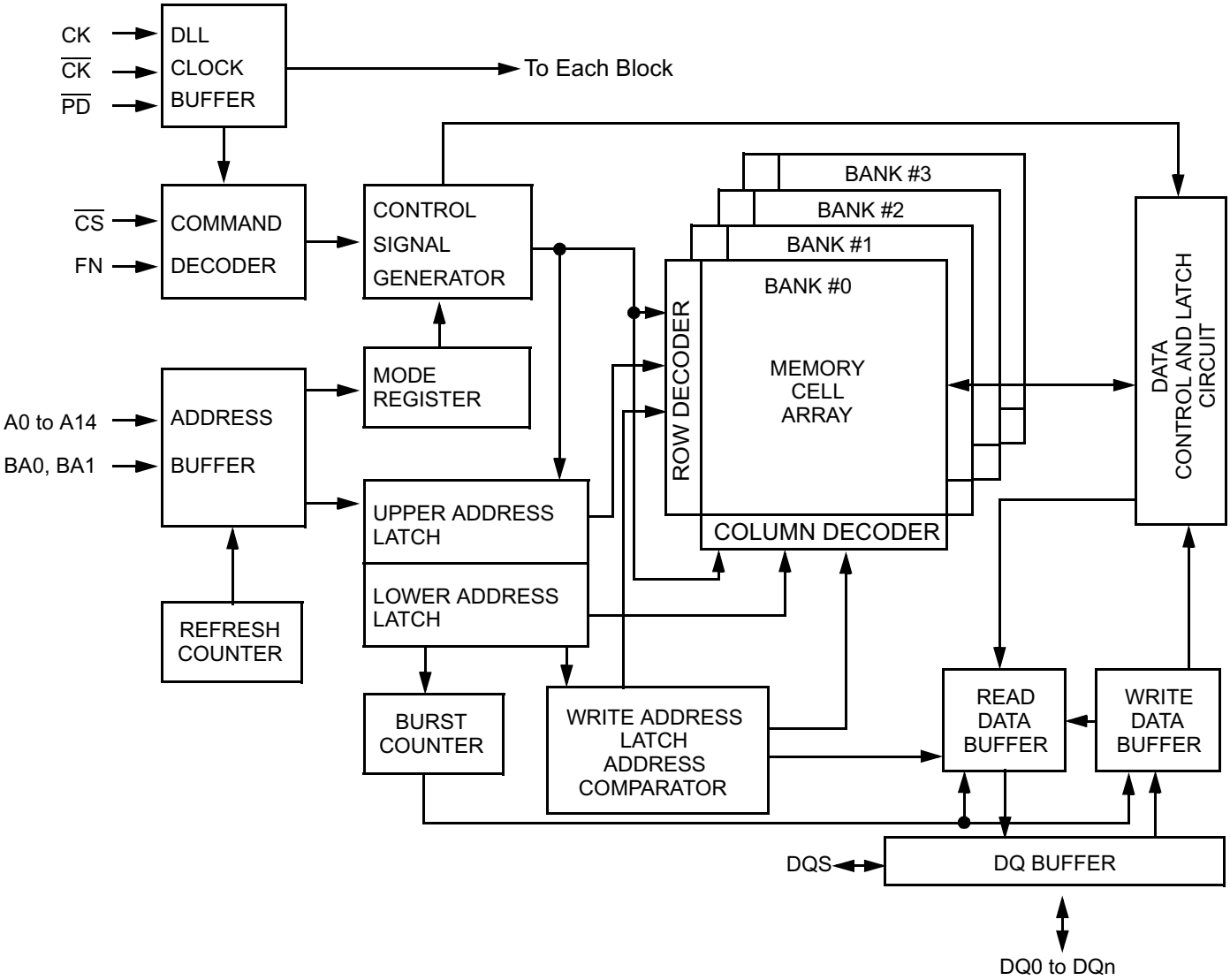


Package Outline Drawing (TSOP II 66-P-400-0.65)

Unit in mm



Block Diagram



Note : The K4C560838C-TC configuration is 327768X256X 8 of cell array with the DQ pins numbered DQ0-7
The K4C561638C-TC configuration is 327768X128X16 of cell array with the DQ pins numbered DQ0-15.

Absolute Maximum Ratings

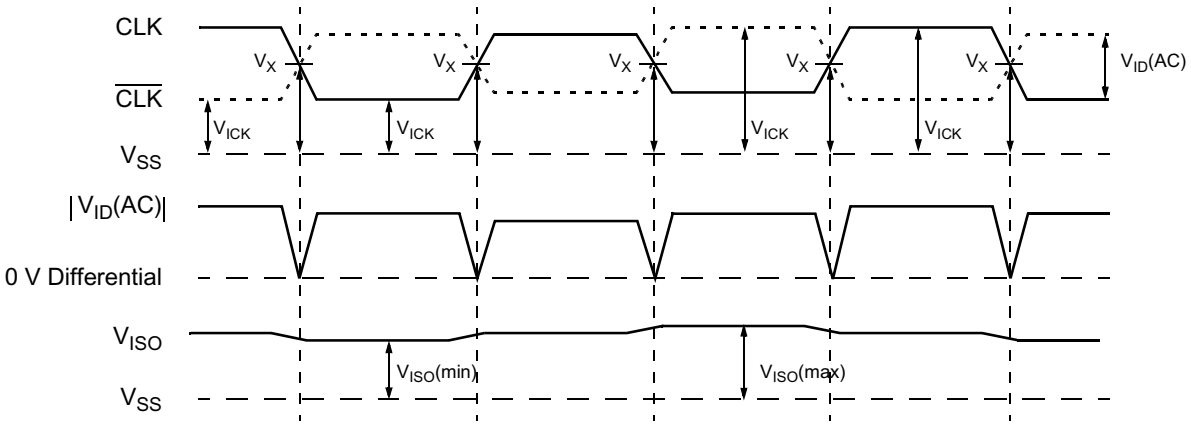
Symbol	Parameter	Rating	Units	Notes
Vdd	Power Supply Voltage	-0.3 to 3.3	V	
VddQ	Power Supply Voltage (for I/O buffer)	-0.3 to Vdd + 0.3	V	
V_{IN}	Input Voltage	-0.3 to Vdd + 0.3	V	
V_{OUT}	DQ pin Voltage	-0.3 to VddQ + 0.3	V	
V_{REF}	Input Reference Voltage	-0.3 to 3.3	V	
T_{OPR}	Operating Temperature	0 to 70	^{o}C	
T_{STG}	Storage Temperature	-55 to 150	^{o}C	
T_{SOLDER}	Soldering Temperature(10s)	260	^{o}C	
P_D	Power Dissipation	1	W	
I_{OUT}	Short Circuit Output Current	± 50	mA	

Caution : Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may affect device reliability.

Recommanded DC,AC Operating Conditions (Notes : 1) (Ta = 0 to 70 ×C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
Vdd	Power Supply Voltage	2.35	2.5	2.65	V	
VddQ	Power Supply Voltage (for I/O Buffer)	2.35	Vdd	Vdd	V	
V_{REF}	Input Reference Voltage	VddQ/2*96%	VddQ/2	VddQ/2*104%	V	2
V_{IH} (DC)	Input DC high Voltage	V_{REF}+0.2	-	VddQ+0.2	V	5
V_{IL}(DC)	Input DC Low Voltage	-0.1	-	V_{REF}-0.2	V	5
V_{ICK} (DC)	Differential Clock DC Input Voltage	-0.1	-	VddQ+0.1	V	10
V_{ID} (DC)	Input Differential Voltage. CK and $\overline{CK}$ Inputs (DC)	0.4	-	VddQ+0.2	V	7,10
V_{IH} (AC)	Input AC High Voltage	V_{REF}+0.35	-	VddQ+0.2	V	3,6
V_{IL} (AC)	Input AC Low Voltage	-0.1	-	V_{REF}-0.35	V	4,6
V_{ID} (AC)	Input Differential Voltage. CK and $\overline{CK}$ Inputs (AC)	0.7	-	VddQ+0.2	V	7,10
V_X (AC)	Differential AC Input Cross Point Voltage	VddQ/2-0.2	-	VddQ/2+0.2	V	8,10
V_{ISO} (AC)	Differential Clock AC Middle Level	VddQ/2-0.2	-	VddQ/2+0.2	V	9,10

Notes:
1. All voltages are referenced to Vss, VssQ.
2. V_{REF} is expected to track variations in VddQ DC level of the transmitting device. Peak to peak AC noise on V_{REF} may not exceed ± 2% of V_{REF} (DC).
3. Overshoot limit : V_{IH}(max.) = VddQ + 0.9V with a pulse width <= 5ns
4. Undershoot limit : V_{IL}(min.) = -0.9V with a pulse width <= 5ns
5. V_{IH}(DC) and V_{IL}(DC) are levels to maintain the current logic state.
6. V_{IH}(AC) and V_{IL}(AC) are levels to change to the new logic state.
7. V_{ID} is magnitude of the difference between CK input level and $\overline{CK}$ input level.
8. The value of Vx(AC) is expected to equal VddQ/2 of the transmitting device.
9. V_{ISO} means [V_{ICK}(CK) + V_{ICK}($\overline{CK}$)]/2
10. Refer to the figure below.



11. In the case of external termination, VTT(Termination Voltage) should be gone in the range of V_{REF}(DC) ± 0.04V.

Pin Capacitance (Vdd.VddQ = 2.5V, f = 1MHz, Ta = 25×C)

Symbol	Parameter	Min	Max	Units
C_{IN}	Input Pin Capacitance	2.5	4.0	pF
C_{INC}	Clock Pin (CK, CK) Capacitance	2.5	4.0	pF
$C_{I/O}$	I/O Pin (DQ, DQS) Capacitance	4.0	6.0	pF
C_{NC}^{1}	NC1 Pin Capacitance	-	1.5	pF
C_{NC}^{2}	NC2 Pin Capacitance	4.0	6.0	pF

Note : These parameters are periodically sampled and not 100% tested.
The NC^2 pins have additional capacitance for adjustment of the adjacent pin capacitance.
The NC^2 pins have Power and Ground clamp.

DC Characteristics and Operating Conditions (Vdd, VddQ = 2.5V ± 0.15V, Ta = 0~70×C)

Item	Symbol	Max		Units	Notes
		B(200MHz)	A(167MHz)		
Operating Current t_{CK} = min, I_{RC}=min Read/Write command cycling OV<=V_{IN}<=$V_{IL(AC)}$ (max.) $V_{IH(AC)}$(min.) <=V_{IN}<=VddQ 1 bank operation, Burst Length = 4 Address change up to 2 times during minimum I_{RC}.	I_{DD1S}	324	317	mA	1, 2
Standby Current t_{CK}=min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IH}, 0V<=V_{IN}<=$V_{IL(AC)}$(max.) $V_{IH(AC)}$(min.)<=V_{IH}<=VddQ All Banks : inactive state Other input signals are changed one time during 4*t_{CK}	I_{DD2N}	78.7	77		1
Standby (Power Down) Current t_{CK}=min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IL} (Power Down) 0V<=V_{IN}<=VddQ All Banks : inactive state	I_{DD2P}	2	2		1
Auto-Refresh Current t_{CK} = min, I_{REFC}= min, t_{REFI} = min Auto-Refresh command cycling 0V<=V_{IN}<=V_{IL}(AC) (max.), V_{IH}(AC) (min.) <=V_{IN}<=VddQ Address change up to 2 times during minimum I_{REFC}.	I_{DD5}	214	209		1
Self-Refresh Current self-Refresh mode $\overline{PD}$ = 0.2V, OV<=V_{IN}<=VddQ	I_{DD6}	3	3		

Item		Symbol	Min	Max	Unit	Notes
Input Leakage Current (0V<=V_{IN}<=VddQ, All other pins not under test = 0V)		I_{LI}	-5	5	uA	
Output Leakage Current (Output disabled, 0V<=V_{OUT}<=VddQ)		I_{LO}	-5	5	uA	
V_{REF} Current		I_{REF}	-5	5	uA	
Normal Output Driver	Output Source DC Current V_{OH} = VddQ - 0.4V	I_{OH}(DC)	-10	-	mA	3
	Output Sink DC Current V_{OL}=0.4V	I_{OL}(DC)	10	-		3
Strong Output Driver	Output Source DC Current V_{OH} = VddQ - 0.4V	I_{OH}(DC)	-11	-		3
	Output Sink DC Current V_{OL}=0.4V	I_{OL}(DC)	11	-		3
Weaker Output Driver	Output Source DC Current V_{OH} = VddQ - 0.4V	I_{OH}(DC)	-8	-		3
	Output Sink DC Current V_{OL}=0.4V	I_{OL}(DC)	8	-		3
Weakest Output Driver	Output Source DC Current V_{OH} = VddQ - 0.4V	I_{OH}(DC)	-7	-		3
	Output Sink DC Current V_{OL}=0.4V	I_{OL}(DC)	7	-		3

Notes : 1. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK}, t_{RC} and I_{RC}.
2. These parameters depend on the output loading. The specified values are obtained with the output open.
3. Refer to output driver characteristics for the detail. Output Driver Strength is selected by Extended Mode Register.

AC Characteristics and Operating Conditions (Notes : 1, 2)

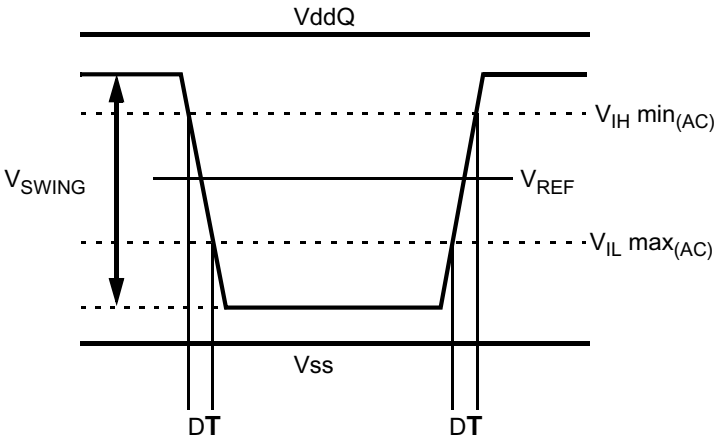
Symbol	Item		B(200MHz)		A(167MHz)		Units	Notes
			Min	Max	Min	Max		
t_{RC}	Random Cycle Time		25	-	30	-	ns	3
t_{CK}	Clock Cycle Time	CL = 3	5.5	8.5	6.5	12		3
		CL = 4	5	8.5	6	12		3
t_{RAC}	Random Access Time		-	22	-	26		3
t_{CH}	Clock High Time		0.45*t_{CK}	-	0.45*t_{CK}	-		3
t_{CL}	Clock Low Time		0.45*t_{CK}	-	0.45*t_{CK}	-		3
t_{CKQS}	DQS Access Time from CLK		-0.65	0.65	-0.85	0.85		3, 8
t_{QSQ}	Data Output Skew from DQS		-	0.4	-	0.5		4
t_{AC}	Data Access Time from CLK		-0.65	0.65	-0.85	0.85		3, 8
t_{OH}	Data Output Hold Time from CLK		-0.65	0.65	-0.85	0.85		3, 8
t_{QSPRE}	DQS(Read) Preamble Pulse Width		0.9*t_{CK}-0.2	1.1*t_{CK}+0.2	0.9*t_{CK}-0.2	1.1*t_{CK}+0.2		3
t_{HP}	CLK half period (minium of Actual t_{CH}, t_{CL})		min(t_{CH}, t_{CL})	-	min(t_{CH}, t_{CL})	-		
t_{QSP}	DQS(Read) Pulse Width		t_{HP}-0.55	-	t_{HP}-0.65	-		4
t_{QSQV}	Data Output Valid Time from DQS		t_{HP}-0.55	-	t_{HP}-0.65	-		4
t_{DQSS}	DQS(Write) Low to High Setup Time		0.75*t_{CK}	1.25*t_{CK}	0.75*t_{CK}	1.25*t_{CK}		3
t_{DSPRE}	DQS(Write) Preamble Pulse Width		0.4*t_{CK}	-	0.4*t_{CK}	-		4
t_{DSPRES}	DQS First Input Setup Time		0	-	0	-		3
t_{DSPREH}	DQS First Low Input Hold Time		0.25*t_{CK}	-	0.25*t_{CK}	-		3
t_{DSP}	DQS High or Low Input Pulse Width		0.45*t_{CK}	0.55*t_{CK}	0.45*t_{CK}	0.55*t_{CK}		4
t_{DSS}	DQS Input Falling Edge to Clock Setup Time	CL = 3	1.3	-	1.5	-		3, 4
		CL = 4	1.3	-	1.5	-		3, 4
t_{DSPST}	DQS(Write) Postamble Pulse Width		0.45*t_{CK}	-	0.45*t_{CK}	-		4
t_{DSPSTH}	DQS(Write) Postamble Hold Time	CL = 3	1.3	-	1.5	-		3, 4
		CL = 4	1.3	-	1.5	-		3, 4
t_{DSSK}	UDQS - LDQS Skew (x16)		-0.5*t_{CK}	0.5*t_{CK}	-0.5*t_{CK}	0.5*t_{CK}		
t_{DS}	Data Input Setup Time from DQS		0.5	-	0.6	-		4
t_{DH}	Data Input Hold Time from DQS		0.5	-	0.6	-		4
t_{DIPW}	Data Input pulse Width (for each device)		1.5	-	1.9	-		
t_{IS}	Command / Address Input Setup Time		0.9	-	1	-		3
t_{IH}	Command / Address Input Hold Time		0.9	-	1	-		3
t_{IPW}	Command / Address Input Pulse Width (for each device)		2.0	-	2.2	-		
t_{LZ}	Data-out Low Impedance Time from CLK		-0.65	-	-0.85	-		3, 6, 8
t_{HZ}	Data-out High Impedance Time from CLK		-	0.65	-	0.85		3, 7, 8
t_{QSLZ}	DQS-out Low Impedance Time from CLK		-0.65	-	-0.85	-		3, 6, 8
t_{QSHZ}	DQS-out High Impedance Time from CLK		-0.65	0.65	-0.85	0.85		3, 7, 8
t_{QPDH}	Last Output to $\overline{PD}$ High Hold Time		0	-	0	-		
t_{PDEX}	Power Down Exit Time		2	-	2	-		3
t_T	Input Transition Time		0.1	1	0.1	1		
t_{FPDL}	$\overline{PD}$ Low Input Window for Self-Refresh Entry		-0.5*t_{CK}	5	-0.5*t_{CK}	5		3

AC Characteristics and Operating Conditions (Notes : 1, 2) (Continued)

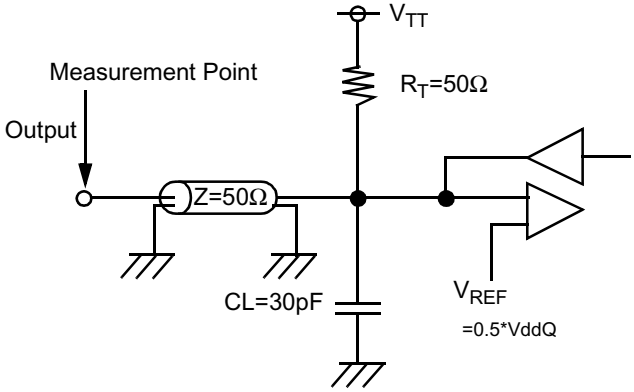
Symbol	Item		B(200MHz)		A(167MHz)		Units	Notes
			Min	Max	Min	Max		
t_{REFI}	Auto-Refresh Average Interval		0.4	7.8	0.4	7.8	us	5
t_{PAUSE}	Pause Time after Power-up		200	-	200	-		
I_{RC}	Random Read/Write Cycle Time	CL = 3	5	-	5	-	Cycle	
	(Applicable to Same Bank)	CL = 4	5	-	5	-		
I_{RCD}	RDA/WRA to LAL Command Input Delay (Applicable to Same Bank)		1	1	1	1		
I_{RAS}	LAL to RDA/WRA Command Input Delay (Applicable to Same Bank)	CL = 3	4	-	4	-		
		CL = 4	4	-	4	-		
I_{RBD}	Random Bank Access Delay (Applicable to Other Bank)		2	-	2	-		
I_{RWD}	LAL following RDA to WRA Delay (Applicable to Other Bank)	BL = 2	2	-	2	-		
		BL = 4	3	-	3	-		
I_{WRD}	LAL following WRA to RDA Delay (Applicable to Other Bank)		1	-	1	-		
I_{RSC}	Mode Register Set Cycle Time	CL = 3	5	-	5	-		
		CL = 4	5	-	5	-		
I_{PD}	$\overline{PD}$ Low to Inactive State of Input Buffer		-	1	-	1		
I_{PDA}	$\overline{PD}$ High to Active State of Input Buffer		-	1	-	1		
I_{PDV}	Power down mode valid from REF command	CL = 3	15	-	15	-		
		CL = 4	18	-	18	-		
I_{REFC}	Auto-Refresh Cycle Time	CL = 3	15	-	15	-		
		CL = 4	18	-	18	-		
I_{CKD}	REF Command to Clock Input Disable at Self-Refresh Entry		16	-	16	-		
I_{LOCK}	DLL Lock-on Time (Applicable to RDA command)		200	-	200	-		

AC Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{IH}(min)	Input high voltage (minimum)	V_{REF} + 0.35	V	
V_{IL} (max)	Input low voltage (maximum)	V_{REF} - 0.35	V	
V_{REF}	Input reference voltage	VddQ/2	V	
V_{TT}	Termination voltage	V_{REF}	V	
V_{SWING}	Input signal peak to peak swing	1.0	V	
V_R	Differential clock input reference level	$V_{X(AC)}$	V	
V_{ID}(AC)	Input differential voltage	1.5	V	
SLEW	Input signal minimum slew rate	1.0	V/ns	
V_{OTR}	Output timing measurement reference voltage	VddQ/2	V	



Slew=($V_{IH}min_{(AC)}$ - $V_{IL}max_{(AC)}$/DT



Output Load Circuit(SSTL_2)

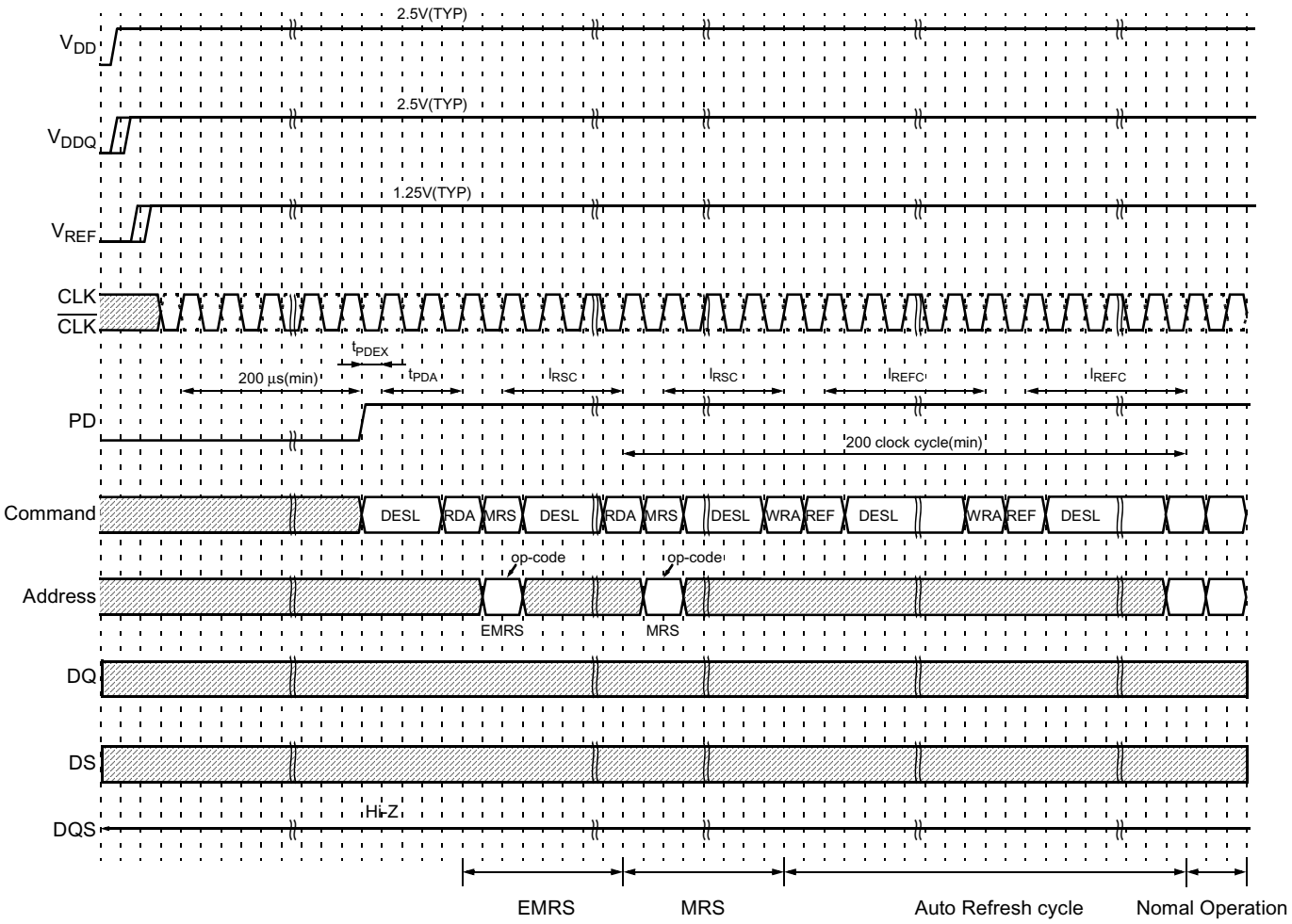
Notes : 1. Transition times are measured between V_{IH} $min_{(DC)}$ and V_{IL} $max_{(DC)}$.
Transition (rise and fall) of input signals have a fixed slope.

2. If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., t_{DQSS} = 0.75*t_{CK}, t_{CK} = 5ns, 0.75*5ns = 3.75ns is rounded up to 3.8ns.)
3. These parameters are measured from the differential clock (CK and $\overline{CK}$) AC cross point.
4. These parameters are measured from signal transition point of DQS crossing V_{REF} level.
5. The t_{REFI} (MAX.) applies to equally distributed refresh method.
The t_{REFI} (MIN.) applies to both burst refresh method and distributed refresh method.
In such case, the average interval of eight consecutive Auto-Refresh commands has to be more than 400ns always. In other words, the number of Auto- Refresh cycles which can be performed within 3.2us (8X400ns) is to 8 times in the maximum.
6. Low Impedance State is speified at VddQ/2± 0.2V from steady state.
7. High Impedance State is specified where output buffer is no longer driven.
8. These parameters depend on the clock jitter. These parameters are measured at stable clock.

Power Up Sequence

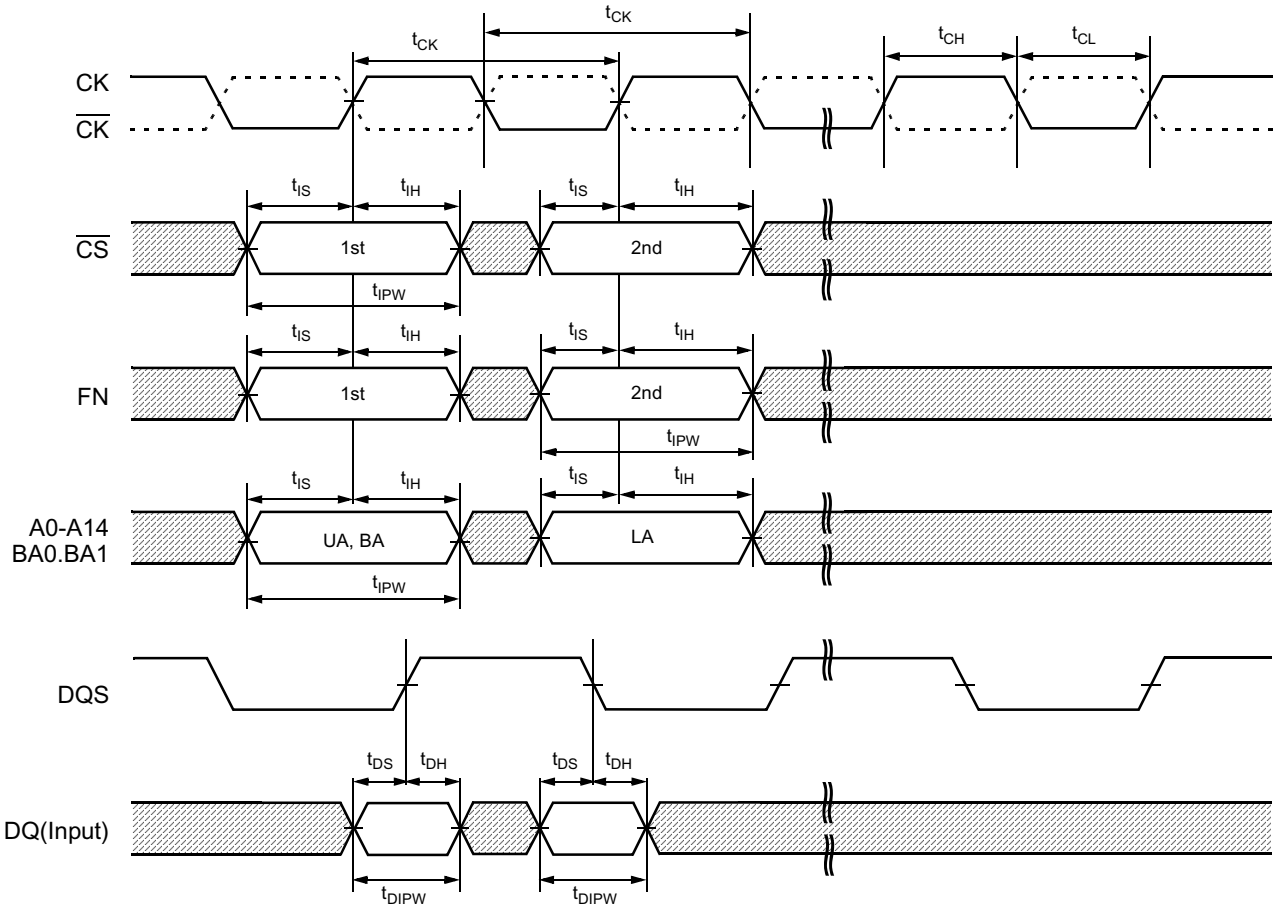
1. As for $\overline{PD}$, being maintained by the low state (°¬0.2V) is desirable before a power-supply injection.
2. Apply Vdd before or at the same time as VddQ.
3. Apply VddQ before or at the same time as V_{REF}.
4. Start clock (CK, $\overline{CK}$) and maintain stable condition for 200us (min.).
5. After stable power and clock, apply DESL and take $\overline{PD}$ = H.
6. Issue EMRS to enable DLL and to define driver strength. (Note : 1)
7. Issue MRS for set $\overline{CAS}$ Latency (CL), Burst Type (BT), and Burst Length (BL). (Note : 1)
8. Issue two or more Auto-Refresh commands. (Note:1)
9. Ready for normal operation after 200 clocks from Extended Mode Register programming. (Note : 2)

Note : 1. Sequence 6, 7 and 8 can be issued in random order.
2. L=Logic Low, H = Logic High



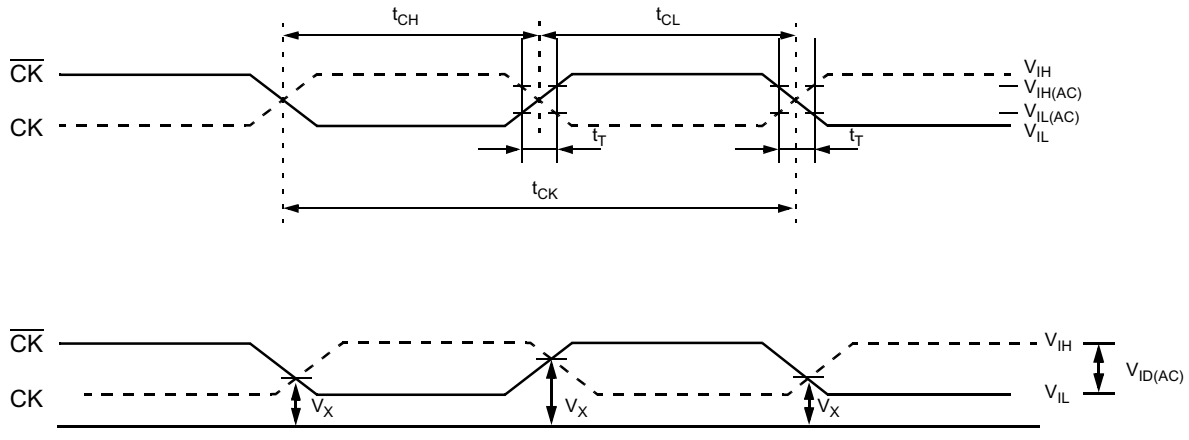
Basic Timing Diagrams

Input Timing

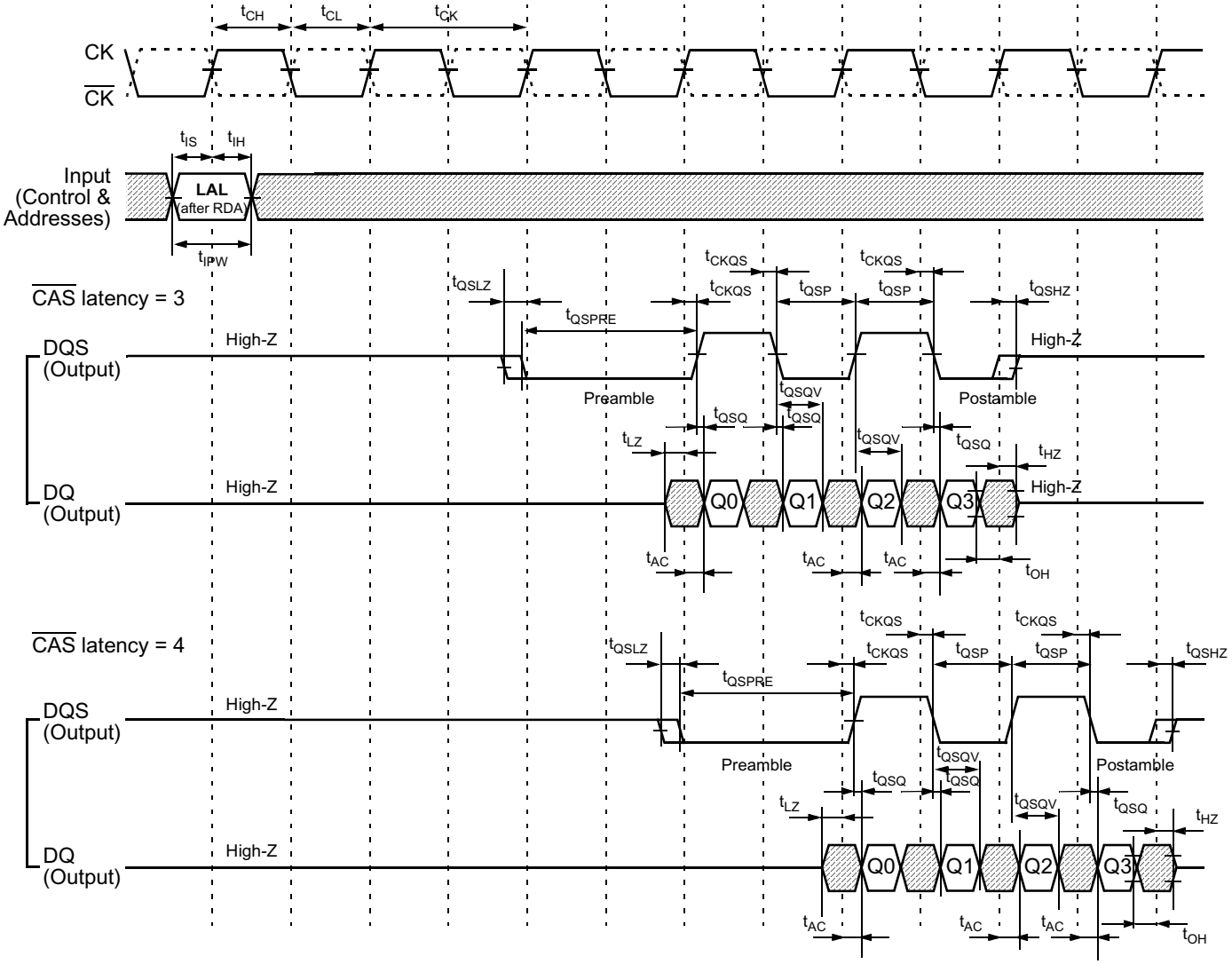


Refer to the Command Truth Table.

Timing of the CK, /CK



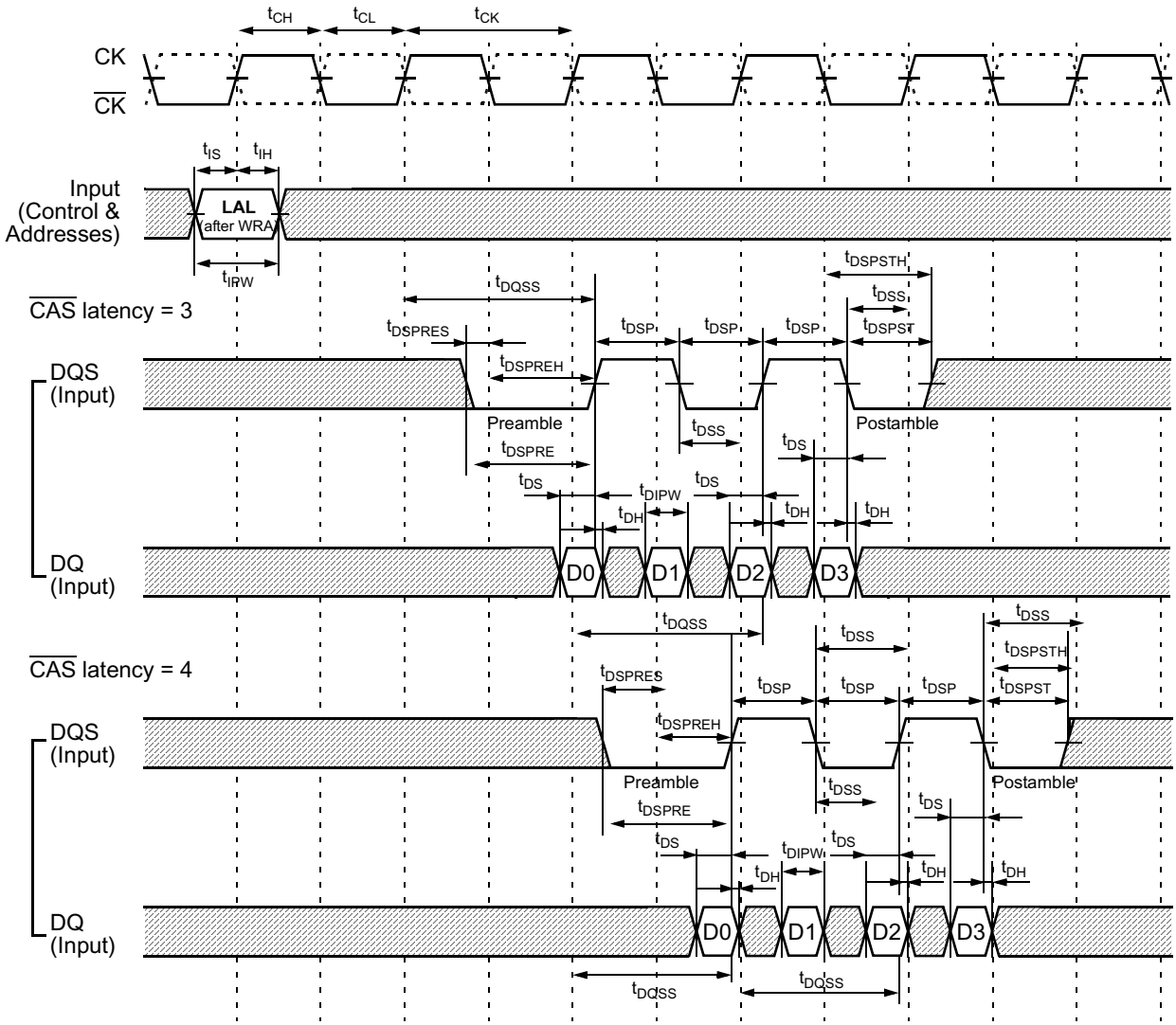
Read Timing (Burst Length = 4)



Note : The correspondence of LDQS, UDQS to DQ. (K4C561638C-TC)

LDQS	DQ0 to 7
UDQS	DQ8 to 15

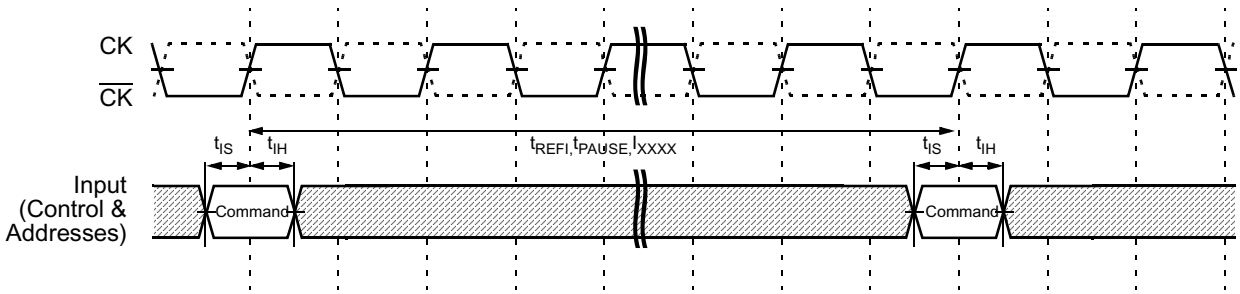
Write Timing (Burst Length = 4)



Note. The correspondence of LDQS, UDQS to DQ. (K4C561638C-TC)

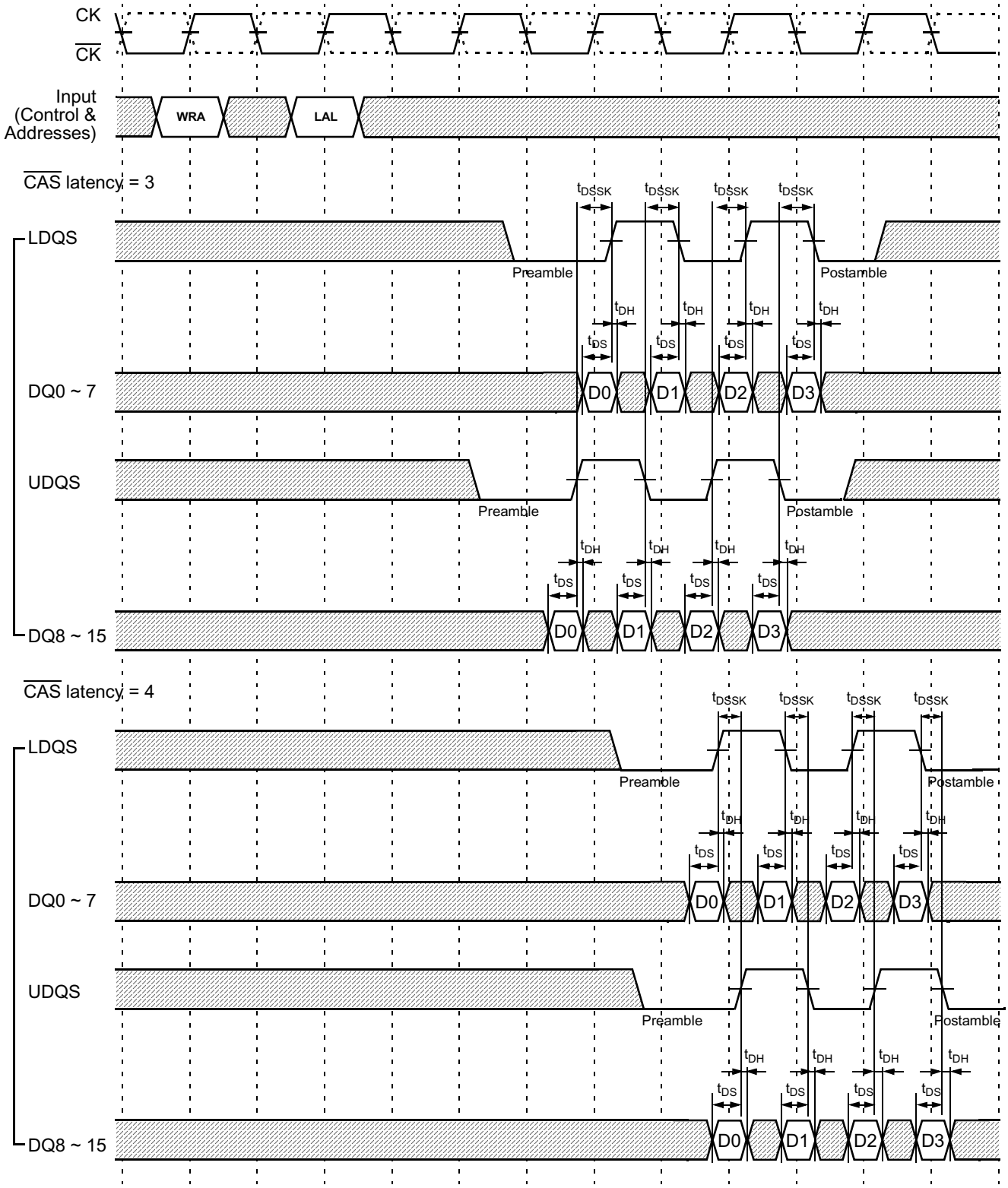
LDQS	DQ0 to 7
UDQS	DQ8 to 15

tREFI, tPAUSE, Ixxxx Timing



Note. "I_{XXXX}"means "I_{RC}", "I_{RCD}", "I_{RAS}", etc.

Write Timing (x16 device) (Burst Length = 4)



Function Truth Table (Notes : 1,2,3)

Command Truth Table (Notes : 4)

•The First Command

Symbol	Function	$\overline{CS}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0
DESL	Device Deselect	H	X	X	X	X	X	X
RDA	Read with Auto-close	L	H	BA	UA	UA	UA	UA
WRA	Write with Auto-close	L	L	BA	UA	UA	UA	UA

•The Second Command (The next clock of RDA or WRA command)

Symbol	Function	$\overline{CS}$	FN	BA1-BA0	A14-A13	A12-A11	A10-A9	A8	A7	A6-A0
LAL	Lower Address Latch (x16)	H	X	X	V	V	X	X	X	LA
LAL	Lower Address Latch (x8)	H	X	X	V	X	X	X	LA	LA
REF	Auto-Refresh	L	X	X	X	X	X	X	X	X
MRS	Mode Register Set	L	X	V	L	L	L	L	V	V

Notes : 1. L = Logic Low, H = Logic High, X = either L or H, V = Valid (Specified Value), BA = Bank Address, UA = Upper Address, LA = Lower Address.
2. All commands are assumed to issue at a valid state.
3. All inputs for command (excluding SELFX and PDEX) are latched on the crossing point of differential clock input where CLK goes to High.
4. Operation mode is decided by the comination of 1st command and 2nd command refer to "STATE DIAGRAM" and the command table below.

Read Command Table

Command (Symbol)	$\overline{CS}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
RDA (1st)	L	H	BA	UA	UA	UA	UA	
LAL (2nd)	H	X	X	X	X	LA	LA	5

Notes : 5. For x16 device, A7 is "X" (either L or H).

Write Command Table

K4C561638C-TC

Command (Symbol)	$\overline{CS}$	FN	BA1-BA0	A14	A13	A12	A11	A10-A9	A8	A7	A6-A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	X	X	LVWO	LVW1	UVW0	UVW1	X	X	X	LA

K4C560838C-TC

Command (Symbol)	$\overline{CS}$	FN	BA1-BA0	A14	A13	A12	A11	A10-A9	A8	A7	A6-A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	X	X	VWO	VW1	X	X	X	X	LA	LA

Note : 6. A14 to A11 are used for variable Write Length (VW) control at Write Operation.

VW Truth Table

	Function	*VW0*	*VW1*
BL = 2	Write All Words	L	X
	Write First One Word	H	X
BL = 4	Reserved	L	L
	Write All Words	H	L
	Write First Two Words	L	H
	Write First One Word	H	H

Note : 7. For x16 device, LVW0 and LVW1 control DQ0-DQ7, UVW0 and UVW1 control DQ8-DQ15.

Mode Register Set Command Truth Table

Command (Symbol)	$\overline{CS}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
RDA (1st)	L	H	X	X	X	X	X	
MRS (2nd)	L	X	V	L	L	V	V	8

Note : 8. Refer to "Mode Register Table".

Function Truth Table (Continued)

Auto-Refresh Command Table

Function	Command (Symbol)	Current State	$\overline{PD}$		$\overline{CS}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
			n-1	n								
Active	WRA(1st)	Standby	H	H	L	L	X	X	X	X	X	
Auto-Refresh	REF(2nd)	Active	H	H	L	X	X	X	X	X	X	

Self-Refresh Command Table

Function	Command (Symbol)	Current State	$\overline{PD}$		$\overline{CS}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
			n-1	n								
Active	WRA(1st)	Standby	H	H	L	L	X	X	X	X	X	
Self-Refresh Entry	REF(2nd)	Active	H	L	L	X	X	X	X	X	X	9, 10
Self-Refresh Continue	-	Self-Refresh	L	L	X	X	X	X	X	X	X	
Self-Refresh Exit	SELFX	Self-Refresh	L	H	H	X	X	X	X	X	X	11

Power Down Table

Function	Command (Symbol)	Current State	$\overline{PD}$		$\overline{CS}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
			n-1	n								
Power Down Entry	PDEN	Standby	H	L	H	X	X	X	X	X	X	10
Power Down Continue	-	Power Down	L	L	X	X	X	X	X	X	X	
Power Down Exit	PDEX	Power Down	L	H	H	X	X	X	X	X	X	11

Notes : 9. $\overline{PD}$ has to be brought to Low within t_{FPDL} from REF command.
10. $\overline{PD}$ should be brought to Low after DQ's state turned high impedance.
11. When $\overline{PD}$ is brought to High from Low, this function is executed asynchronously.

Function Truth Table (Continued)

Current State	$\overline{PD}$ n-1	$\overline{PD}$ n	$\overline{CS}$	FN	Address	Command	Action	Notes
Idle	H	H	H	X	X	DESL	NOP	
	H	H	L	H	BA, UA	RDA	Row activate for Read	
	H	H	L	L	BA, UA	WRA	Row activate for Write	
	H	L	H	X	X	PDEN	Power Down Entry	12
	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Refer to Power Down state	
Row Active for Read	H	H	H	X	LA	LAL	Begin read	
	H	H	L	X	Op-Code	MRS/EMRS	Access to Mode Register	
	H	L	H	X	X	PDEN	Illegal	
	H	L	L	X	X	REF (Self)	Illegal	
	L	X	X	X	X	-	Invalid	
Row Active for Write	H	H	H	X	LA	LAL	Begin Write	
	H	H	L	X	X	REF	Auto-Refresh	
	H	L	H	X	X	PDEN	Illegal	
	H	L	L	X	X	REF (Self)	Self-Refresh entry	
	L	X	X	X	X	-	Invalid	
Read	H	H	H	X	X	DESL	Continue burst read to end	
	H	H	L	H	BA, UA	RDA	Illegal	13
	H	H	L	L	BA, UA	WRA	Illegal	13
	H	L	H	X	X	PDEN	Illegal	
	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
Write	H	H	H	X	X	DESL	Data write & continue burst write to end	13
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	13
	H	L	H	X	X	PDEN	Illegal	
	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
Auto-Refreshing	H	H	H	X	X	DESL	NOP-> Idle after I_{REFC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	X	X	PDEN	Self-Refresh entry	
	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Refer to Self-Refreshing state	
Mode Register Accessing	H	H	H	X	X	DESL	Nop-> Idle after I_{RSC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	X	X	PDEN	Illegal	14
	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
Power Down	H	X	X	X	X	-	Invalid	
	L	L	X	X	X	-	Maintain Power Down Mode	
	L	H	H	X	X	RDEX	Exit Power Down Mode->Idle after t_{PDEX}	
	L	H	L	X	X	-	Illegal	
Se;f-Refreshing	H	X	X	X	X	-	Invalid	
	L	L	X	X	X	-	Maintain Self-Refresh	
	L	H	H	X	X	SELFX	Exit Self-Refresh->Idle after I_{REFC}	
	L	H	L	X	X	-	Illegal	

Notes : 12. Illegal if any bank is not idle.
13. Illegal to bank in specified states : Function may be Legal in the bank indicated by bank Address (BA).
14. Illegal if t_{FPDL} is not Stisfied.

Mode Register Table

Regular Mode Register (Notes : 1)

Address	BA1[*1]	BA0[*1]	A14-A8	A7[*3]	A6-A4	A3	A2-A0
Register	0	0	0	TM	CL	BT	BL

A7	Test Mode (TM)
0	Regular (Default)
1	Test Mode Entry

A3	Burst Type (BT)
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency (CL)
0	0	X	Reserved [*2]
0	1	0	Reserved [*2]
0	1	1	3
1	0	0	4
1	0	1	Reserved [*2]
1	1	X	Reserved [*2]

A2	A1	A0	Burst Length (BL)
0	0	0	Reserved [*2]
0	0	1	2
0	1	0	4
0	1	1	Reserved [*2]
1	X	X	

Extended Mode Register (Notes : 4)

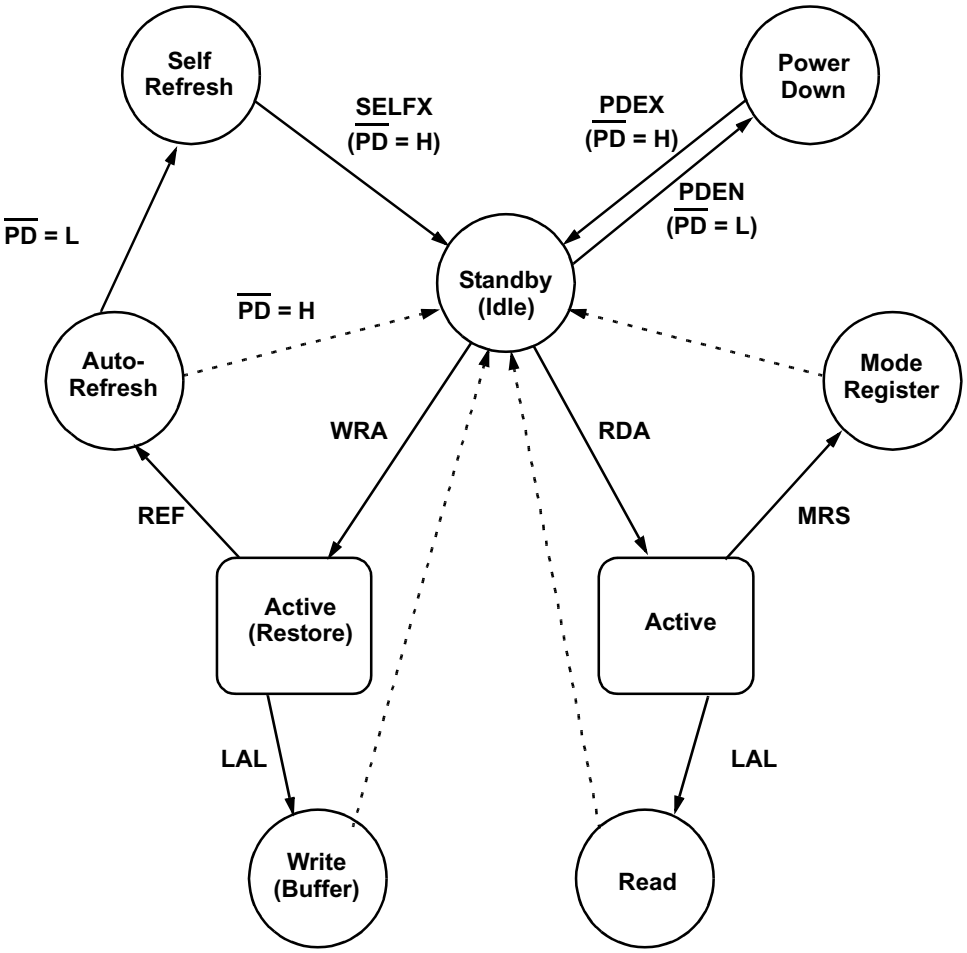
Address	BA1[*4]	BA0[*4]	A14-A7	A6	A5-A2	A1	A0
Register	0	1	0	DIC	0	DIC	DS

A6	A1	Output Driver Impedance Control (DIC)
0	0	Normal Output Driver
0	1	Strong Output Driver
1	0	Weaker Output Driver
1	1	Weakest Output Driver

A0	DLL Switch (DS)
0	DLL Enable
1	DLL Disable

Note : 1. Regular Mode Reister Is Chosen Using the combination of BA0 = 0 and BA1 = 0.
2. "Reserved" places in Regular Mode Register should not be set.
3. A7 in Regular Mode Register must be set to "0"(Low state).
Because 1est Mode is specific mode for supplier.
4. Extended Mode Register is chosen using the Combination of BA0 = 1 and BA1 = 0.

State Diagram



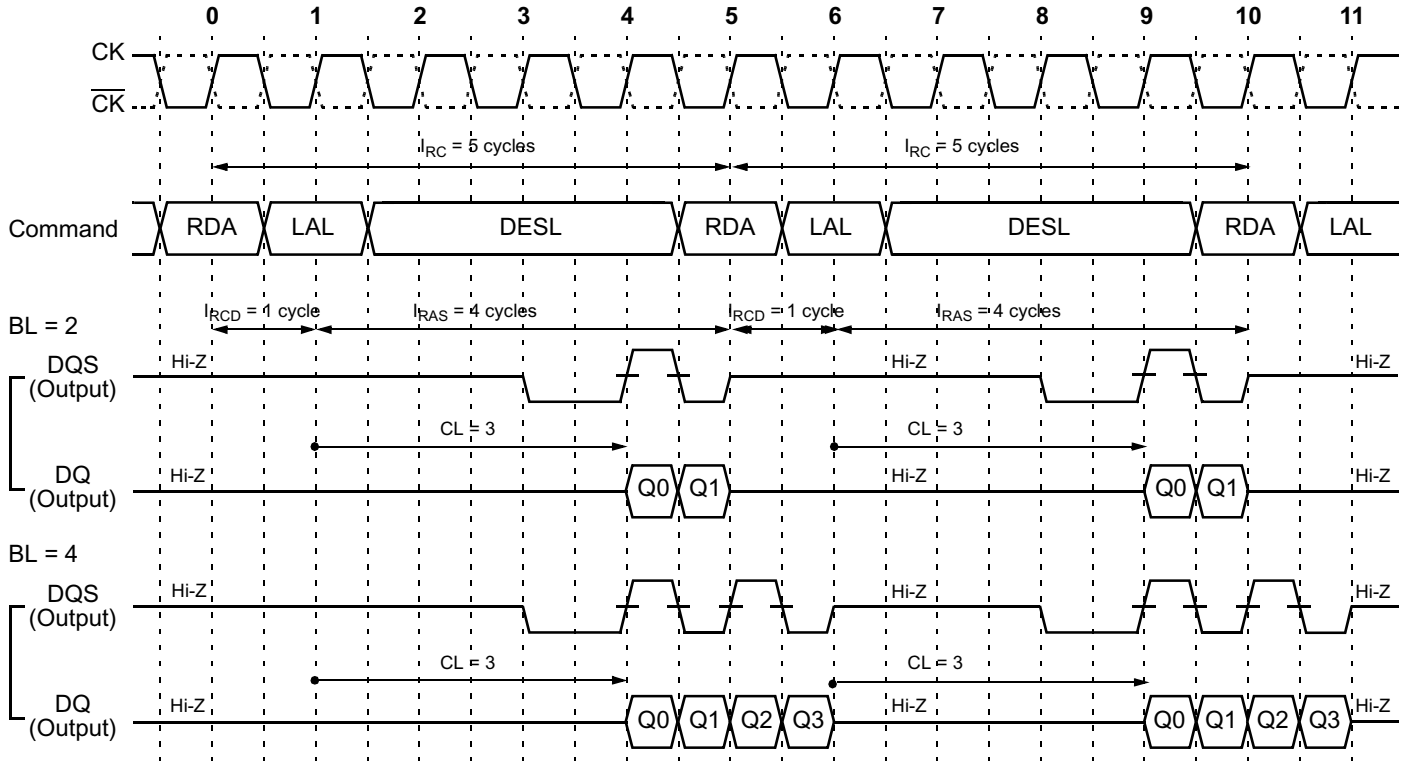
Command Input

Automatic Return

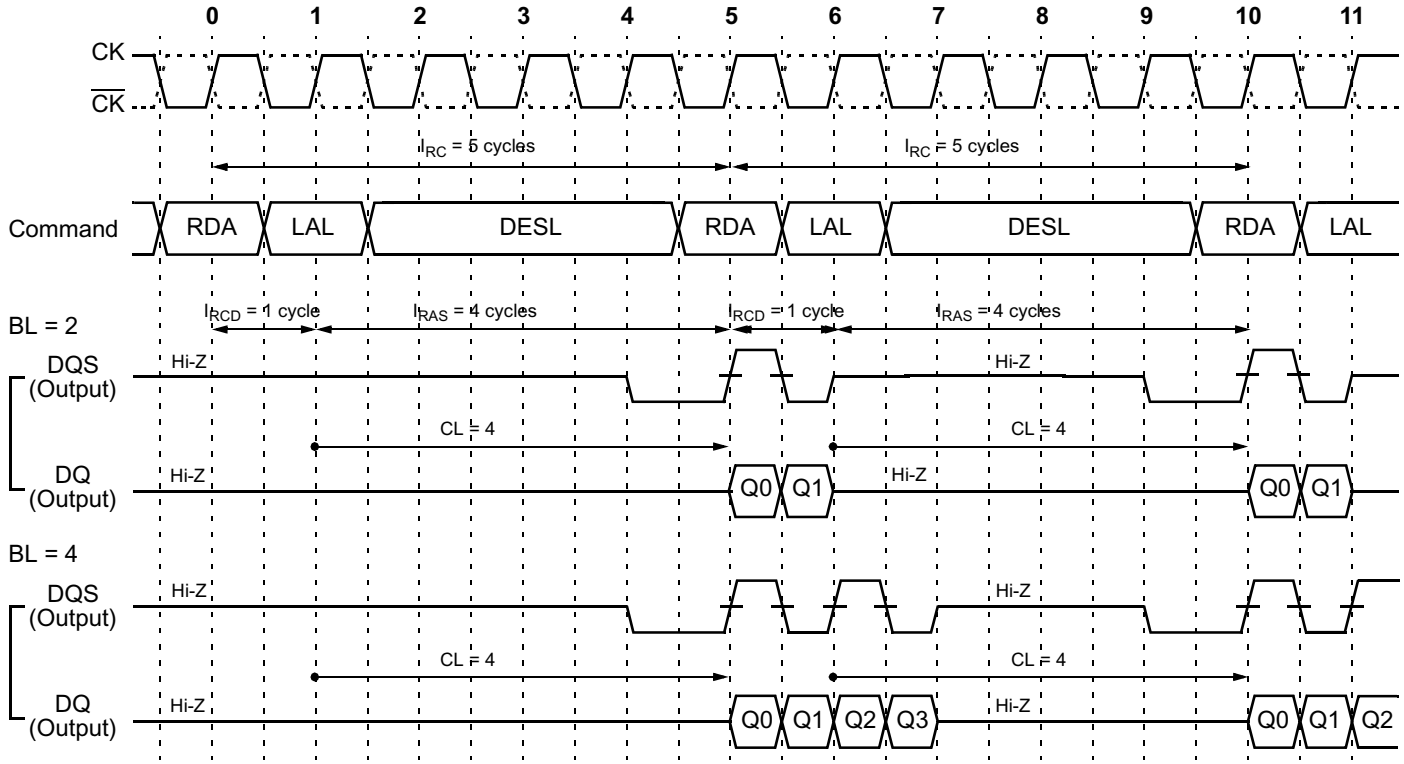
The second command at Active state must be issued 1clock after RDA or WRA command input

Timing Diagrams

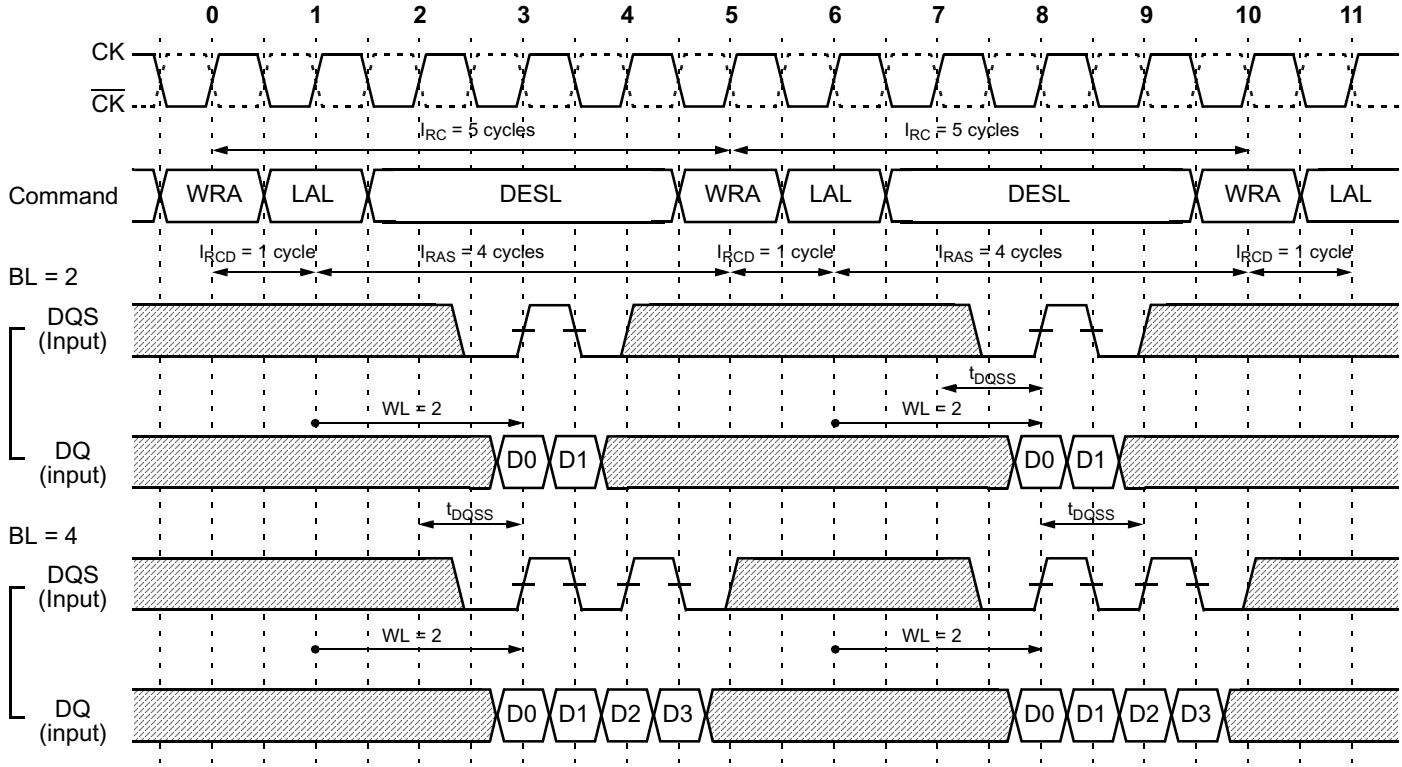
Single Bank Read Timing (CL = 3)



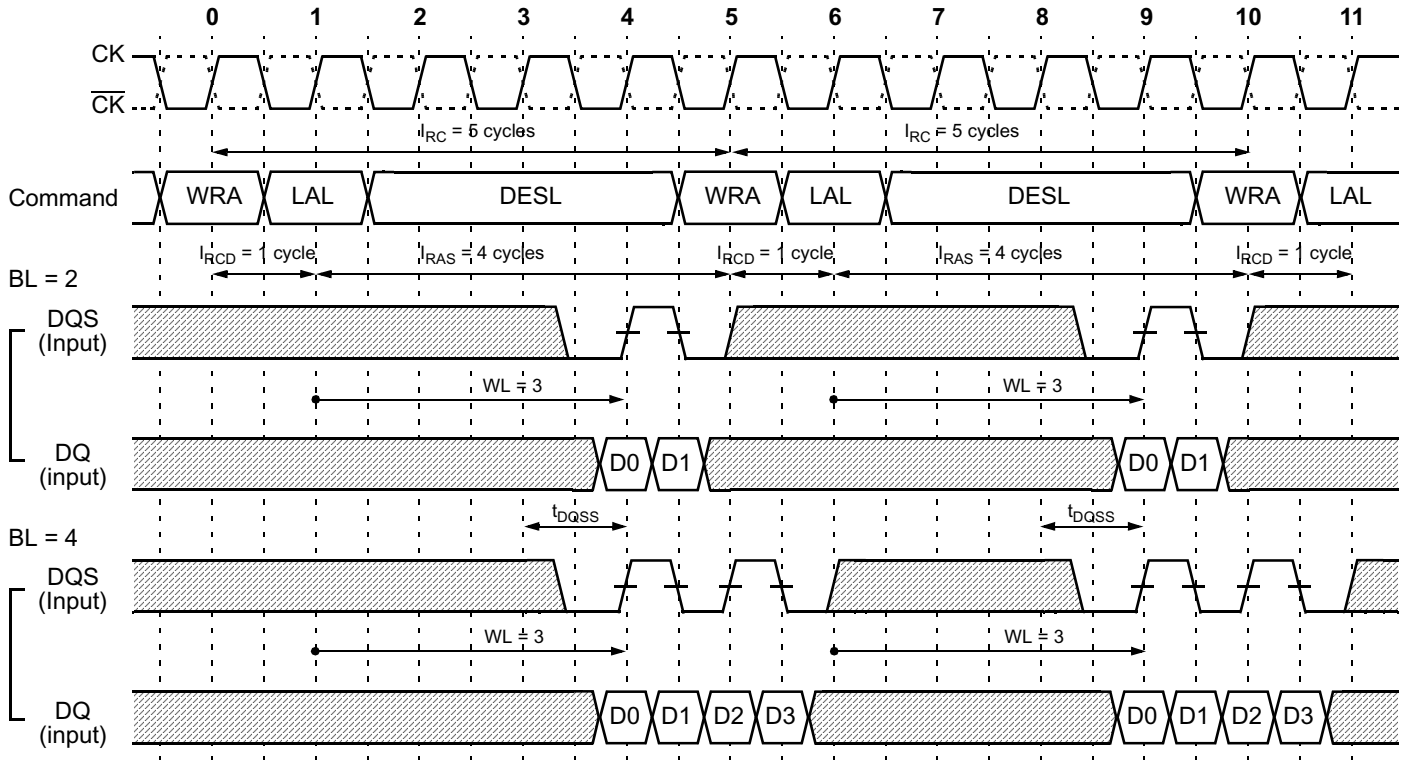
Single Bank Read Timing (CL = 4)



Single Bank Write Timing (CL = 3)

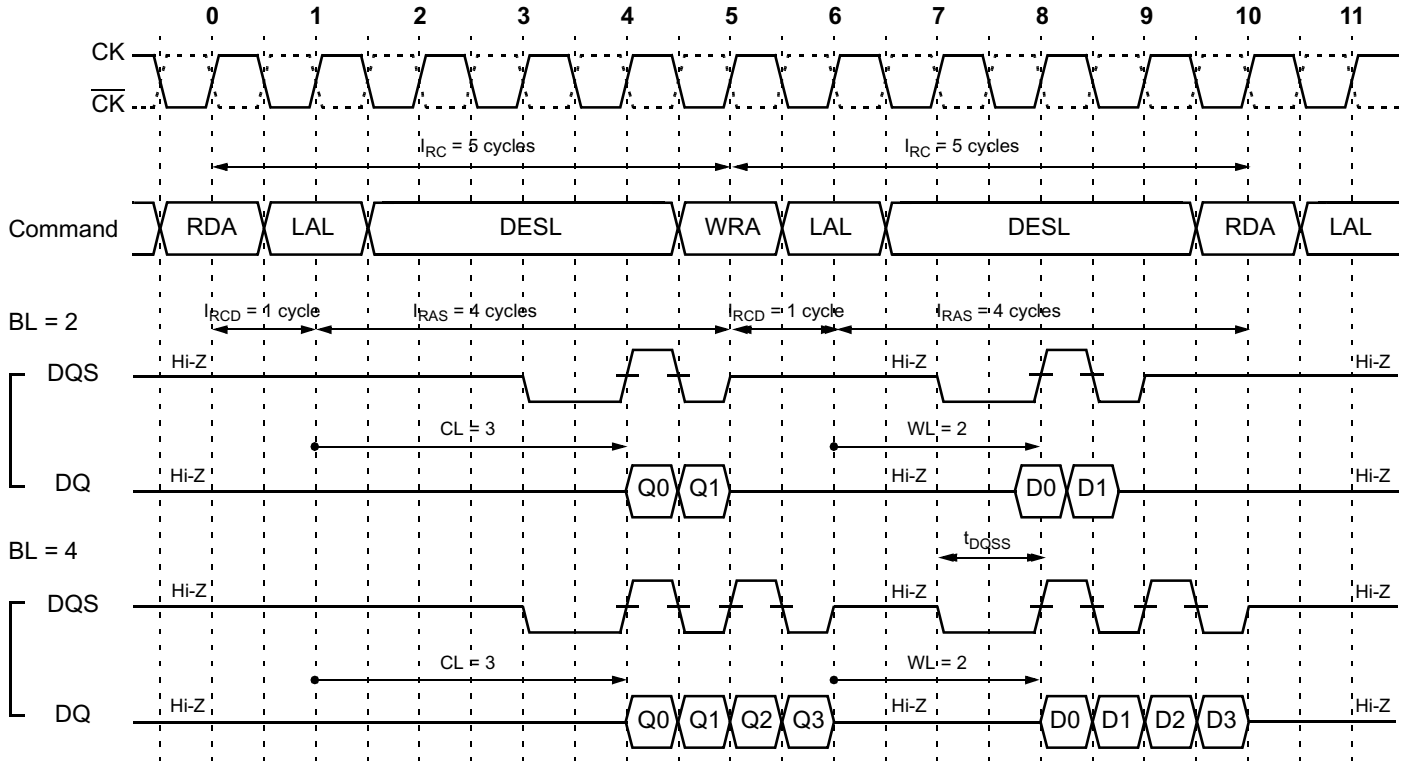


Single Bank Write Timing (CL = 4)

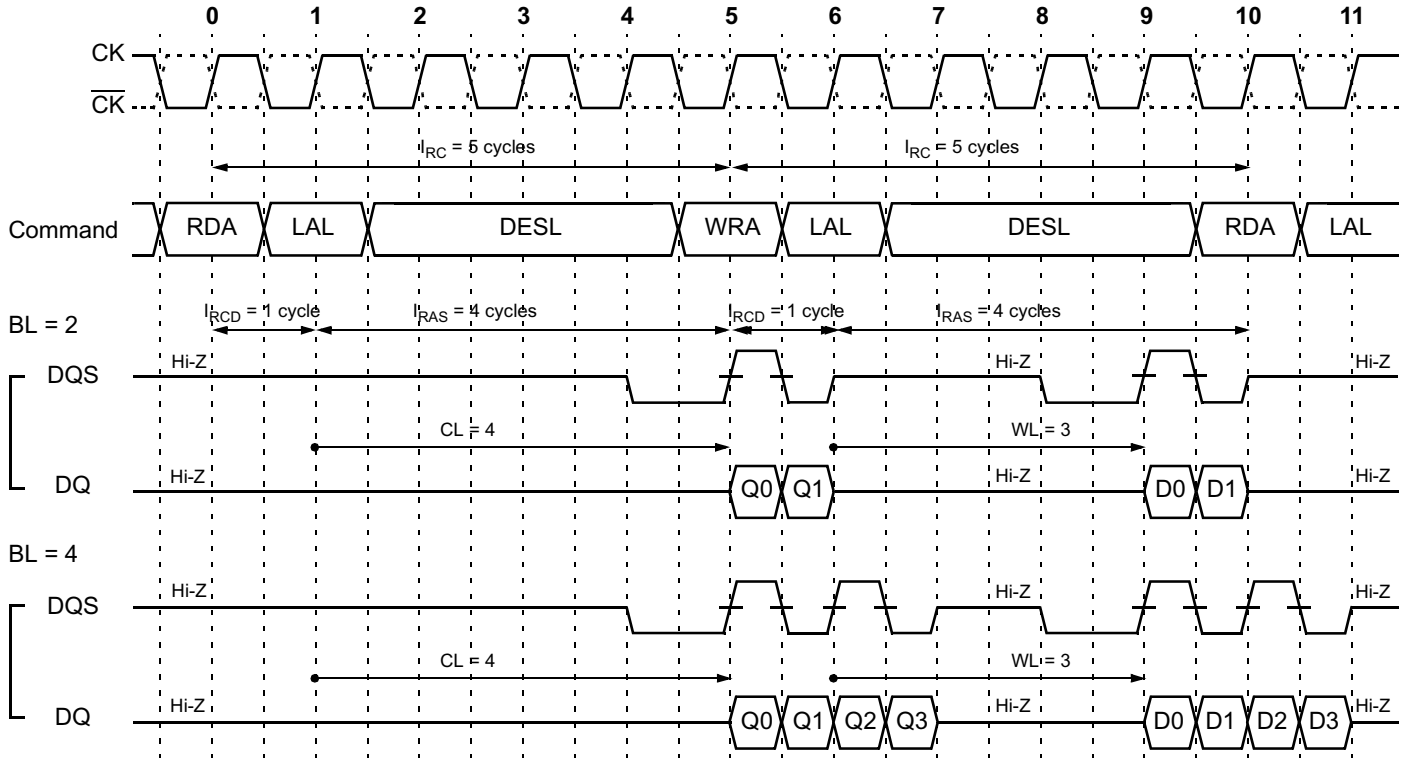


Note : means "H" or "L"

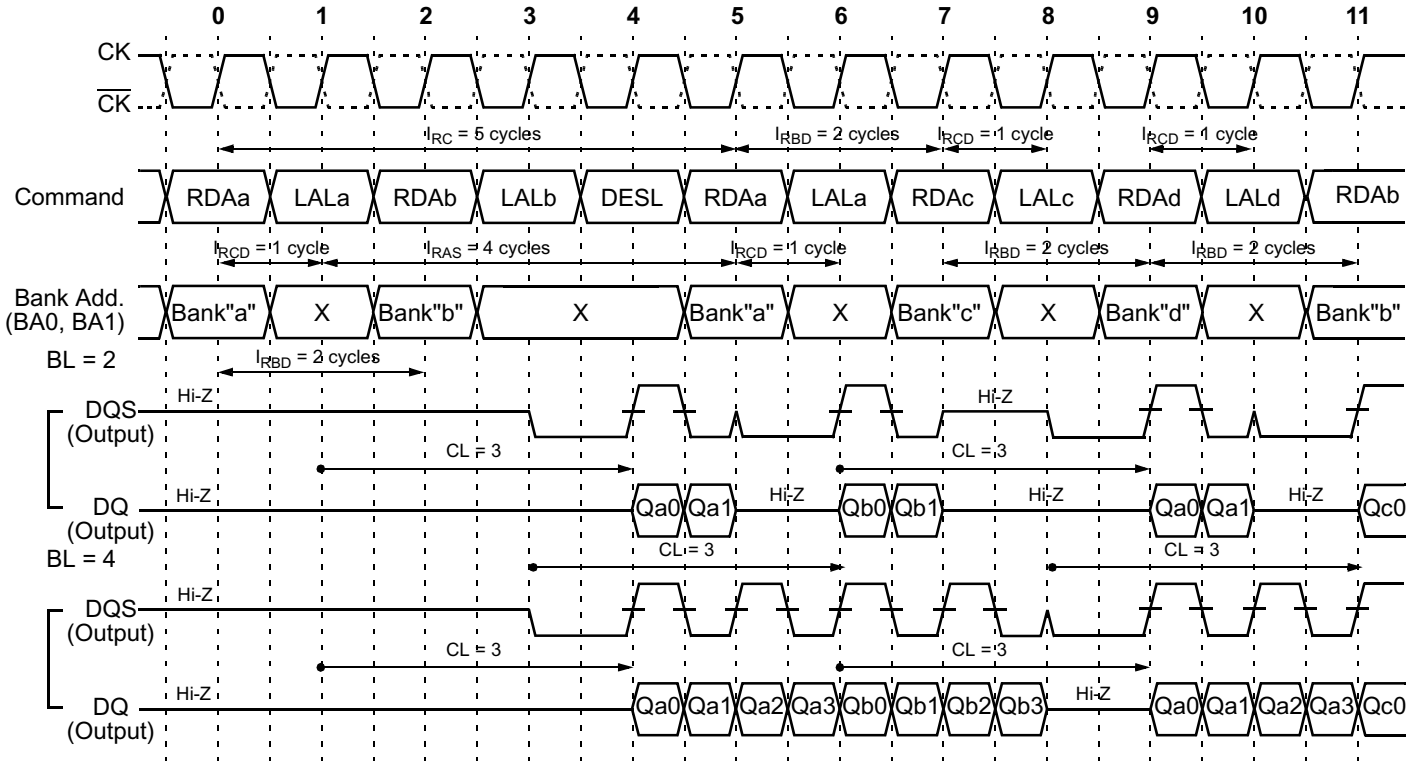
Single Bank Read-Write Timing (CL = 3)



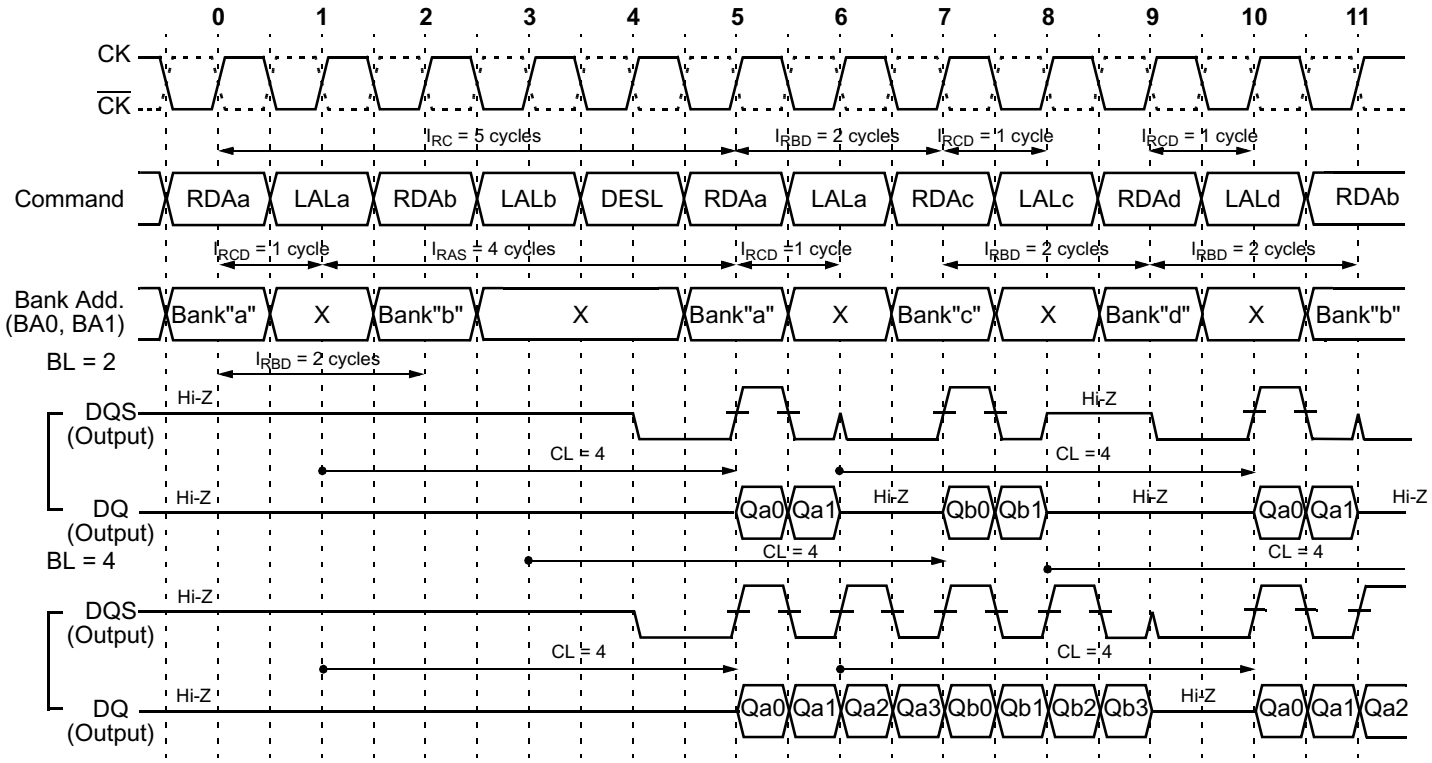
Single Bank Read-Write Timing (CL = 4)



Multiple Bank Read Timing (CL = 3)

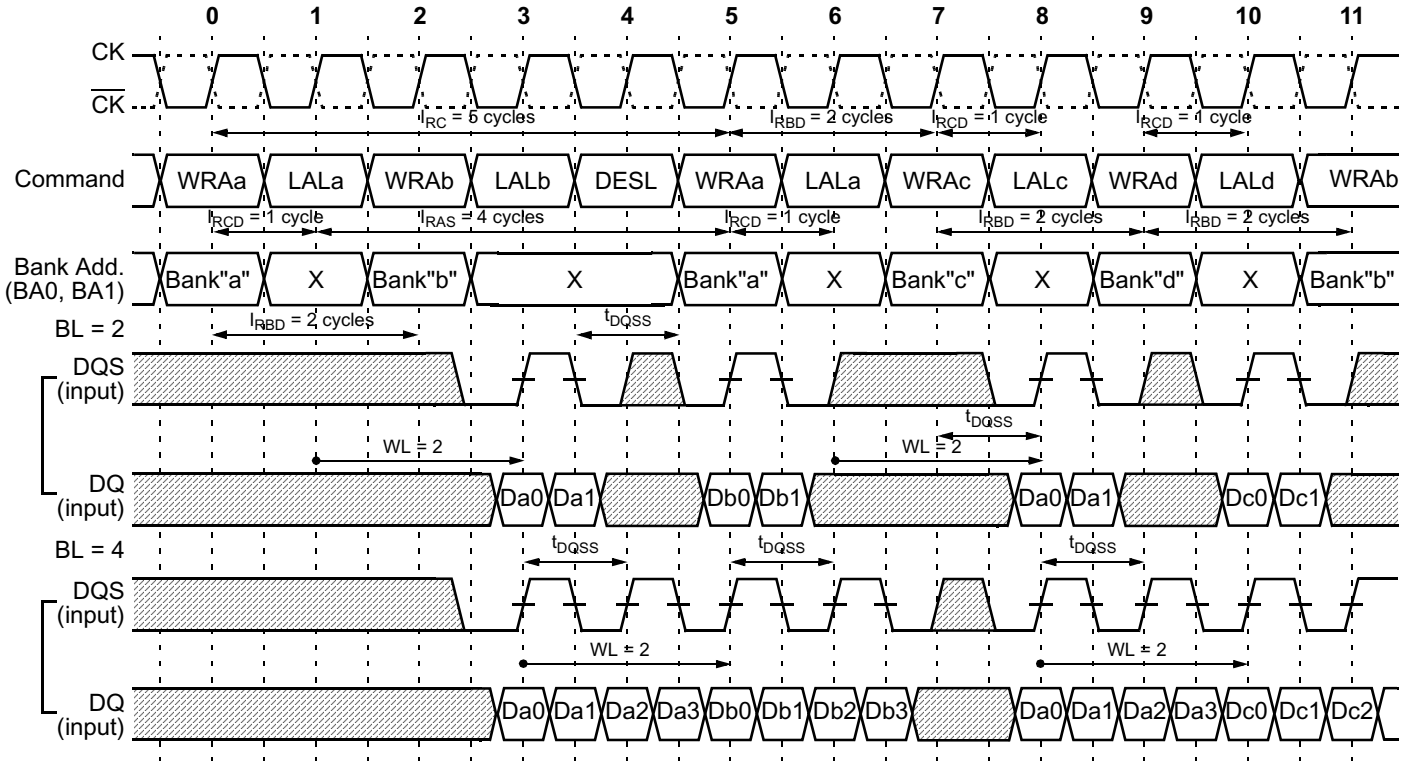


Multiple Bank Read Timing (CL = 4)

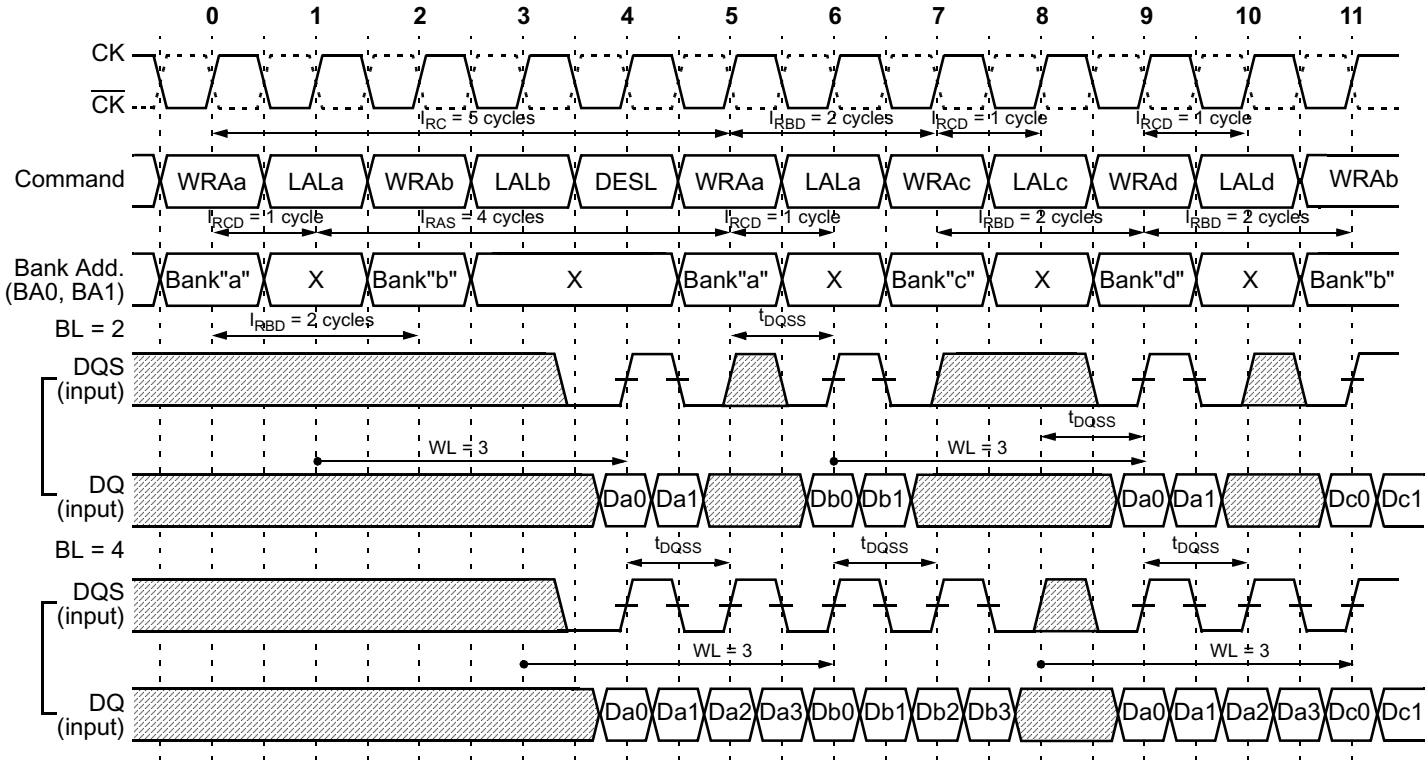


Note : "X" is don't care. I_{RC} to the same bank must be satisfied.

Multiple Bank Write Timing (CL = 3)

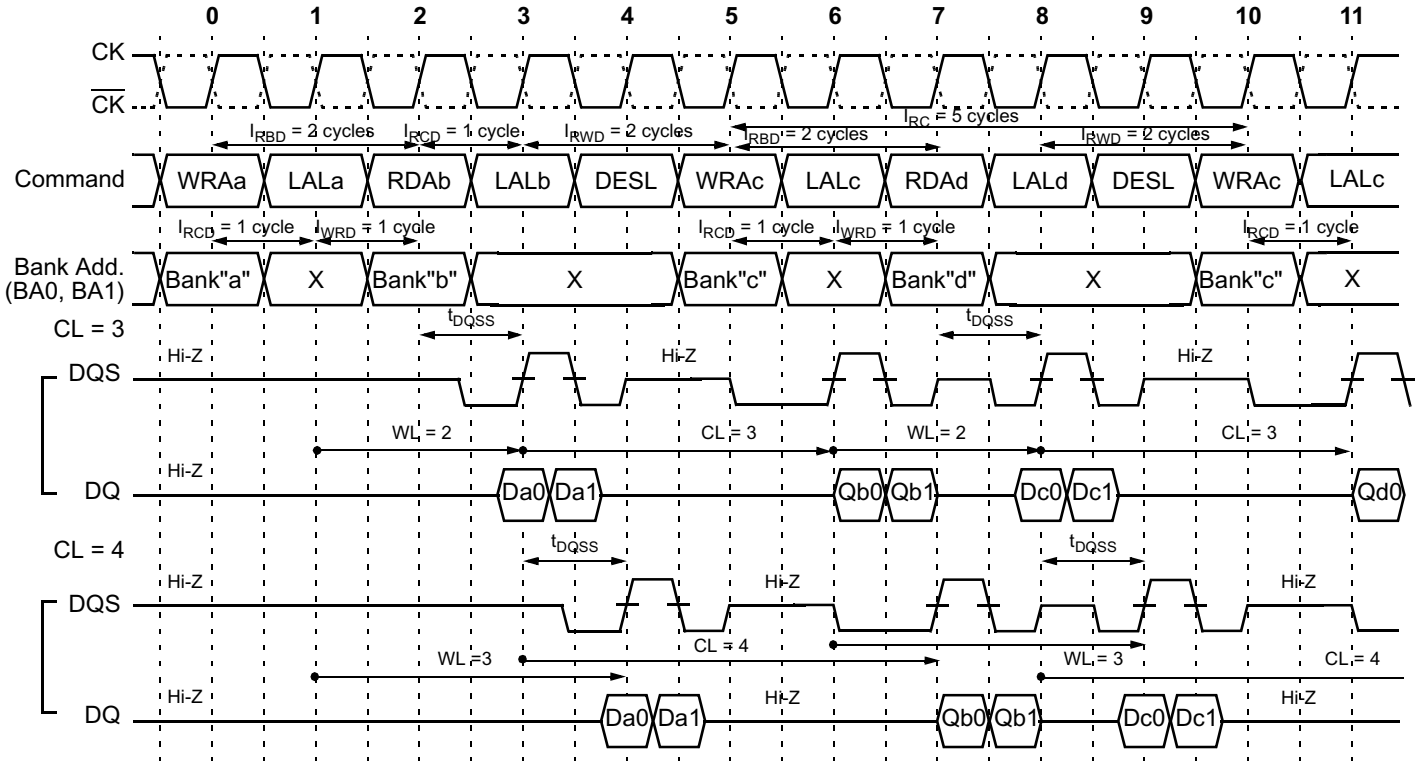


Multiple Bank Write Timing (CL = 4)

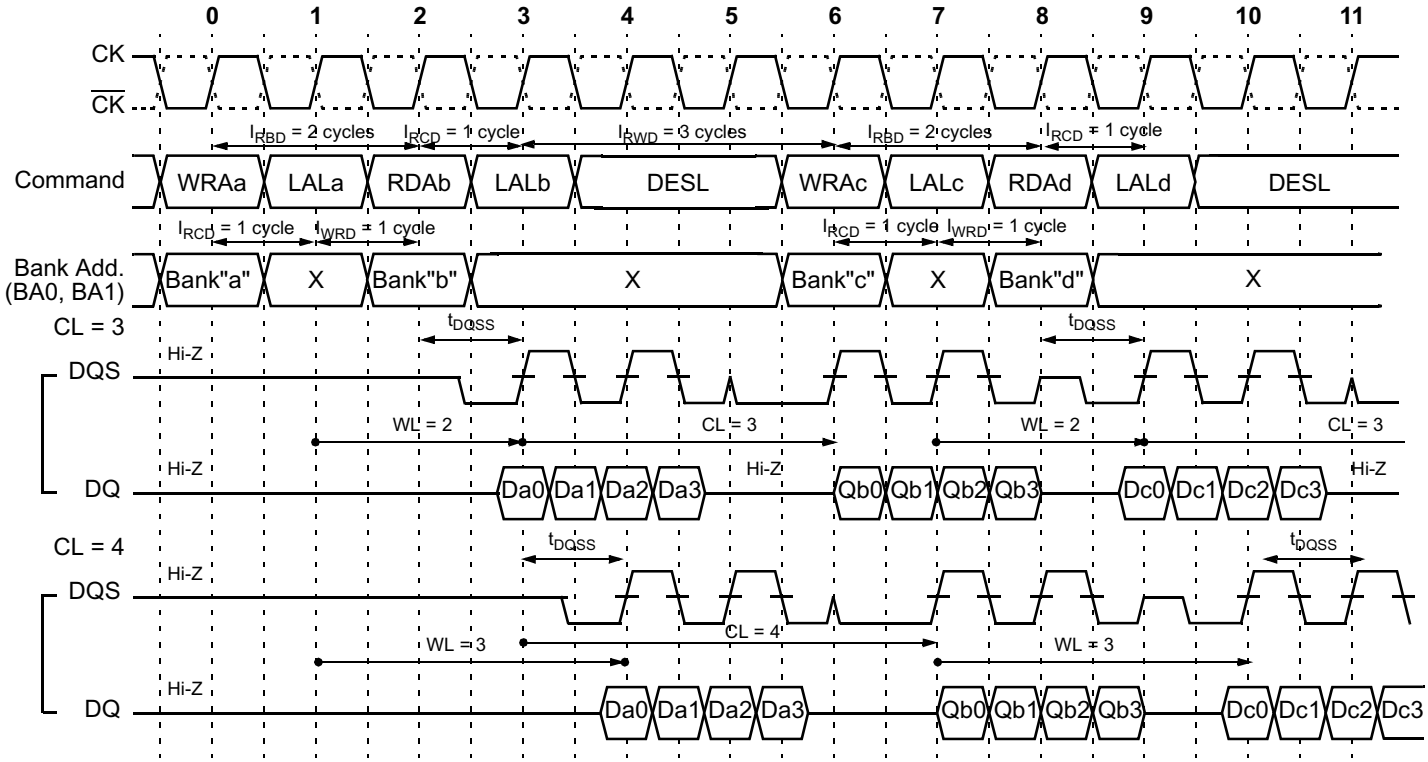


Note : means "H" or "L" "X" is don't care I_{RC} to the same bank must be satisfied.

Multiple Bank Read-Write Timing (BL = 2)

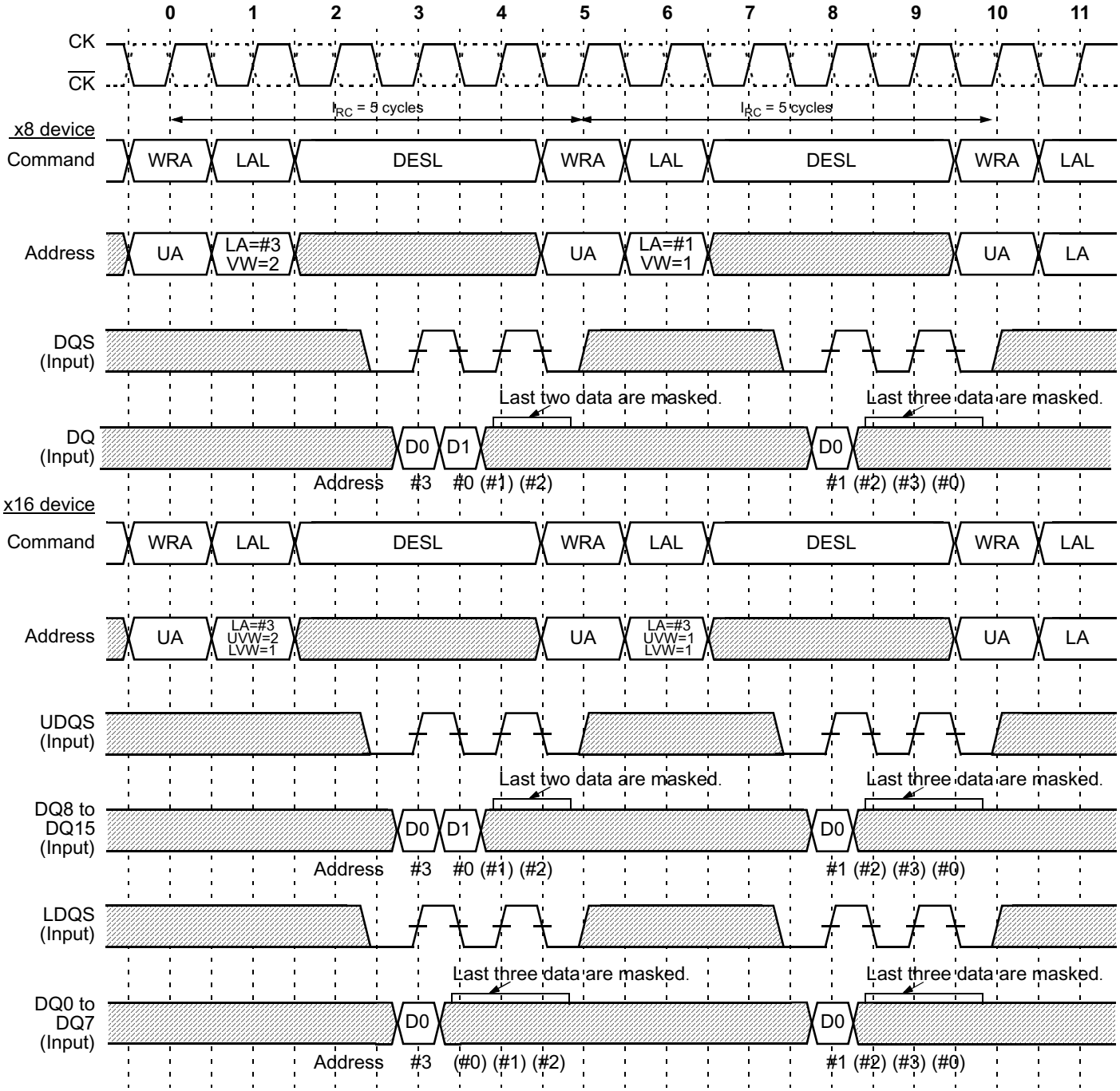


Multiple Bank Read-Write Timing (BL = 4)



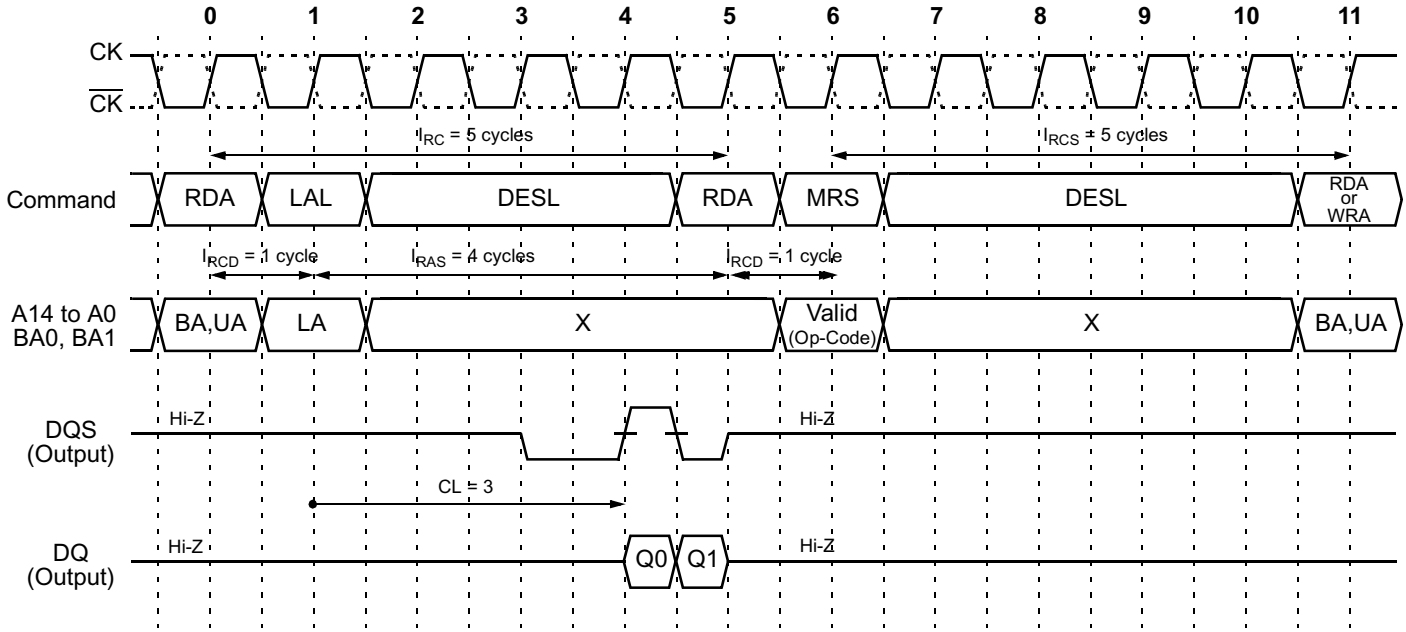
Note : "X" is dont care
I_{RC} to the same bank must be satisfied.

Single Bank Write with VW (CL=3, BL=4, Sequential mode)

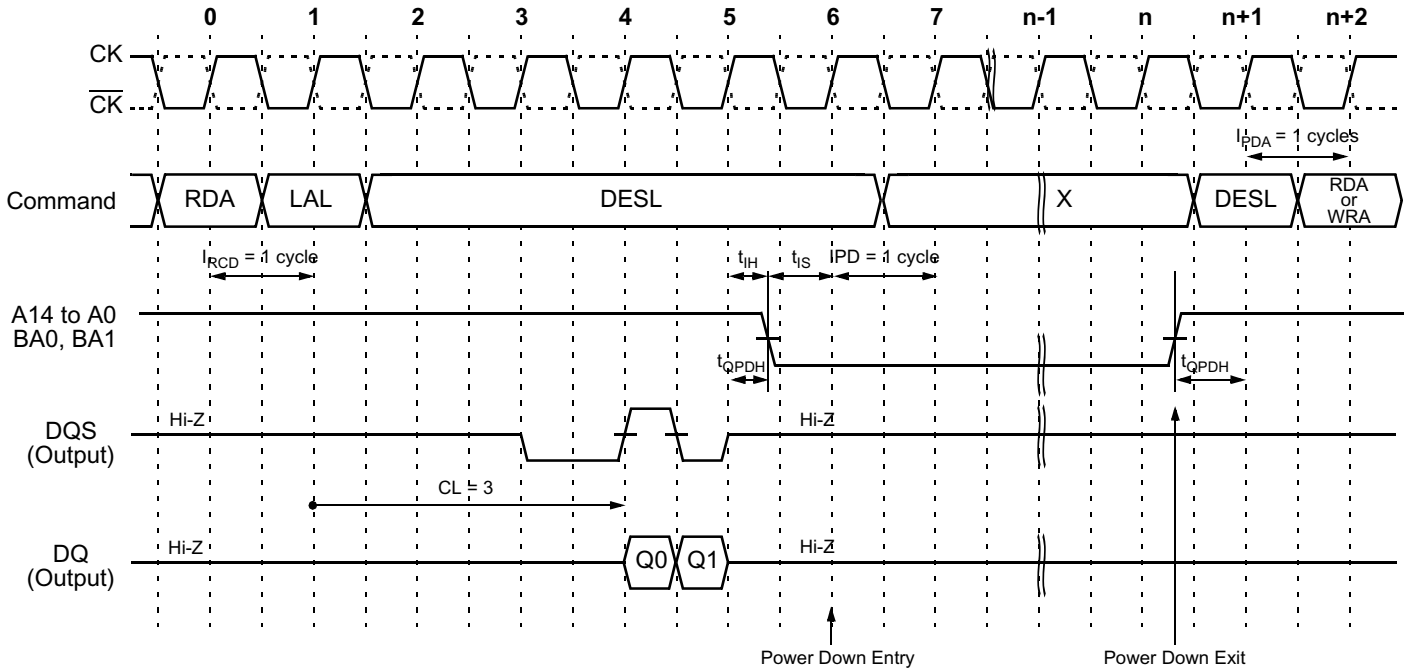


Notes : DQS input must be continued till end of burst count even if some of laster data is masked.

Mode Register Set Timing (CL=3, BL=2)



Power Down Timing (CL=3, BL=2)



Note : "x" is don't care.

IPD is defined from the first clock rising edge after $\overline{PD}$ is brought to "Low".

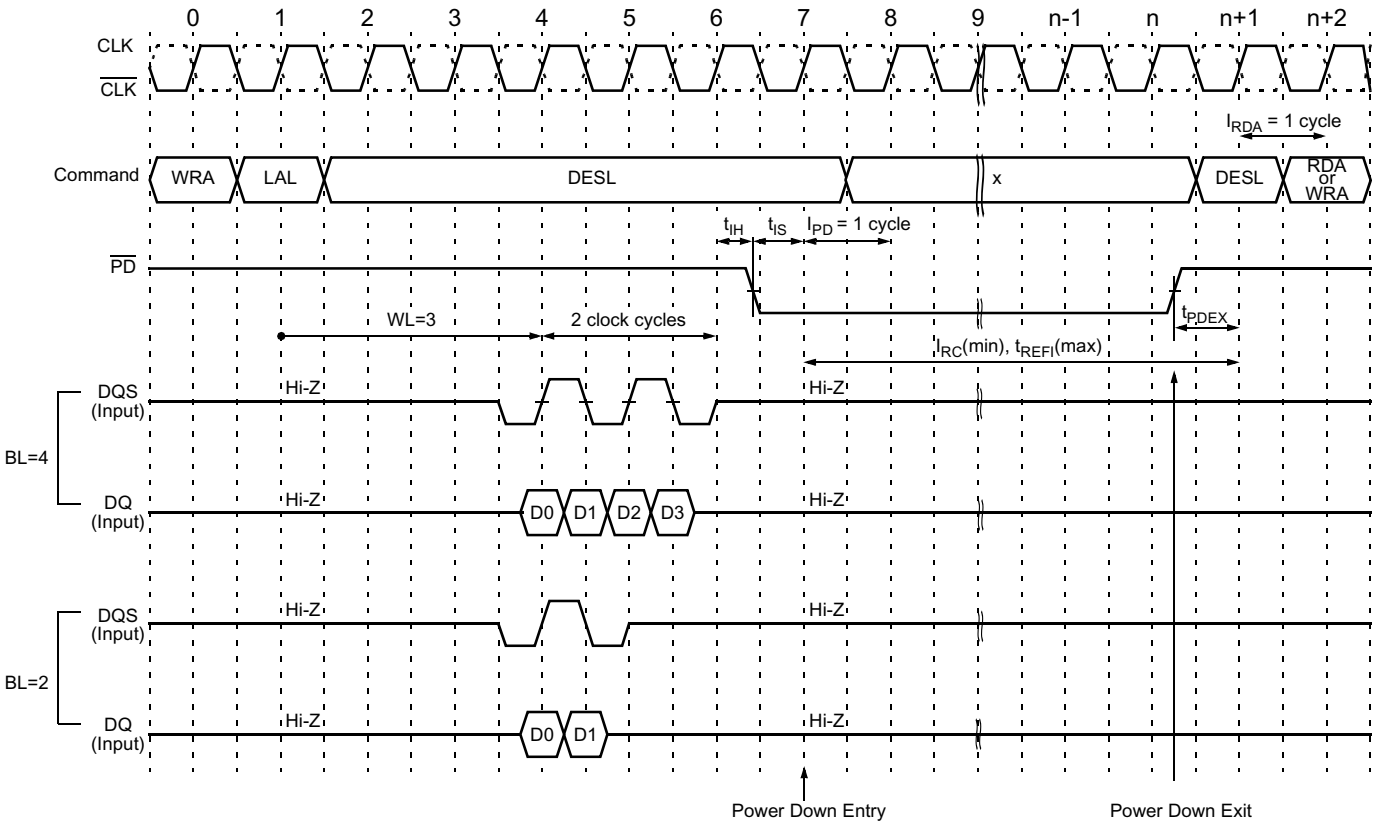
IPDA is defined from the first clock rising edge after $\overline{PD}$ is brought to "High".

$\overline{PD}$ must be kept "High" level until end of Burst data output.

$\overline{PD}$ should be brought to high within $t_{REFI(max)}$ to maintain the data written into cell.

Power Down Timing (CL=4)

Write cycle to Power Down Mode

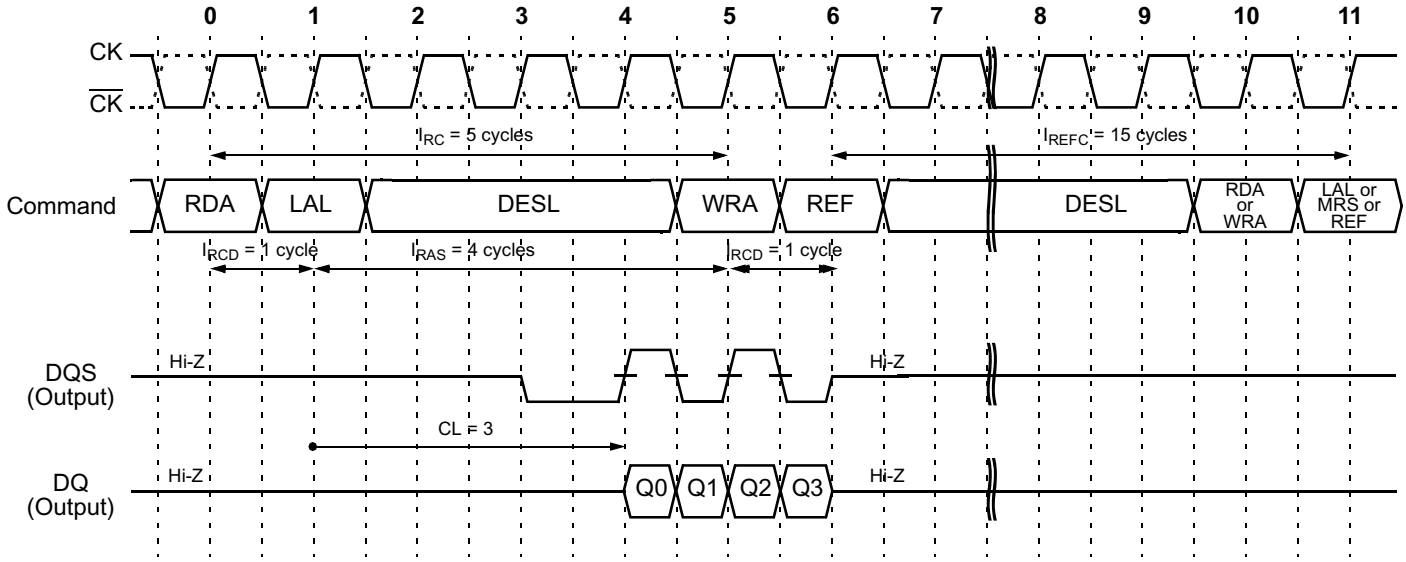


Note : "x" is don't care.

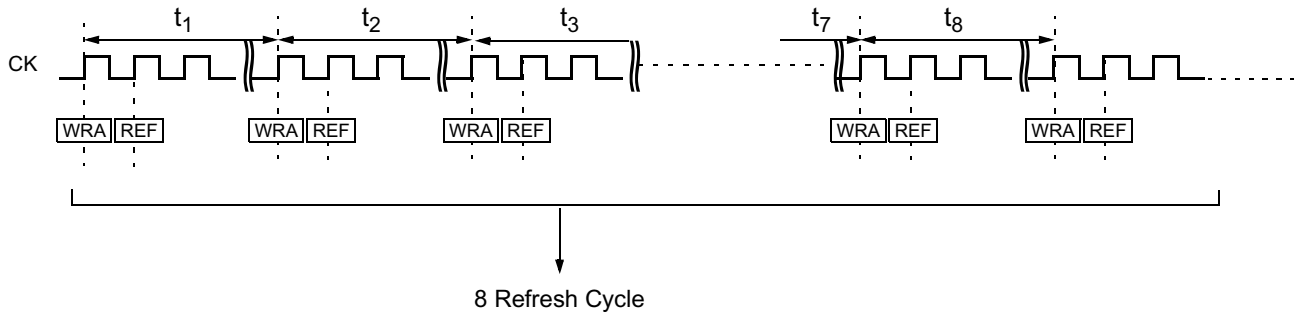
$\overline{PD}$ must be kept "High" level until WL+2 clock cycles from LAL command.

$\overline{PD}$ should be brought to high within $t_{REFI(max)}$ to maintain the data written into cell.

Auto-Refresh Timing (CL=3, BL=4)



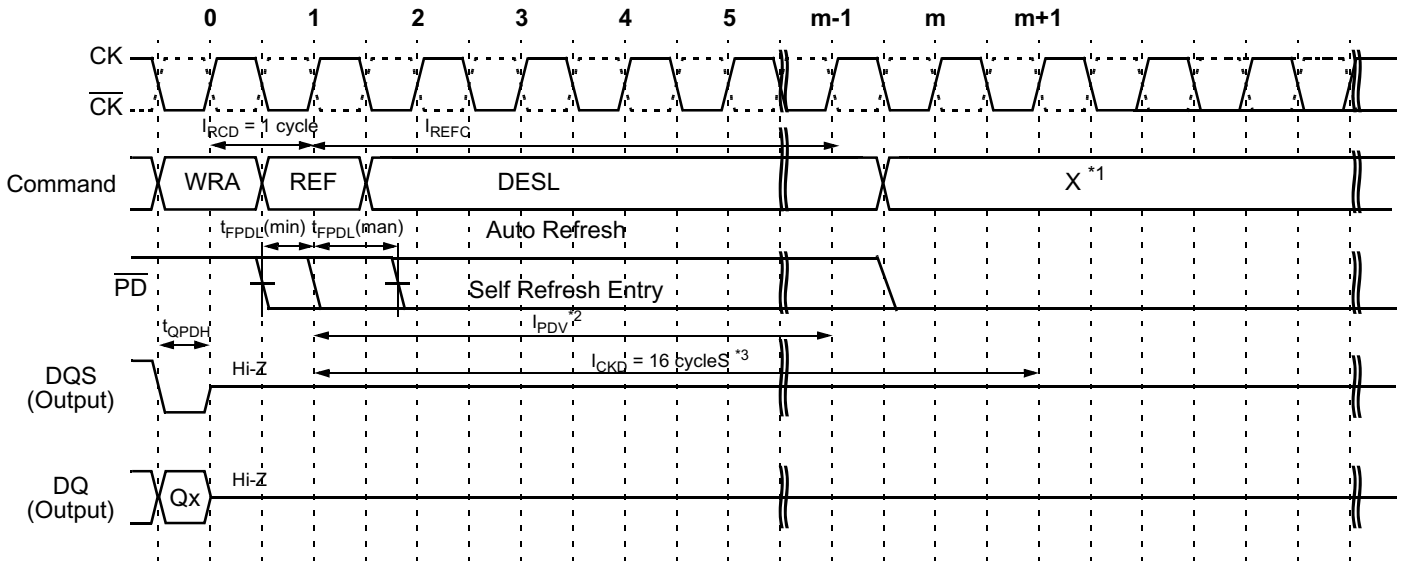
Note : In case of CL=3, I_{REFC} must be meet 15 clock cycles. When the Auto-Refresh operation is performed, the synthetic average interval of Auto-Refresh command specified by t_{REFI} must be satisfied. t_{REFI} is average Interval time in 8 Refresh cycles that is sampled randomly.



$$t_{REFI} = \frac{\text{Total time of 8 Refresh cycle}}{8} = \frac{t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8}{8}$$

t_{REFI} is specified to avoid partly concentrated current of Refresh operation that is activated larger area than Read/Write operation.

Self-Refresh Entry Timing

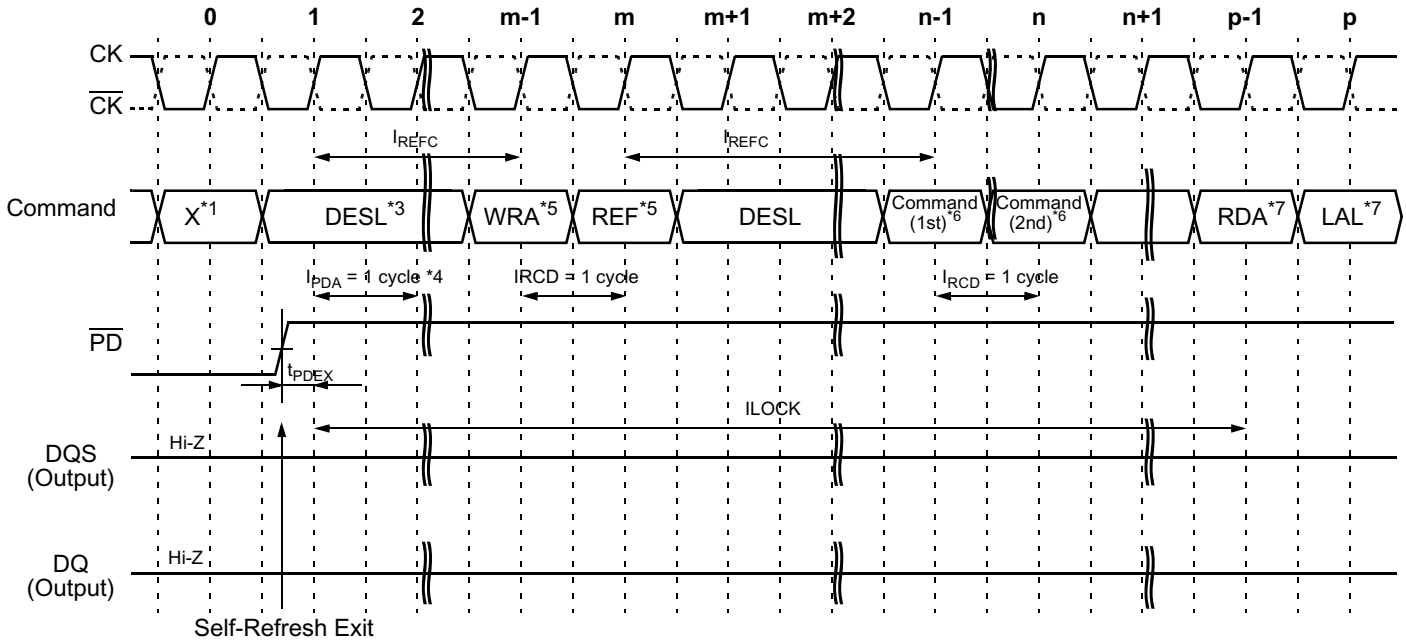


Note : 1. "X" is don't care.

2. $\overline{PD}$ msut be brought to "Low" within the timing between t_{FPDL}(min) and t_{FPDL}(max) to Self Refresh mode When $\overline{PD}$ is brought to "Low" after I_{PDV}, Network-DRAM perform Auto Refresh and enter Power down mode.

3. It is desirable that clock input is continued at least 16 clock cycles from REF command even though $\overline{PD}$ is brought to "Low" for Self-Refresh Entry.

Self-Refresh Exit Timing



Note : 1. "X" is don't care.,

2. Clock should be stable prior to $\overline{PD}$ = "High" if clock input is suspended in Self-Refresh mode.
3. DESL command must be asserted during I_{REFC} after $\overline{PD}$ is brought to "High".
4. IPDA is defined from the first clock rising edge after $\overline{PD}$ is brought to "High".
5. It is desirable that one Auto-Refresh command is issued just after Self-Refresh Exit before any other operation.
6. Any command (except Read command) can be issued after I_{REFC}.
7. Read command (RDA+LAL) can be issued after ILOCK.

Function Description

Network-DRAM

The Network-DRAM is Double Data Rate (DDR) operating. The Network-DRAM is competent to perform fast random core access, low latency, low consumption and high-speed data bandwidth.

Pin Functions

Clock Inputs : CK & $\overline{CK}$

The CK and $\overline{CK}$ inputs are used as the reference for synchronus operation. CK is master clock input. The $\overline{CS}$, FN and all address input signals are sampled on the crossing of the positive edge of $\overline{CK}$ and the negative edge of CK. The DQS and DQ and DQ output data are referenced to the crossing point of CK and $\overline{CK}$. The timing reference point for the differential clock is when the CK and $\overline{CK}$ signals cross during a transition.

Power Down : PD

The $\overline{PD}$ input controls the entry to the Power Down or Self-Refresh modes. The $\overline{PD}$ input does not have a Clock Suspend function like a CKE input of a standard SDRAMs, therefore it is illegal to bring PD pin into low state if any Read or Write operation is being performed.

Chip Select & Function Control : $\overline{CS}$ & FN

The $\overline{CS}$ and FN inputs are a control aignal for forming the operation commands on Network-DRAM. Each operation mode is decided by the combination of the two consecutive operation commands using the $\overline{CS}$ and FN inputs.

Bank Addresses : BA0 & BA1

The BA0 and BA1 inputs are latched at the time of assertion of the RDA or WRA command and are selected the bank to be used for the operation.

	BA0	BA1
Bank #0	0	0
Bank #1	1	0
Bank #2	0	1
Bank #3	1	1

Functional Description (Continued)

Address Inputs : A0 to A14

Address inputs are used to access the arbitrary address of the memory cell array within each bank. The Upper Addresses with Bank address are latched at the RDA or WRA command and the Lower Addresses are latched at the LAL command. The A0 to A14 inputs are also used for setting the data in the Regular or Extended Mode Register set cycle.

	Upper Address	Lower Address
K4C560838C-TC	A0 to A14	A0 to A7
K4C561638C-TC	A0 to A14	A0 to A6

Data Input/Output : DQ0 to DQ7 or DQ15

The input data of DQ0 to DQ15 are taken in synchronizing with the both edges of DQS input signal.
The output data of DQ0 to DQ15 are outputted synchronizing with the both edges of DQS output signal.

Data Strobe : DQS or LDQS, UDQS

The DQS is bi-directional signal. Both edges of DQS are used as the reference of data input or output. The LDQS is allotted for Lower Byte (DQ0 to DQ7) Data. The UDQS is allotted for Upper Byte(DQ8 to DQ15) Data. In write operation, the DQS used as an input signal is utilized for a latch of write data. In read operation, the DQS that is an output signal provides the read data strobe.

Power Supply : Vdd, VddQ, Vss, VssQ

Vdd and Vss are supply pins for memory core and peripheral circuits.
VddQ and VssQ are power supply pins for the output buffer.

Reference Voltage : VREF

V_{REF} is reference voltage for all input signals.

Functional Description (Continued)

Command Functions and Operations

K4C5608/1638C-TC are introduced the two consccutive command input method. Therefore, except for Power Down mode, each operation mode decided by the combination of the first command and the second command from stand-by states of the bank to be accessed.

Read Operation (1st command + 2nd command = RDA + LAL)

Issuing the RDA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a read mode. When the LAL command with Lower Addresses is issued at the next clock of the RDA command, the data is read out sequentially synchroniaing with the both edges of DQS output signal (Burst Read Operation). The initial valid read data appears after CAS latency, the burst length of read data and the burst type must be set in the Mode Register beforehand. The read operated bank goes back automatically to the idle state after I_{RC}.

Write Operation (1st command + 2nd command = WRA + LAL)

Issuing the WRA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a write mode. When the LAL command with Lower Addresses is issued at the next clock of the WRA command, the input data is latched sequentially synchronizing with the both edges of DQS input signal (Burst Write Operation). The data and DQS inputs have to be asserted in keeping with clock input after CAS latency-1 from the issuing of the LAL command. The write data length is set by the VW in the LAL command. The DQS have to be provided for a burst length. The CAS latency and the burst type must be set in the Mode Register beforehand. The write operated bank goes back automatically to the idle state after I_{RC}.

Auto-Refresh Operation (1st command + 2nd command = WRA + REF)

K4C560838/1638C-TC are required to refresh like a standard SDRAM. The Auto-Refresh operation is begun with the REF command following to the WRA command. The Auto-Refresh mode can be effective only when all banks are in the idle state and all outputs are in Hi-z states. In a point to notice, the write mode started with the WRA command is canceled by the REF command having gone into the next clock of the WRA command instead of the LAL command. The minimum period between the Auto-Refresh command and the next command is specified by I_{REFC}. However, about a synthetic average interval of Auto-Refresh command, it must be careful. In case of equally distributed refresh, Auto-Refresh command has to be issued within once for every 7.8us by the maximum In case of burst refresh or random distributed refresh, the average interval of eight consecutive Auto-Refresh command has to be more than 400ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2us (8x400ns) is to 8 times in the maximum.

Self-Refresh Operation (1st command + 2nd command = WRA + REF with $\overline{PD}$="L")

It is the function of Self-Refresh operation that refresh operation can be performed automatically by using an internal timer. When all banks are in the idle state and all outputs are in Hi-z states, the K4C560838/1638C-TC become Self-Refresh mode by issuing the Self-Refresh command. $\overline{PD}$ has to be brought to "Low" within t_{FPDL} from the REF command following to the WRA command for a Self-Refresh mode entry. In order to satisfy the refresh period, the Self-Refresh entry command should be asserted within 7.8us after the latest Auto-Refresh command. Once the device enters Self-Refresh mode, the DESL command must be continued for I_{REFC} period. In addition, it is desirable that clock input is kept in I_{CKD} period. The device is in Self-Refresh mode as long as $\overline{PD}$ held "Low". During Self-Refresh mode, all input and output buffers except for $\overline{PD}$ are disabled, therefore the power dissipation lowers. Regarding a Self-Refresh mode exit, $\overline{PD}$ has to be changed over from "Low" to "High" along with the DESL command, and the DESL command has to be continuously issued in the number of clocks specified by I_{REFC}. The Self-Refresh exit function is asynchronous operation. It is required that one Auto-Refresh command is issued to avoid the violence of the refresh period just after I_{REFC} from Self-Refresh exit.

Power Down Mode($\overline{PD}$="L")

When all banks are in the idle state and all outputs are in Hi-Z states, the K4C560838/1638C-TC become Power Down Mode by asserting $\overline{PD}$ is "Low". When the device enters the Power Down Mode, all input and output buffers except for $\overline{PD}$ are disabled after specified time. Therefore, the power dissipation lowers. To exit the Power Down Mode, $\overline{PD}$ has to be brought to "High" and the DESL command has to be issued at next CK rising edge after $\overline{PD}$ goes high. The Power Down exit function is asynchronous operation.

Mode Register Set (1st command + 2nd command = RDA + MRS)

When all banks are in the idle state, issuing the MRS command following to the RDA command can program the Mode Register. In a point to notice, the read mode started with the RDA command is canceled by the MRS command having gone into the next clock of the RDA command instead of the LAL command. The data to be set in the Mode Register is transferred using A0 to A14, BA0 and BA1 address inputs. The K4C560838/1638C-TC have two mode registers. These are Regule and Extended Mode Register. The Regular or Extended Mode Register is chosen by BA0 in the MRS command.The Regular Mode Register designates the operation mode for a read or write cycle. The Regular Mode Register has four function fields.

The four fields are as follows :
(R-1) Burst Length field to set the length of burst data
(R-2) Burst Type field to designate the lower address access sequence in a burst cycle
(R-3) $\overline{CAS}$ Latency field to set the access time in clock cycle
(R-4) Test Mode field to use for supplier only.

The Extended Mode Register has two function fields.
The two fields are as follows:
(E-1) DLL Switch field to choose either DLL enable or DLL disable
(E-2) Output Driver Impedance Control field.

Once these fields in the Mode Register are set up, the register contents are maintained until the Mode Register is set up again by another MRS command or power supply is lost. The initial value of the Regular or Extended Mode Register after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

Functional Description (Continued)

• Regular Mode Register/Extended Mode Register change bits (BA0, BA1)

These bits are used to choose either Regular MRS or Extended MRS

BA1	BA0	A14 - A0
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	X	Reserved

Regular Mode Register Fields

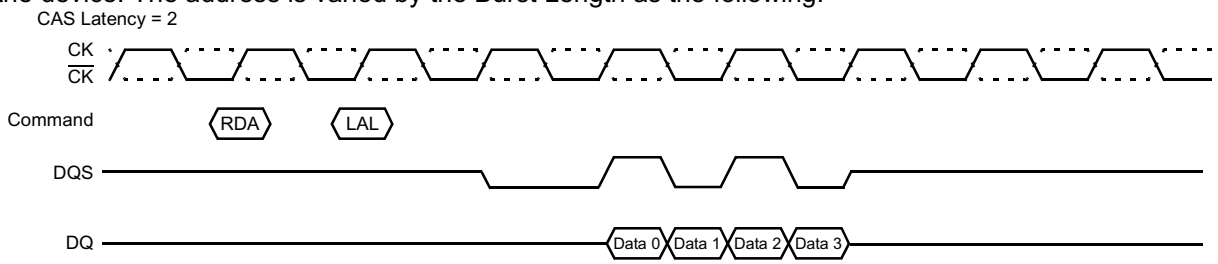
(R-1) Burst Length field (A2 to A0)
This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2 or 4 words.

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	Reserved
1	X	X	Reserved

(R-2) Burst Type field (A3)
This Burst Type can be chosen Interleave mode or Sequential mode. When the A3 bit is " 0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both burst types support burst length of 2 and 4 words.

A3	Burst Type
0	Sequential
1	Interleave

• Addressing sequence of Sequential mode (A3)
A column access is started from the inputted lower address and is performed by incrementing the lower address input to the device. The address is varied by the Burst Length as the following.



Addressing sequence for Sequential mode

Data	Access Address	Burst Length
Data 0	n	2 words (Address bits is LA0) not carried from LA0 to LA1
Data 1	n + 1	
Data 2	n + 2	4 words(Address bits is LA1, LA0) not carried from LA0 to LA1
Data 3	n + 3	

Functional Description (Continued)

• Addressing sequence of Inteleave mode
A column access is started from the inputted lower address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

Data	Access Address	Burst Length
Data 0	...A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	...A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	...A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	...A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	

(R-3) $\overline{CAS}$ Latency field (A6 to A4)
This field specifies the number of clock cycles from the assertion of the LAL command following the RDA command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CK. In a write mode, the place of clock which should input write data is $\overline{CAS}$ Latency cycles - 1.

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

(R-4) Test Mode field (A7)
This bit is used to enter Test Mode for supplier only and must be set to "0" for normal operation.

(R-5) Reserved field in the Regular Mode Register
• Reserved bits (A8 to A14)
These bits are reserved for future operations. They must be set to "0" for normal operation.

Functional Description (Continued)

Extended Mode Register Fields

(E-1) DLL Switch field (A0)
This bit is used to enable DLL. When the A0 bit is set "0", DLL is enabled.
(E-2) Output Driver Impedance Control field (A1/A0)
This field is used to choose Output Driver Strength. Four types of Driver Strength are supported.

A6	A1	Output Driver Impedance Control
0	0	Normal Output Driver
0	1	Strong Output Driver
1	0	Weaker Output Driver
1	1	Weakest Output Driver

(E-3) Reserved field (A2 to A5, A7 to A14)
These bits are reserved for future operations and must be set to "0" for normal operation.