Product Flyer

MB86670

KeyWave™ ADSL Transceiver/Controller

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The **KeyWave™** ADSL Transceiver/Controller, from Fujitsu, is the key component for Asymetrical Digital Subscriber Line (ADSL) modems supporting Discrete Multi Tone (DMT) modulation.

This highly integrated device supports Category II ADSL functionality as defined by ANSI T1.413, including trellis encoding and echo cancellation, with bit rates programmable up to 1 Mbps upstream and 8 Mbps downstream. The device includes a hardware DMT modulator/demodulator with digital signal processor (DSP) support, framer and user interfaces, high resolution A/D and D/A convertors and active filtering, which significantly reduces the requirement for external components.

KeyWave™ is ideal for cost sensitive Customer Premises Equipment and power sensitive Central Office equipment.

PLASTIC PACKAGE
HQFP240

Features

- Supports ANSI T1.413 Issue 2 and ETSI 328 DMT ADSL
- Programmable for future ADSL derivatives (e.g. G.Lite, UADSL)
- Configurable as Central Office (ATU-C) or Remote (ATU-R) ADSL Termination Unit
- Integrated 15-bit resolution A/D and D/A convertors and active filtering
- Low noise Receive path summing amplifier (2.5 nV/ Hz typical)
- Analogue and digital echo cancellation
- Six configurable serial data interfaces
- UTOPIA data interface, Level 2 PHY layer or Level 1 ATM layer
- Supports Rate Adaptation (programmable N x 32 kbps channel allocation)
- Compatible with POTS and ISDN
- Low power operation (< 2 Watts typical)
- General purpose microprocessor interface
- 3.3V CMOS device

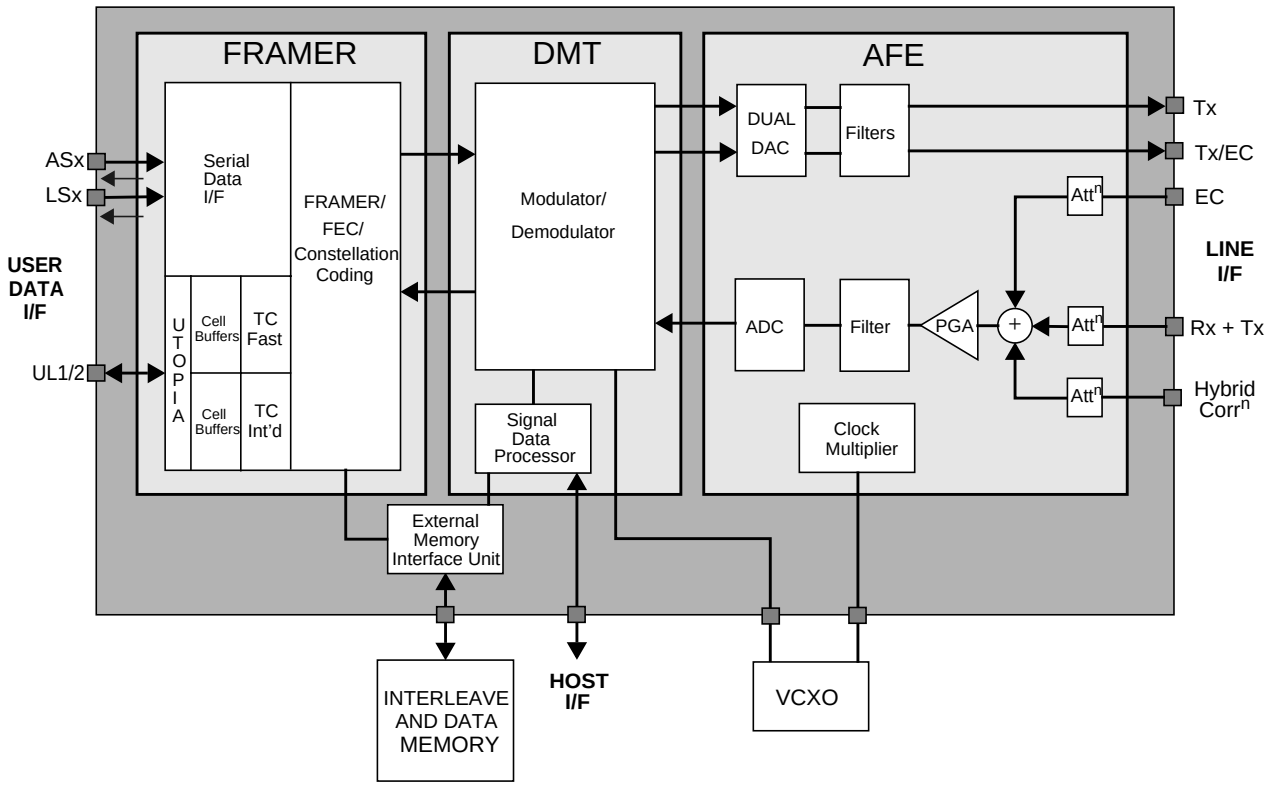

Figure 1 KeyWave™ Logical Block Diagram

General

A logical block diagram of **KeyWave™**, ADSL Transceiver/Controller, is shown in figure 1. Internally, the device consists of an Analogue Front End block, a DMT modulator/demodulator block, and a Framer block. The main interfaces are the User Data Interfaces, the Host Interface, the Local Memory Interface, and the Line Interface.

This device incorporates multiple high resolution A/D and D/A convertors with active filters and gain stages required for the line interface. Echo cancellation is implemented in both the analogue and digital domains. An integrated digital signal processor (DSP) is used to support the dedicated DMT hardware. An external host processor provides modem control and is supplied with software for this purpose. The device requires a single 17.664 MHz clock source which may be an external reference, or a VCXO which can be locked to the line symbol rate.

Analogue Front End (AFE)

The analogue circuitry consists of two 15-bit DACs with associated anti-imaging filters, a 15-bit ADC with anti-aliasing filter, and a programmable gain summing amplifier. The dual DAC is configured for oversampling parallel operation for ATU-C use by summing the two Tx outputs, providing conversion at 8.832 MSps and, for ATU-R use, as separate Transmit and Echo Cancellation DACs, each running at 4.416 MSps. The anti-imaging filters are 4^{th} order with programmable cut-off frequency and a programmable gain stage providing an output for direct connection to an external line driver.

The Receiver front end has programmable attenuators on all inputs for handling all line lengths and maintaining sufficient dynamic range in the low noise summing amplifier. This amplifier has programmable gain and the 4^{th} order anti-aliasing filter has programmable cut-off frequency.

The ADC uses a proprietary error correcting successive approximation architecture (patent applied for), and provides samples at 8.832 MSps. All analogue signal paths are differential.

This highly integrated AFE reduces the components required for the line interface to a line driver and a small number of passives.

DMT Modulator/Demodulator

This block performs time domain and frequency domain digital processing as required for Discrete Multi Tone modulation and demodulation. Dedicated hardware is used for Fast Fourier Transforms, echo cancellation, interpolation/decimation, and adaptive equalisation. This block includes a Digital Signal Processor which assists the dedicated processing modules. Sufficient processing capacity is provided to handle 256 downstream tones and 64 upstream tones, as required for operation over ISDN.

Framer/FEC/Constellation coding

This block consists of the User Data Interface, Framer, Forward Error Corrector (FEC) and constellation encoder/decoder.

The Framer multiplexes/demultiplexes the serial data supplied from the user data interface into frames, generates/checks Reed-Solomon FEC bytes, performs the interleaving function and encodes/decodes the frames to produce constellation data for the DMT modulator.

The User Data Interface allows data to be provided in ATM cells or as a number of serial data streams. The framer is configurable for assignment to fast and interleaved paths. The interleaving operation requires access to external RAM which is managed by the external memory interface unit. The constellation encoding may optionally use Trellis coding to improve the data rate capacity of the system.

External Memory Interface Unit

This block provides the interfaces to external Static RAM for use by the interleaver and for DSP data storage.

Host Interface

The Host microprocessor is required for control and monitoring of the device. Software is supplied for this purpose which implements an Applications Programming Interface to allow host user code to provide high level control of the modem. The program code required by the DSP is supplied in binary form and is downloaded from host memory to internal program RAM by the modem control software. The modem control software handles the ADSL overhead channel, whilst the embedded operations channel data is made available to the host user code across the API.

User Data Interfaces

For ATM mode operation, the data interfaces are configurable to offer either a UTOPIA Level 2 PHY layer or a UTOPIA Level 1 ATM Layer interface. This block performs the Transmission Convergence function for Fast and Interleaved channels in this mode, the channels being selected as separate PHY ports on the UTOPIA interface. Cell buffering is provided for cell transfer across the clock domains.

For Packet or STM mode operation, six serial data channels with associated clocks are provided which may be configured as any subset of the ANSI STM mode interface. The direction of the data is configurable, and a choice of data valid or byte sync indication is provided for each channel. A Network Timing Reference is made available across the ADSL link.

Applications

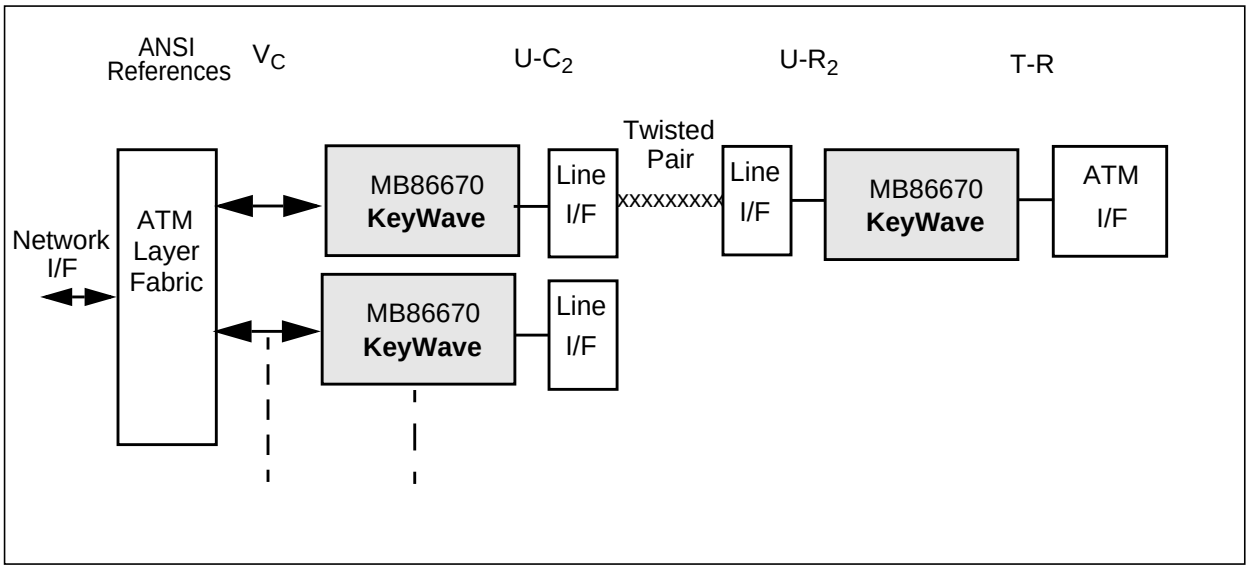

Figure 2 KeyWave™ used at either end of an ADSL system.

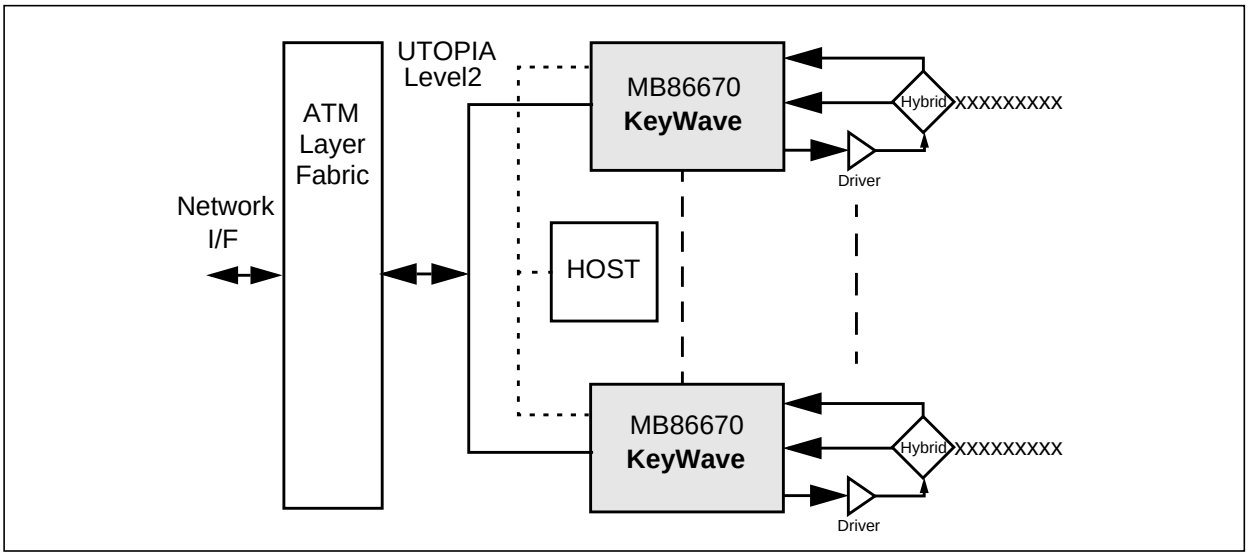

Figure 3 KeyWave™ used in an ATM based Central Office Service Access Multiplexer. In this configuration a local Host is shown managing multiple ADSL Transceiver/Controllers.

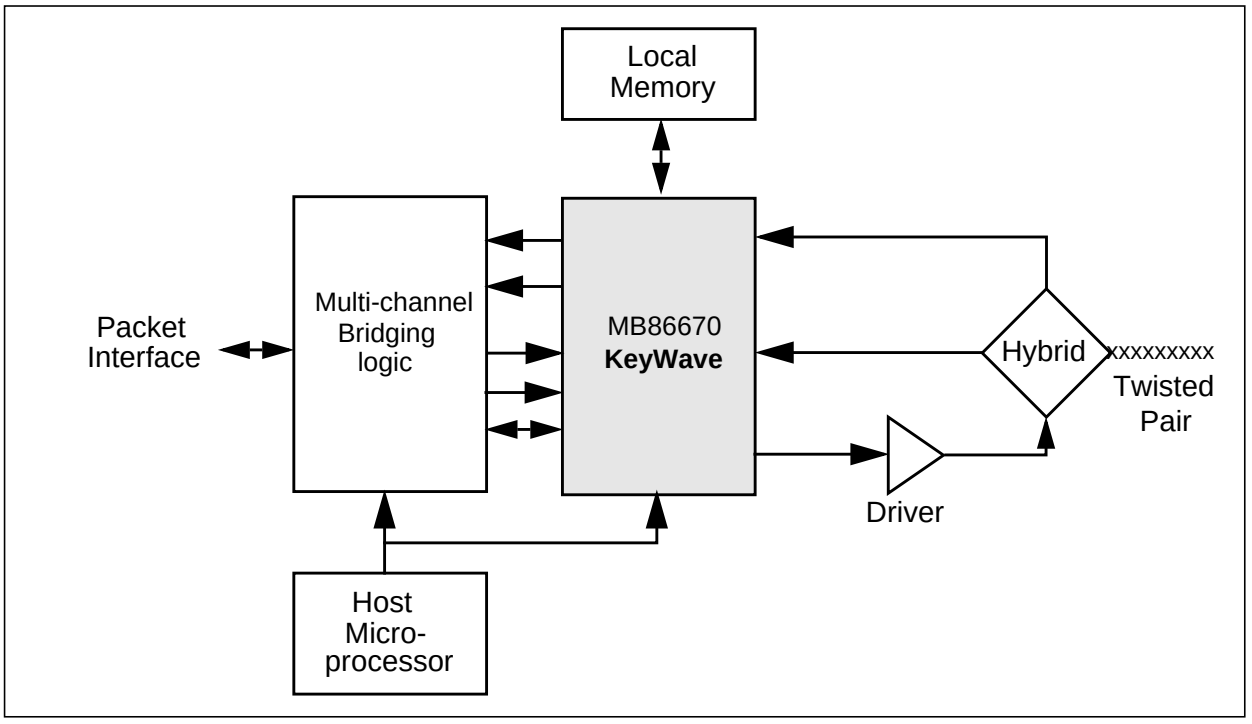

Figure 4 KeyWave™ used in a packet mode application.

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