
Document Title

256Kx36 & 256Kx32 & 512Kx18-Bit Synchronous Pipelined Burst SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	May. 18 . 2001	Preliminary
0.1	1. Delete pass- through	June. 26. 2001	
0.2	1. Add x32 org part and industrial temperature part	Aug. 11. 2001	

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

8Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
512Kx18	K7A801825B-Q(H)C(I)65/75/85	SB	3.3	6.5/7.5/8.5 ns	Q: 100TQFP H: 119BGA	C: Commercial Temperature Range I: Industrial Temperature Range
	K7A801800B-Q(H)C(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A801809B-Q(H)C(I)25/22/20	SPB(2E1D)	3.3	250/225/200 MHz		
	K7A801801B-QC(I)16/14	SPB(2E2D)	3.3	167/138 MHz		
	K7A801808B-QC(I)25/22/20	SPB(2E2D)	3.3	250/225/200 MHz		
256Kx32	K7A803225B-QC(I)65/75/85	SB	3.3	6.5/7.5/8.5 ns		
	K7A803200B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A803209B-QC(I)25/22/20	SPB(2E1D)	3.3	250/225/200 MHz		
	K7A803201B-QC(I)16/14	SPB(2E2D)	3.3	167/138 MHz		
	K7A803208B-QC(I)25/22/20	SPB(2E2D)	3.3	250/225/200 MHz		
256Kx36	K7A803625B-Q(H)C(I)65/75/85	SB	3.3	6.5/7.5/8.5 ns		
	K7A803600B-Q(H)C(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A803609B-Q(H)C(I)25/22/20	SPB(2E1D)	3.3	250/225/200 MHz		
	K7A803601B-QC(I)16/14	SPB(2E2D)	3.3	167/138 MHz		
	K7A803608B-QC(I)25/22/20	SPB(2E2D)	3.3	250/225/200 MHz		

256Kx36 & 256Kx32 & 512Kx18-bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package)
- Operating in commercial and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-16	-14	Unit
Cycle Time	tCYC	6.0	7.2	ns
Clock Access Time	tCD	3.5	3.8	ns
Output Enable Access Time	tOE	3.5	3.8	ns

GENERAL DESCRIPTION

The K7A803600B, K7A803200B and K7A801800B are 9,437,184-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 256K(512K) words of 36/32(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, $\overline{ZZ}$. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEX}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals. Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

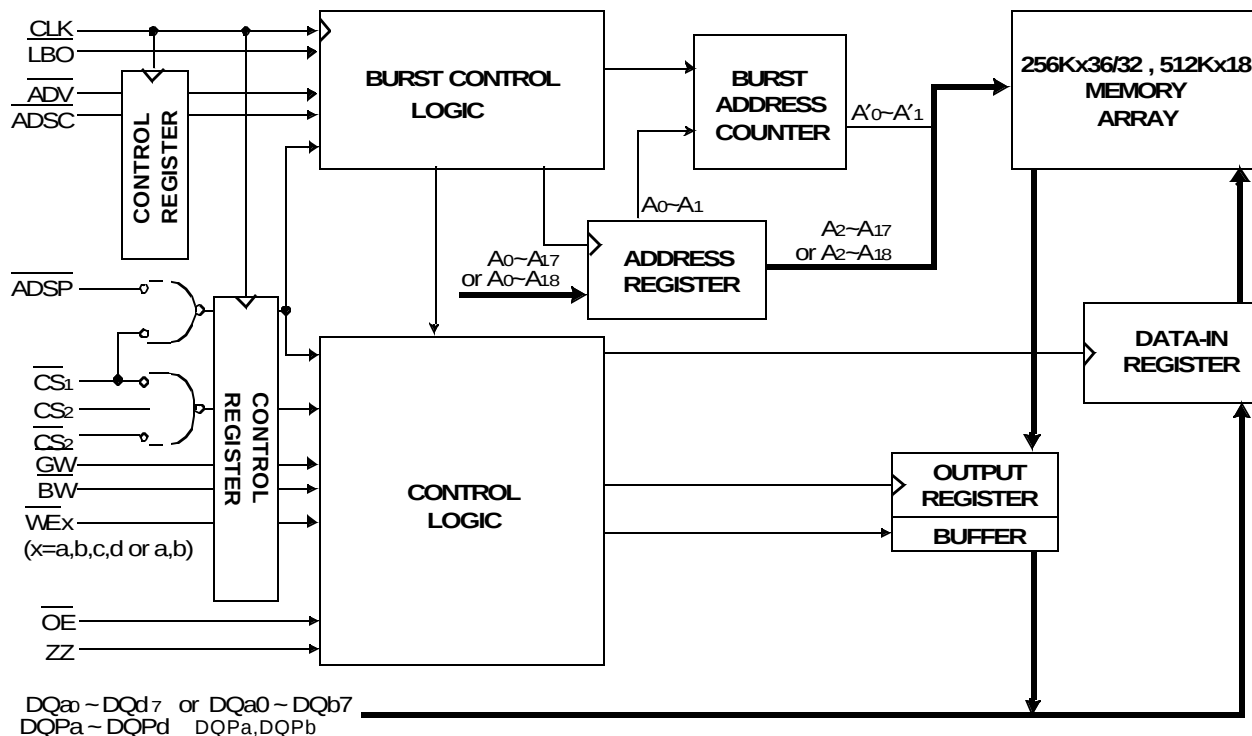
$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

$\overline{ZZ}$ pin controls Power Down State and reduces Stand-by current regardless of CLK.

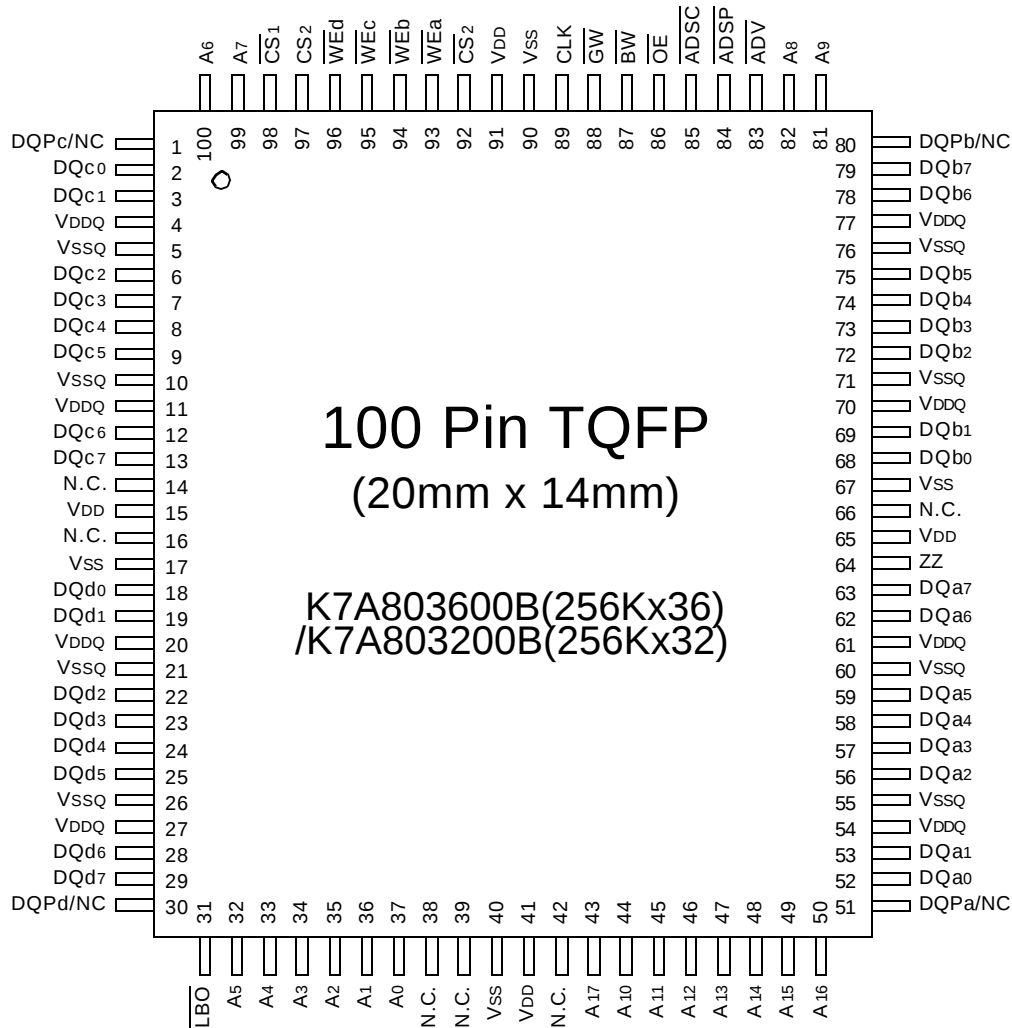
The K7A803600B, K7A803200B and K7A801800B are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package (100pin TQFP only for K7A803200B).

Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

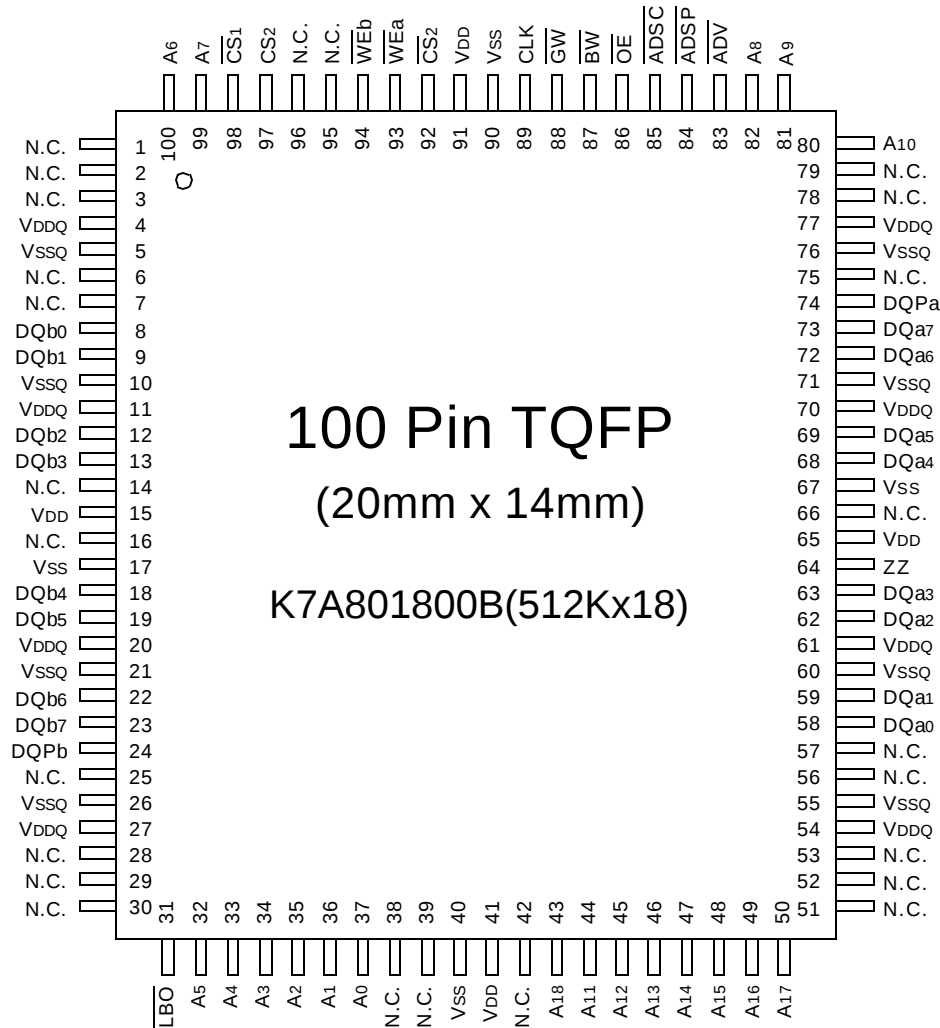


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,66
ADV	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSP	Address Status Processor	84	DQb0~b7		68,69,72,73,74,75,78,79
ADSC	Address Status Controller	85	DQc0~c7		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97	/NC		
CS2	Chip Select	92	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
WE(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
2. The pin 42 is reserved for address bit for the 16Mb .
3. DQPa~DQPd are NC for K7A803200B

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,42,51,52,53,56, 57,66,75,78,79,95,96
ADV	Burst Address Advance	83	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
ADSP	Address Status Processor	84	DQb0 ~ b7		8,9,12,13,18,19,22,23
ADSC	Address Status Controller	85	DQPa, Pb		74,24
CLK	Clock	89	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CS1	Chip Select	98	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	97			
CS2	Chip Select	92			
WEx	Byte Write Inputs	93,94			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
2. The pin 42 is reserved for address bit for the 16Mb .

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A803600B(256Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	CS ₂	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	VSS	NC	VSS	DQPb	DQb
E	DQc	DQc	VSS	$\overline{\text{CS}}_1$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{\text{OE}}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{\text{WE}}_c$	$\overline{\text{ADV}}$	$\overline{\text{WE}}_b$	DQb	DQb
H	DQc	DQc	VSS	$\overline{\text{GW}}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{\text{WE}}_d$	NC	$\overline{\text{WE}}_a$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{\text{BW}}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A ₁ *	VSS	DQa	DQa
P	DQd	DQPd	VSS	A ₀ *	VSS	DQPa	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
CS ₁	Chip Select	DQc	Data Inputs/Outputs
CS ₂	Chip Select	DQd	Data Inputs/Outputs
$\overline{\text{WE}}_x$	Byte Write Inputs	DQPa~Pd	Data Inputs/Outpus
(x=a,b,c,d)			
$\overline{\text{OE}}$	Output Enable	VDDQ	Output Power Supply
$\overline{\text{GW}}$	Global Write Enable		(2.5V or 3.3V)
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A801800B(512Kx18)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	CS ₂	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	$\overline{\text{CS}}_1$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{WE}}_b$	$\overline{\text{ADV}}$	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{\text{GW}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{\text{WE}}_a$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{BW}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A ₁ *	VSS	DQa	NC
P	NC	DQPb	VSS	A ₀ *	VSS	NC	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor	DQa	Data Inputs/Outputs
$\overline{\text{ADSC}}$	Address Status Controller	DQb	Data Inputs/Outputs
CLK	Clock	DQPa~Pb	Data Inputs/Outputs
$\overline{\text{CS}}_1$	Chip Select	VDDQ	Output Power Supply (2.5V or 3.3V)
CS ₂	Chip Select		
$\overline{\text{WE}}_x$	Byte Write Inputs		
(x=a,b)			
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable		
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7A803600B, K7A803200B and K7A801800B are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$. When $\overline{ZZ}$ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2 cycles of wake up time. $\overline{ZZ}$ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WEx}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of $\overline{CLK}$, are carried to the Data-out buffer by the next positive edge of $\overline{CLK}$. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WEx}$ are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$ (regardless of $\overline{BW}$ and $\overline{WEx}$), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WEx}$ when $\overline{GW}$ is high.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WEx}$. $\overline{WEx}$ are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WEx}$ are sampled Low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WEx}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WEx}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals ($\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$ or $\overline{WEd}$) sampled low. The $\overline{WEa}$ control $DQa0 \sim DQa7$ and $DQPa$, $\overline{WEb}$ controls $DQb0 \sim DQb7$ and $DQ Pb$, $\overline{WEc}$ controls $DQc0 \sim DQc7$ and $DQ Pc$, and $\overline{WEd}$ control $DQd0 \sim DQd7$ and $DQ Pd$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.

$\overline{WEx}$ are sampled on the same clock edge that sampled $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

ASYNCHRONOUS TRUTH TABLE

OPERATION	$\overline{ZZ}$	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. $\overline{ZZ}$ pin is pulled down internally.
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	$CS2$	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins($\overline{ZZ}$ and $\overline{OE}$).

WRITE TRUTH TABLE(x36/32)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WE d}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

Notes : 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

Notes : 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS		VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS		VDDQ	VDD	V
Voltage on Input Pin Relative to VSS		VIN	-0.3 to VDD+0.3	V
Voltage on I/O Pin Relative to VSS		VIO	-0.3 to VDDQ+0.3	V
Power Dissipation		PD	1.6	W
Storage Temperature		TSTG	-65 to 150	°C
Operating Temperature	Commercial	TOPR	0 to 70	°C
	Industrial	TOPR	-40 to 85	°C
Storage Temperature Range Under Bias		TBIAS	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE*(TA=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOU=0V	-	7	pF

*Note : Sampled not 100% tested.

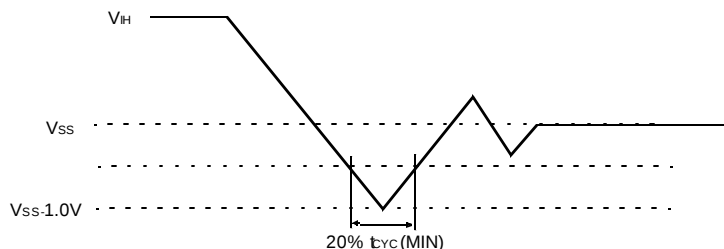
DC ELECTRICAL CHARACTERISTICS ($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES
Input Leakage Current(except	I _{IL}	$V_{DD} = \text{Max}$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	I _{OL}	Output Disabled, $V_{OUT}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, $ZZ \leq V_{IL}$, Cycle Time $\geq t_{CYC}$ Min	-16	-	350	1,2
			-14	-	300	
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, $ZZ \leq V_{IL}$, $f = \text{Max}$, All Inputs $\leq 0.2V$ or $\geq V_{DD}-0.2V$	-16	-	130	
			-14	-	120	
	I _{SB1}	Device deselected, I _{OUT} =0mA, $ZZ \leq 0.2V$, $f = 0$, All Inputs=fixed ($V_{DD}-0.2V$ or $0.2V$)	-	100	mA	
	I _{SB2}	Device deselected, I _{OUT} =0mA, $ZZ \geq V_{DD}-0.2V$, $f = \text{Max}$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	50	mA	
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V	
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V	
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V	
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V	
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V _{IH}		2.0	$V_{DD}+0.3^{**}$	V	3
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V _{IH}		1.7	$V_{DD}+0.3^{**}$	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.

2. Data states are all zero.

3. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3V$.



TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	$V_{DDQ}/2$
Output Load	See Fig. 1

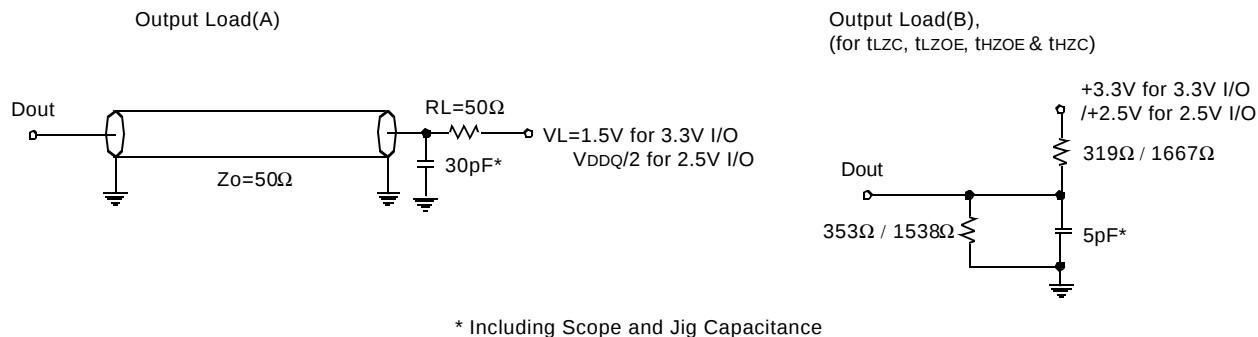


Fig. 1

AC TIMING CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

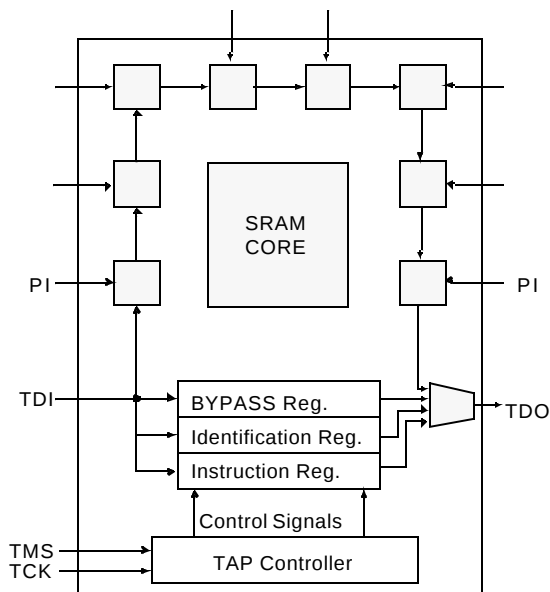
PARAMETER	Symbol	-16		-14		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	tCYC	6.0	-	7.2	-	ns
Clock Access Time	tCD	-	3.5	-	3.8	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.8	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.0	-	3.5	ns
Clock High to Output High-Z	tHZC	1.5	3.0	1.5	3.5	ns
Clock High Pulse Width	tCH	2.3	-	2.5	-	ns
Clock Low Pulse Width	tCL	2.3	-	2.5	-	ns
Address Setup to Clock High	tAS	1.5	-	1.5	-	ns
Address Status Setup to Clock High	tSS	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWS	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



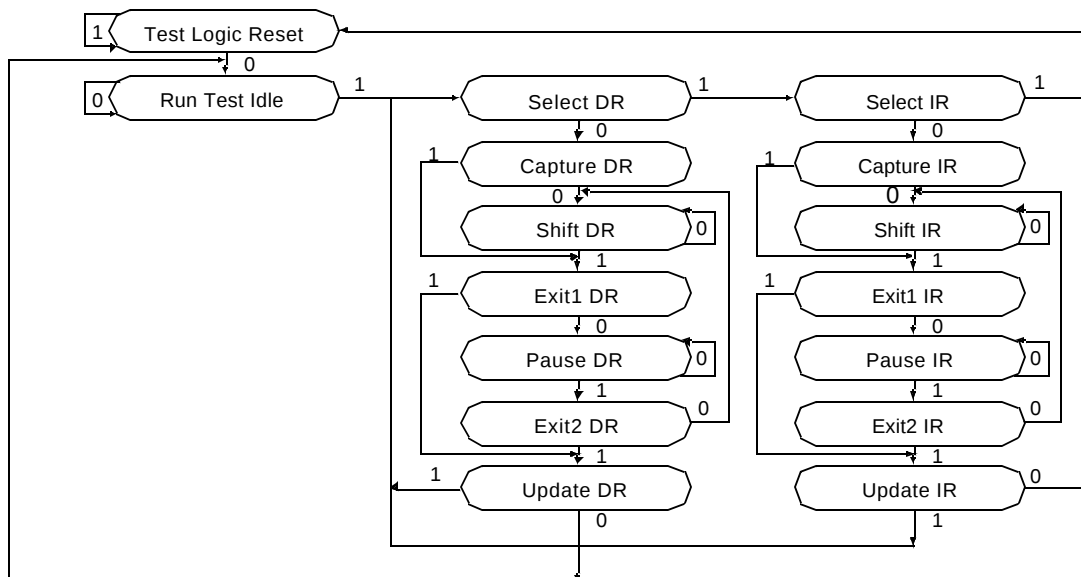
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx36	3 bits	1 bits	32 bits	70 bits
512Kx18	3 bits	1 bits	32 bits	70 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
256Kx36	0000	00110 00100	XXXXXX	00001001110	1
512Kx18	0000	00111 00011	XXXXXX	00001001110	1

119BGA BOUNDARY SCAN EXIT ORDER(x36)

36	4B	ADSC		OE	4F	35
37	4E	CS1		ADV	4G	34
38	4H	GW		CLK	4K	33
39	3G	BWc		BW	4M	32
40	3C	A		ADSP	4A	31
41	3B	A		BWb	5G	30
42	3A	A		A	5C	29
43	2B	CS2		A	5B	28
44	2C	A		A	5A	27
45	2A	A		A	6B	26
46	2D	DQPc		A	6A	25
47	1E	DQc		A	6C	24
48	2F	DQc		DQPb	6D	23
49	1G	DQc		DQb	6E	22
50	2H	DQc		DQb	6G	21
51	1D	DQc		DQb	7H	20
52	2E	DQc		DQb	7D	19
53	2G	DQc		DQb	7E	18
54	1H	DQc		DQb	6F	17
55	2K	DQd		DQb	7G	16
56	1L	DQd		DQb	6H	15
57	2M	DQd		DQa	7K	14
58	1N	DQd		DQa	6L	13
59	1P	DQd		DQa	6N	12
60	1K	DQd		DQa	7P	11
61	2L	DQd		DQa	6K	10
62	2N	DQd		DQa	7L	9
63	2P	DQPd		DQa	6M	8
64	3R	LBO		DQa	7N	7
65	3L	BWd		DQPa	6P	6
66	2R	A		ZZ	7T	5
67	3T	A		A	6R	4
68	4N	A1		BW a	5L	3
69	4P	A0		A	5T	2
70	2T	NC		A	4T	1

119BGA BOUNDARY SCAN EXIT ORDER(x18)

36	4B	ADSC		OE	4F	35
37	4E	CS1		ADV	4G	34
38	4H	GW		CLK	4K	33
39	3G	BWb		BW	4M	32
40	3C	A		ADSP	4A	31
41	3B	A		NC	5G	30
42	3A	A		A	5C	29
43	2B	CS2		A	5B	28
44	2C	A		A	5A	27
45	2A	A		A	6B	26
46	2D	NC		A	6A	25
47	1E	NC		A	6C	24
48	2F	NC		NC	7D	23
49	1G	NC		NC	6E	22
50	2H	NC		NC	6G	21
51	1D	DQb		NC	7H	20
52	2E	DQb		DQPa	6D	19
53	2G	DQb		DQa	7E	18
54	1H	DQb		DQa	6F	17
55	2K	DQb		DQa	7G	16
56	1L	DQb		DQa	6H	15
57	2M	DQb		DQa	7K	14
58	1N	DQb		DQa	6L	13
59	2P	DQPb		DQa	6N	12
60	1K	NC		DQa	7P	11
61	2L	NC		NC	6K	10
62	2N	NC		NC	7L	9
63	1P	NC		NC	6M	8
64	3R	LBO		NC	7N	7
65	3L	NC		NC	6P	6
66	2R	A		ZZ	7T	5
67	3T	A		A	6R	4
68	4N	A1		BW a	5L	3
69	4P	A0		A	5T	2
70	2T	A		A	4T	1

NOTE : NC ; Don't care.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O / 2.5V I/O)	V _{IH}	2.0 / 1.7	-	V _{DD} +0.3	V	1
Input Low Level (3.3V I/O / 2.5V I/O)	V _{IL}	-0.3	-	0.8 / 0.7	V	
Output High Voltage (3.3V I/O / 2.5V I/O)	V _{OH}	2.4 / 2.0	-	-	V	
Output Low Voltage (3.3V I/O / 2.5V I/O)	V _{OL}	-	-	0.4 / 0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

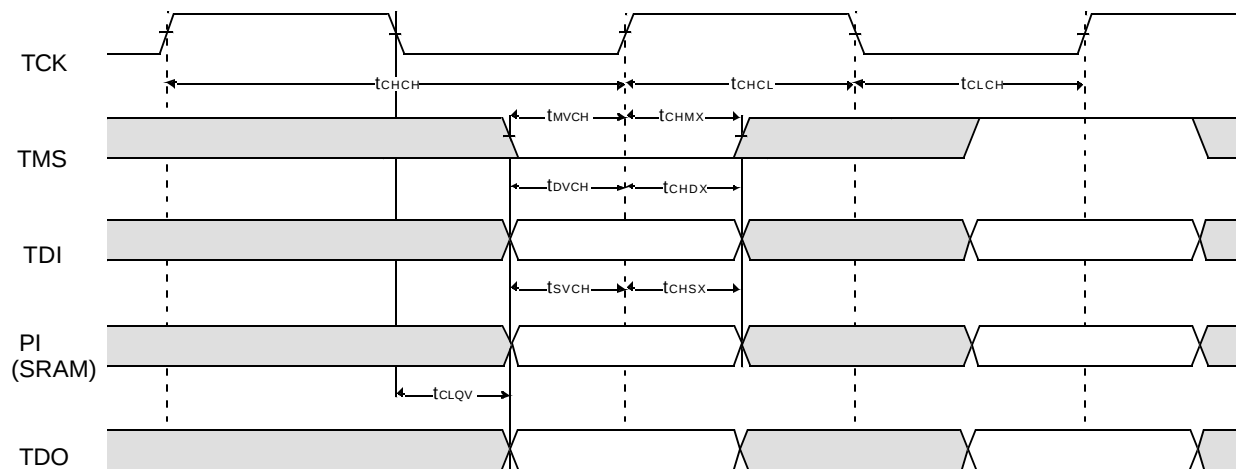
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level (3.3V I/O / 2.5V I/O)	V _{IH} /V _{IL}	3.0 / 0 , 2.5 / 0	V	
Input Rise/Fall Time (3.3V I/O / 2.5V I/O)	TR/TF	1.0 / 1.0 , 1.0 / 1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

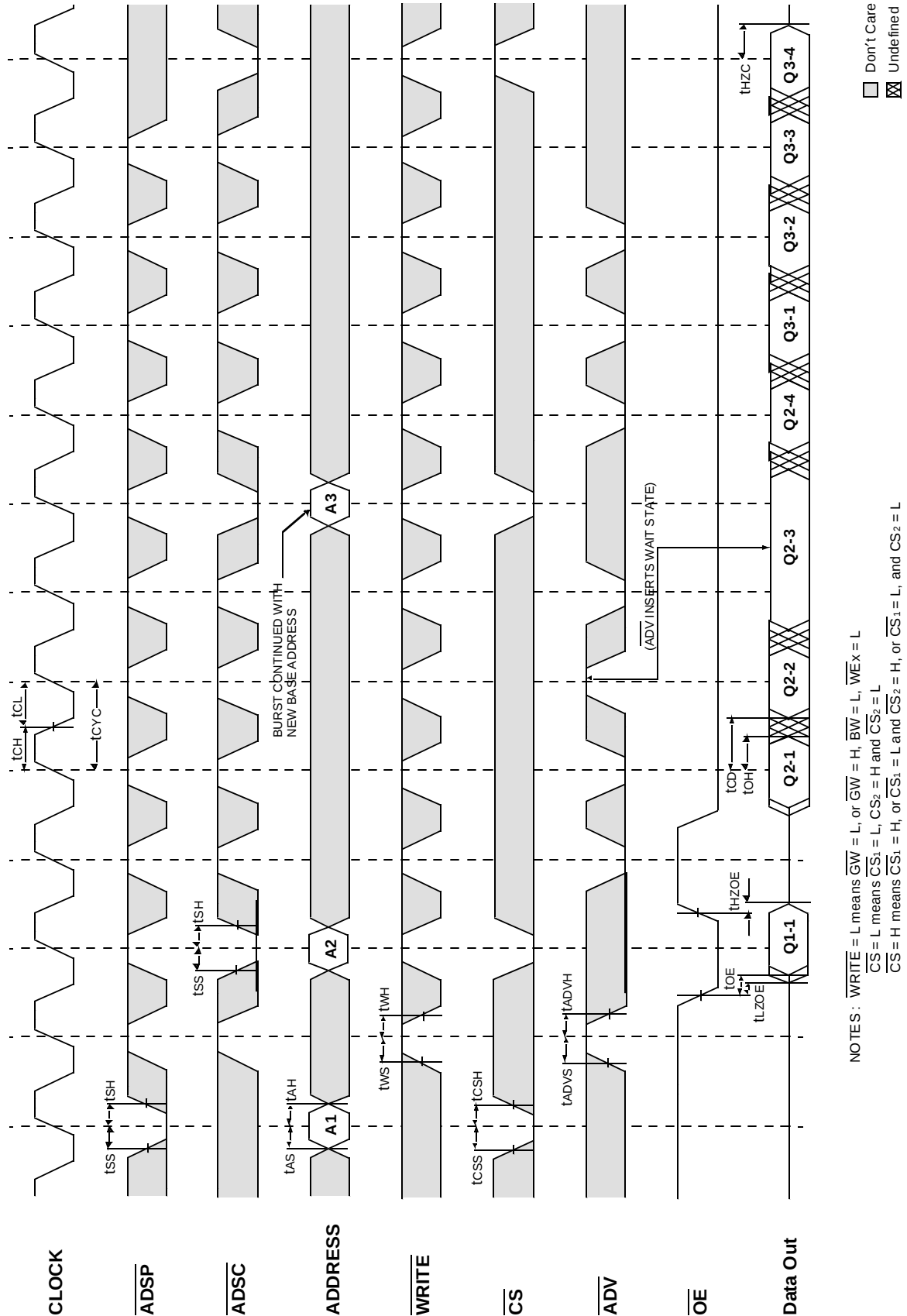
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

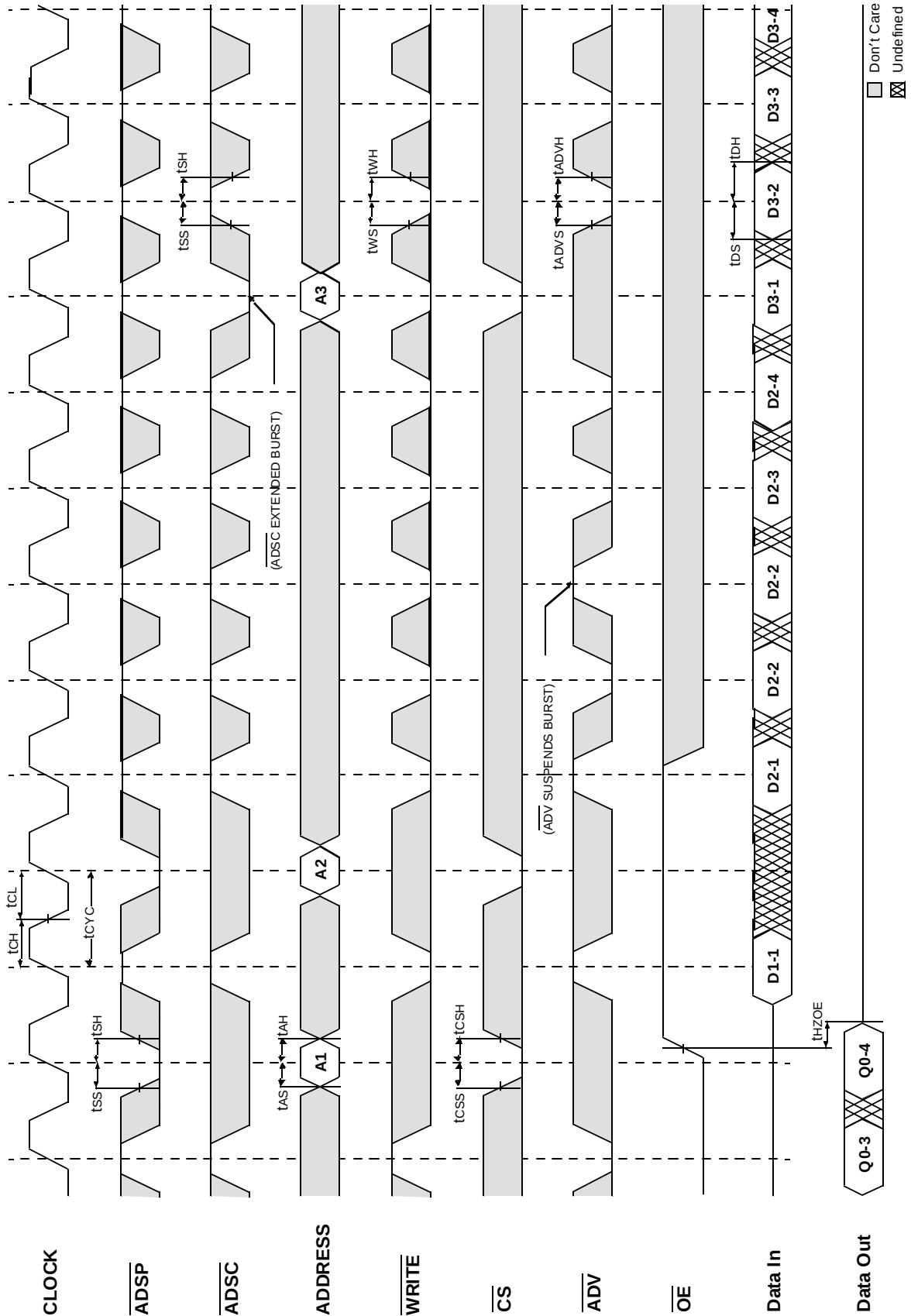
JTAG TIMING DIAGRAM



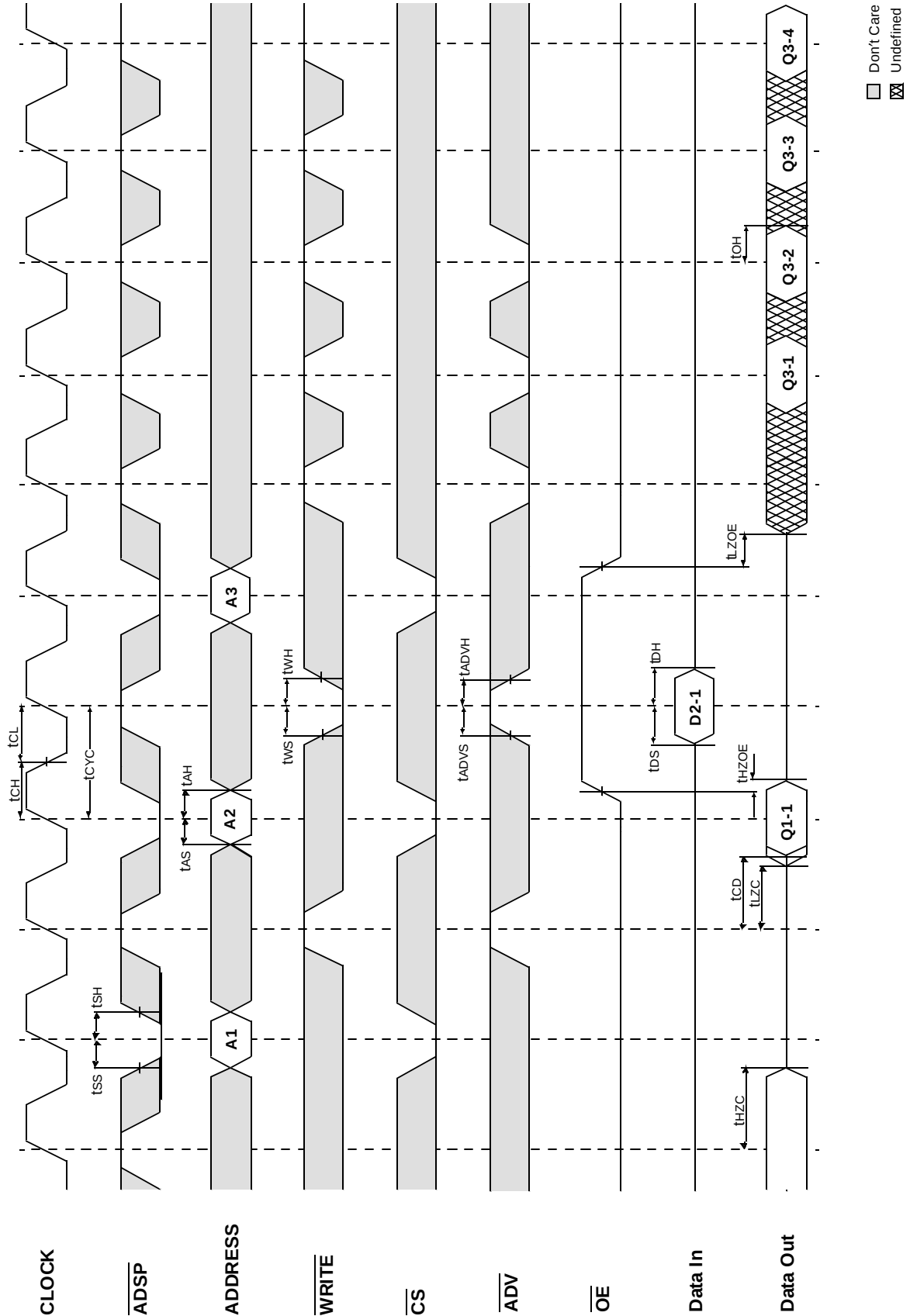
TIMING WAVEFORM OF READ CYCLE



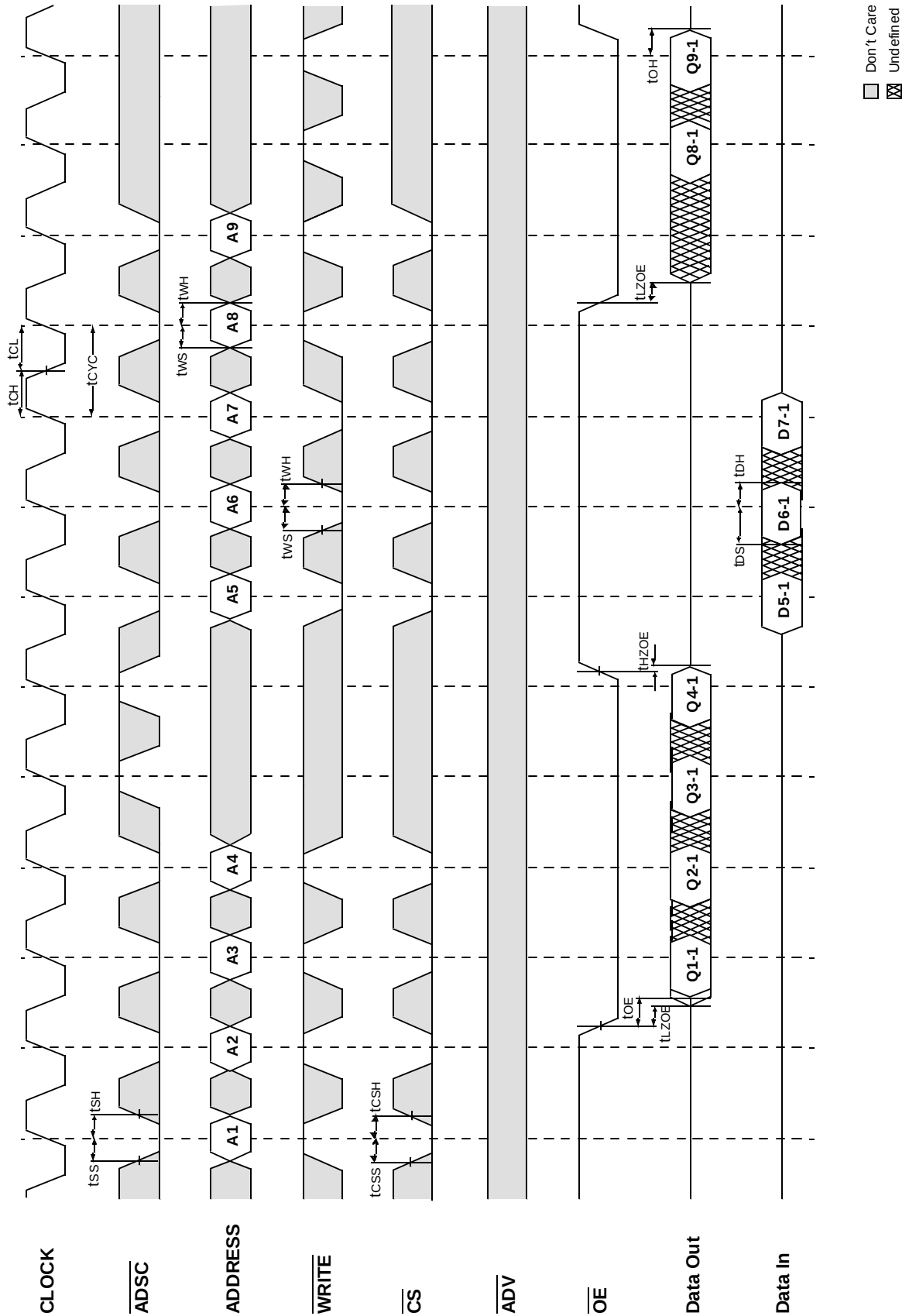
TIMING WAVEFORM OF WRTE CYCLE



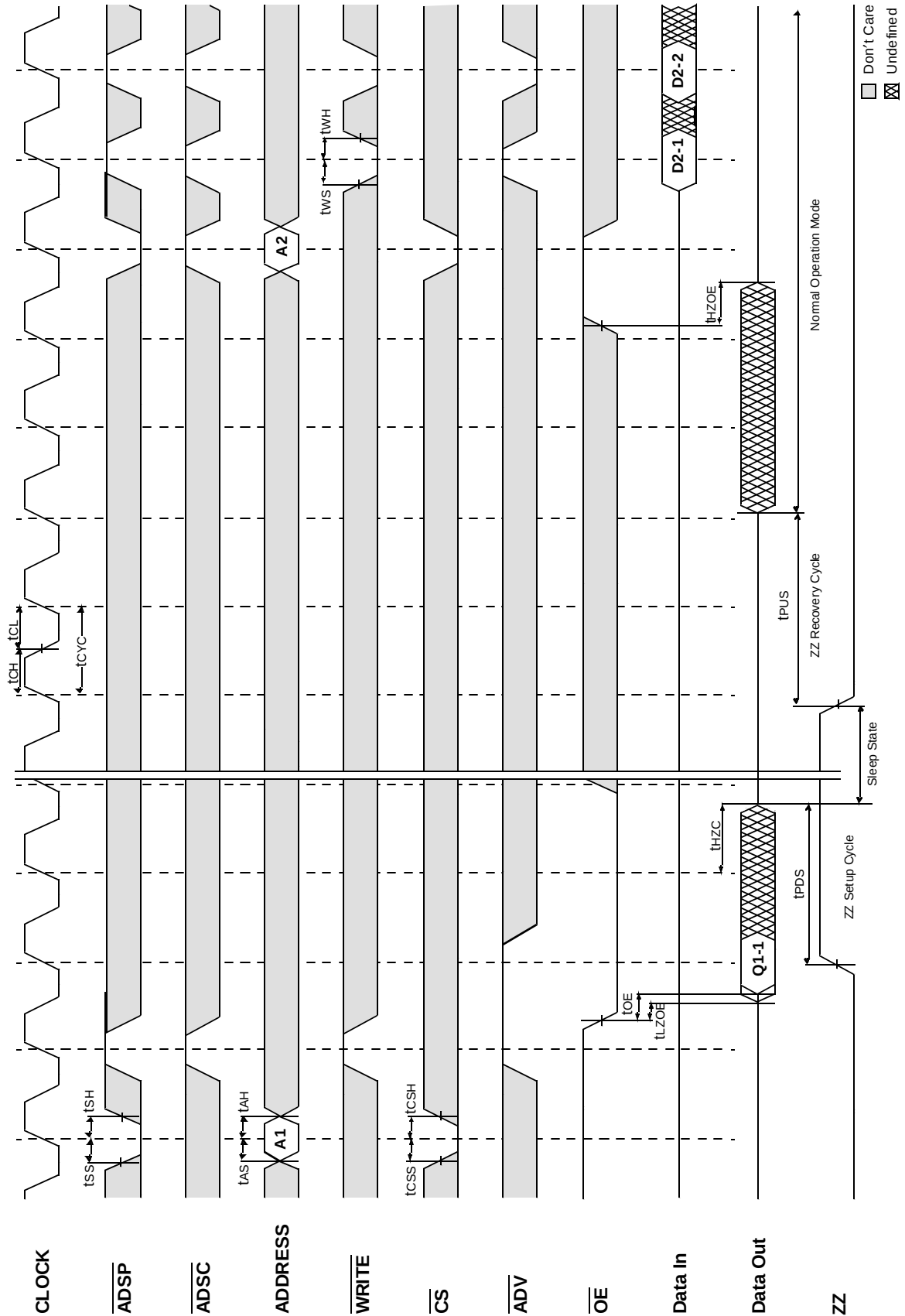
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, $\overline{\text{ADSC}}=\text{HIGH}$)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, $\overline{\text{ADSP}}=\text{HIGH}$)



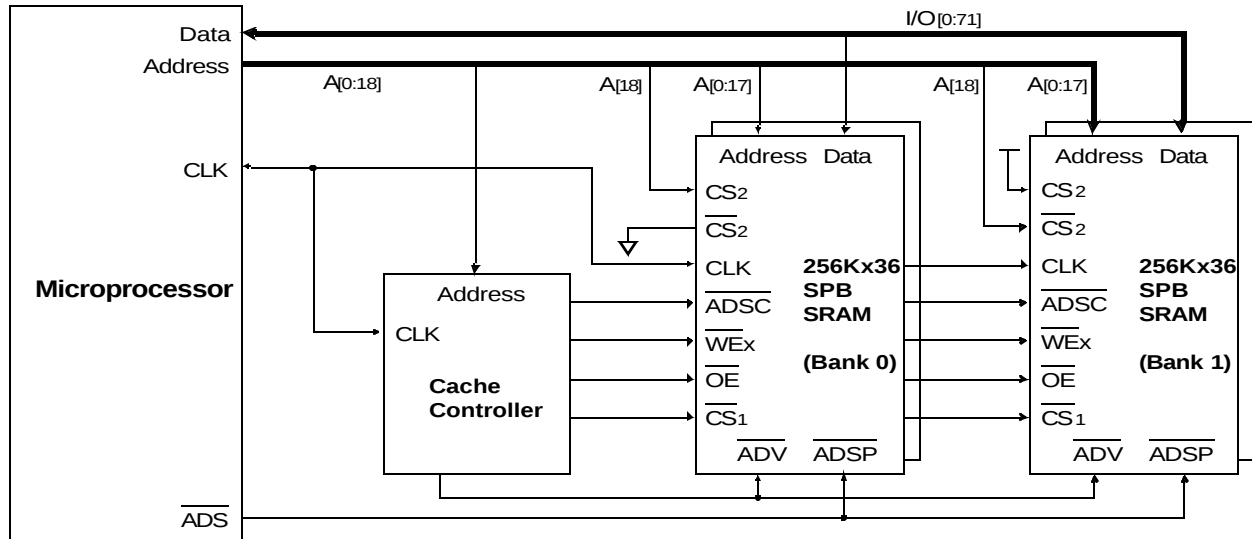
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

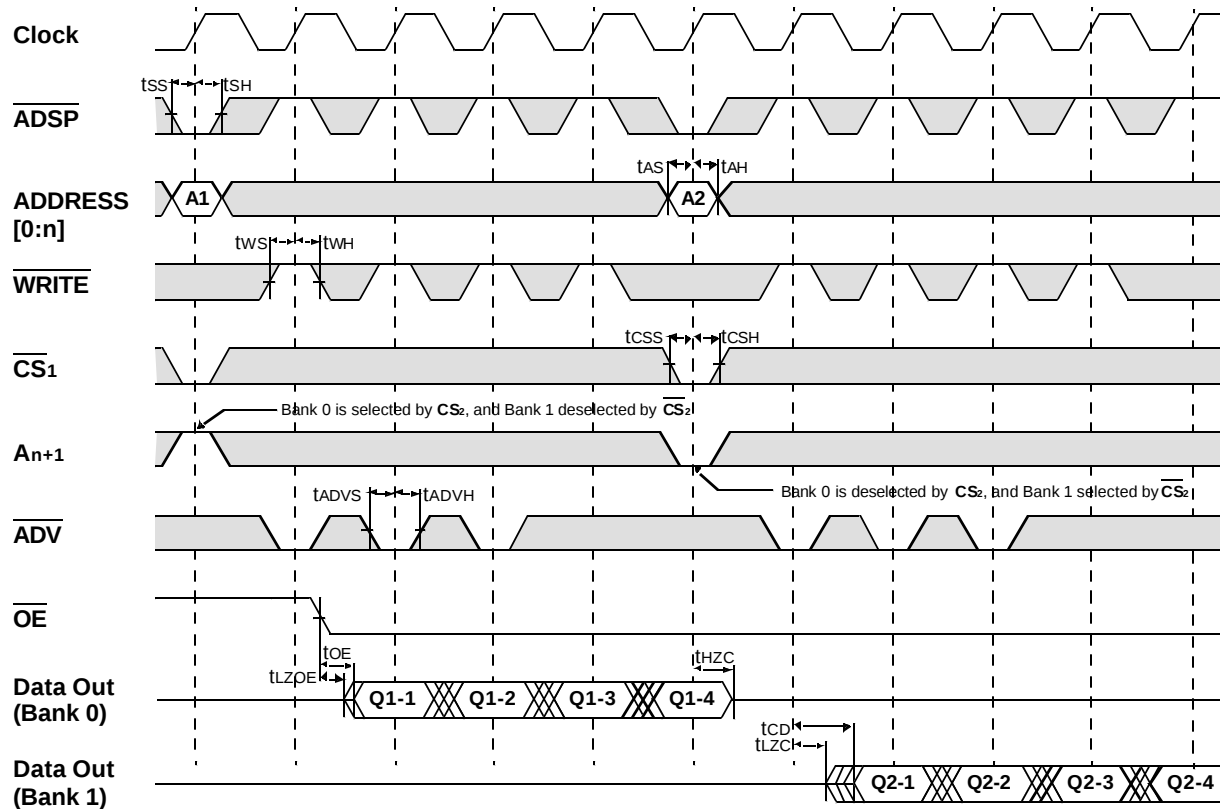
DEPTH EXPANSION

The Samsung 256Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



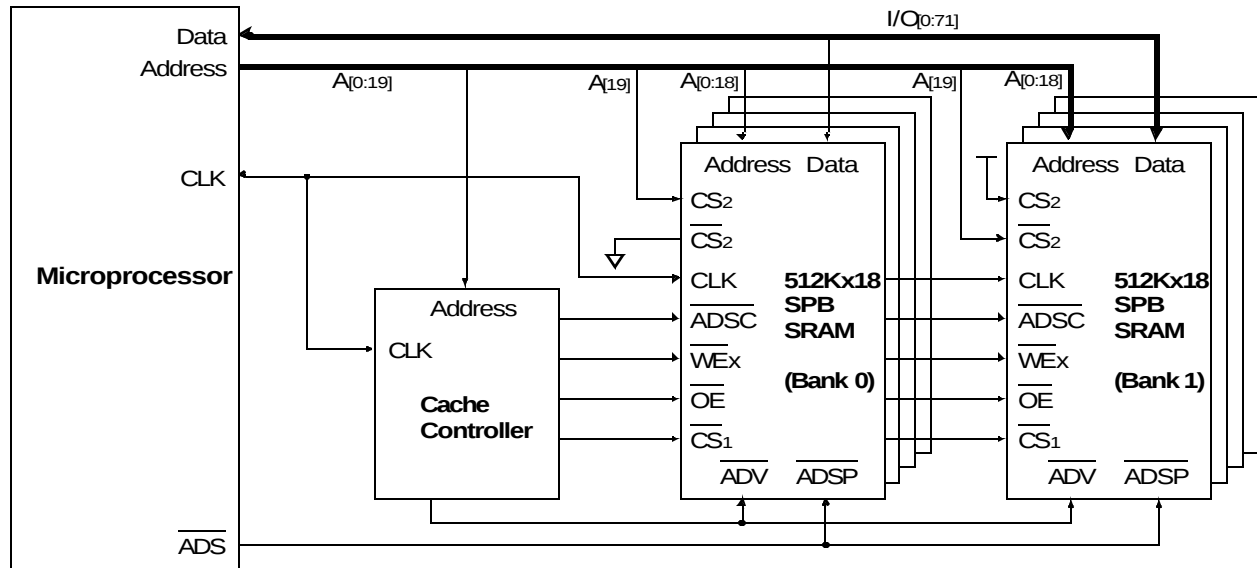
*Notes : n = 14 32K depth, 15 64K depth
16 128K depth, 17 256K depth
18 512K depth

□ Don't Care ■ Undefined

APPLICATION INFORMATION

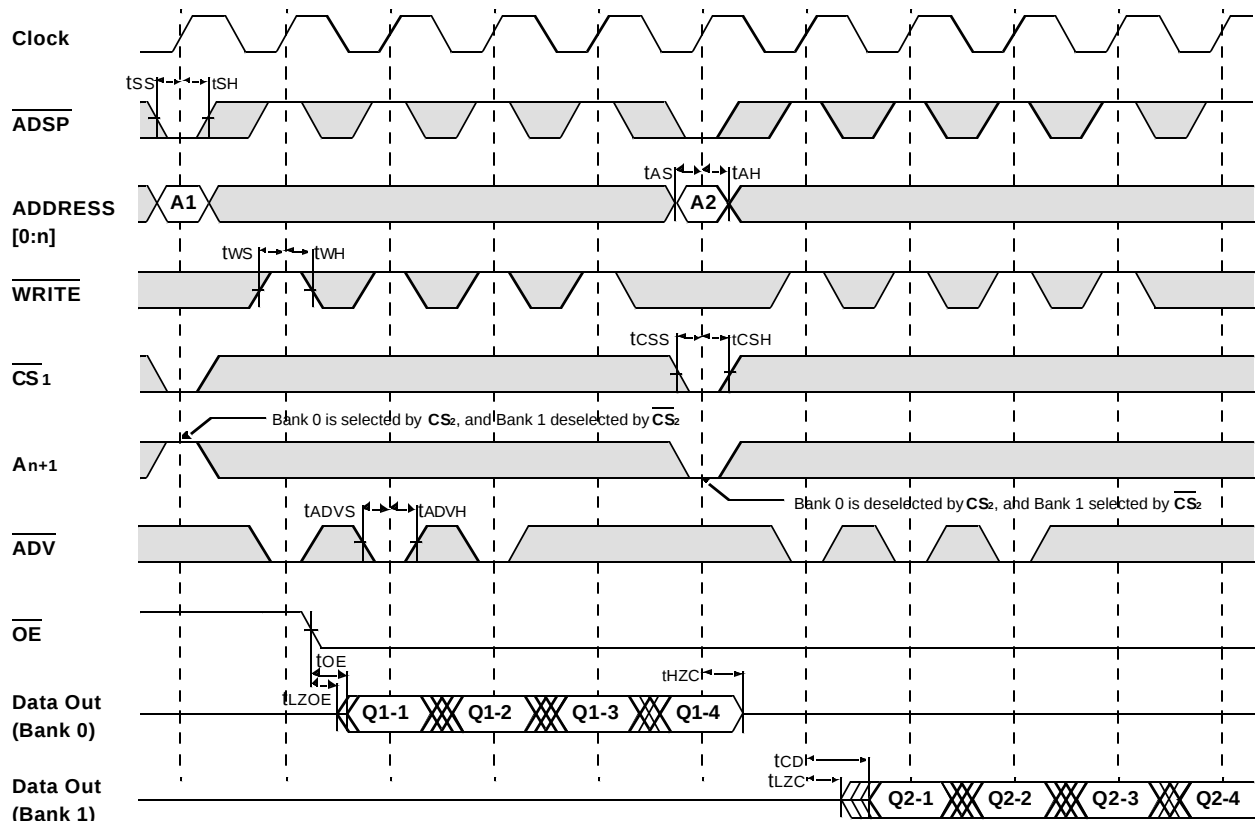
DEPTH EXPANSION

The Samsung 512Kx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

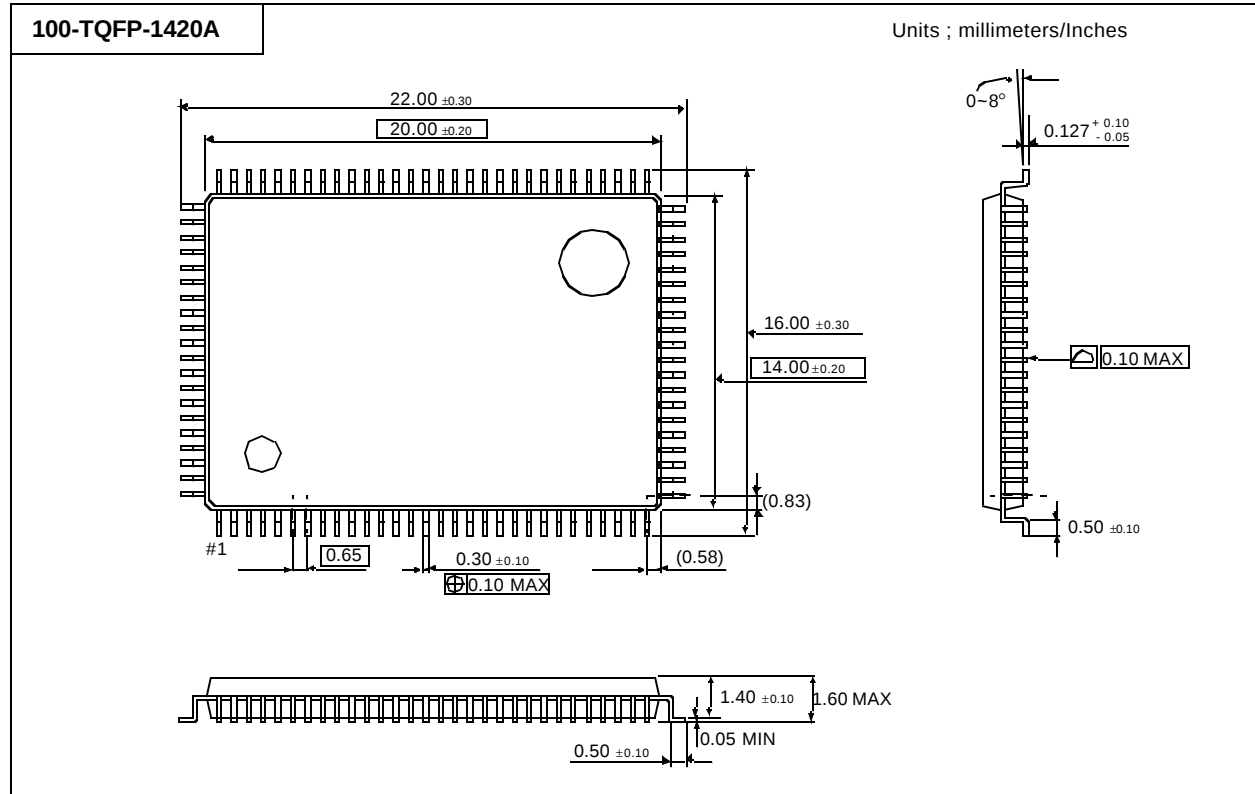
(ADSP CONTROLLED, ADSC=HIGH)



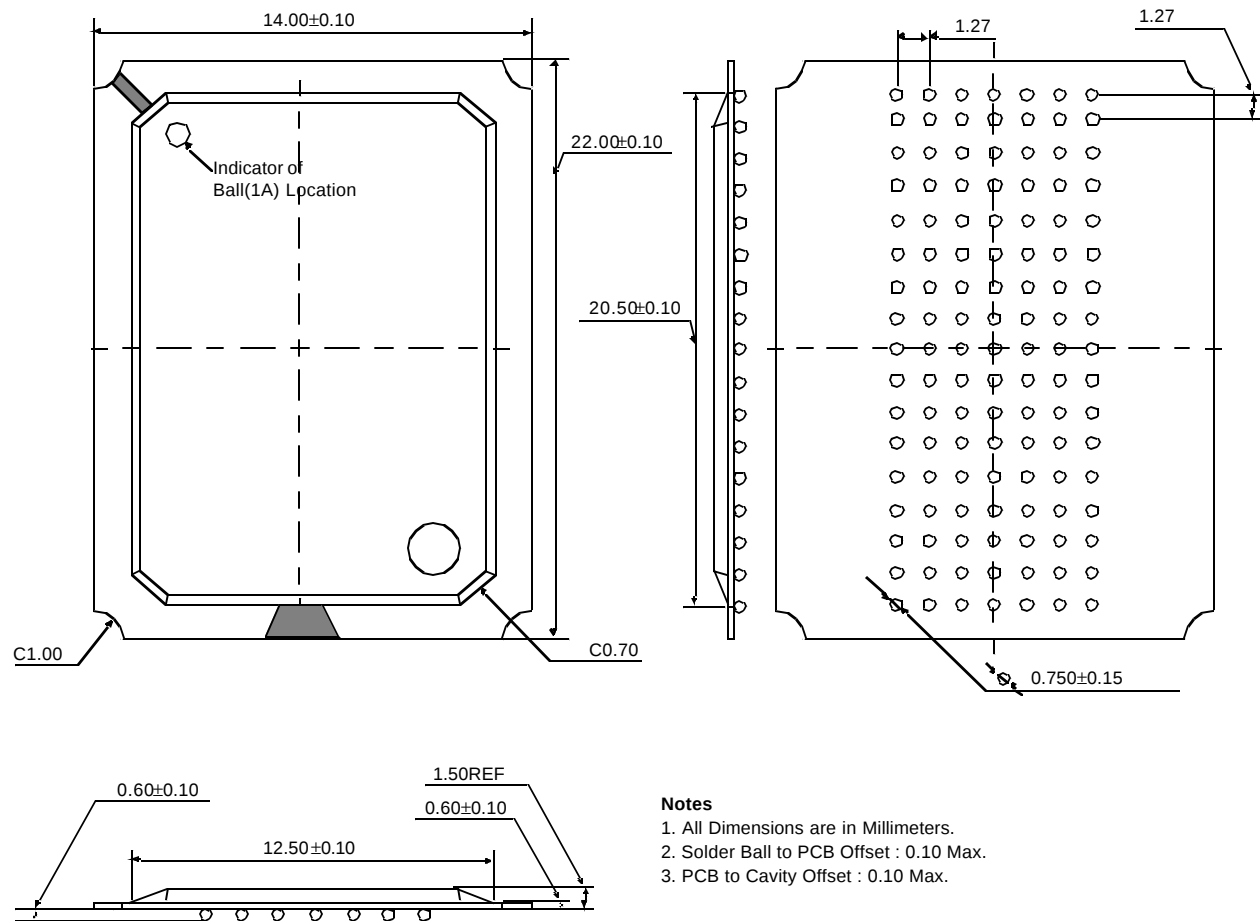
*Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

⊠ Undefined □ Don't Care

PACKAGE DIMENSIONS



119BGA PACKAGE DIMENSIONS



Notes

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 Max.
3. PCB to Cavity Offset : 0.10 Max.