STANDARD
MICROSYSTEMS
CORPORATION

KBD42W11

Keyboard Controller

FEATURES

- Supports IBM PC and Compatible System Designs
- Runs Much Faster Than Traditional Keyboard Controllers
- Host interface Compatible with Traditional Keyboard Controller
- 6 MHz – 12 MHz Operating Frequency
- Communicates with Keyboard Directly
- High-reliability CMOS Technology
- 40 Pin DIP and 44 Pin PLCC Package

GENERAL DESCRIPTION

The KBD42W11 keyboard controller is programmed to support the IBM® compatible personal computer keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks the parity of the data, translates the scan code, and presents the data to the system as a byte of data in its output buffer. The controller will interrupt the system when data is placed in its output buffer. The byte of data will be sent to the keyboard serially with an odd parity bit automatically inserted. The keyboard is required to acknowledge all data transmissions. No transmission should be sent to the keyboard until acknowledgment is received for the previous byte sent.

The KBD42W11 keyboard controller and BIOS to improve the performance of IBM PC machines and their compatibles. A hardwire methodology is used in this keyboard controller instead of a software implementation, as in the traditional 8042 keyboard BIOS. This enables the keyboard controller to respond instantly to all commands sent from the keyboard to the CPU BIOS.

The KBD42W11 enables popular programs such as AutoCAD®, Microsoft® Windows™, NOVELL®, and other programs to run much faster.

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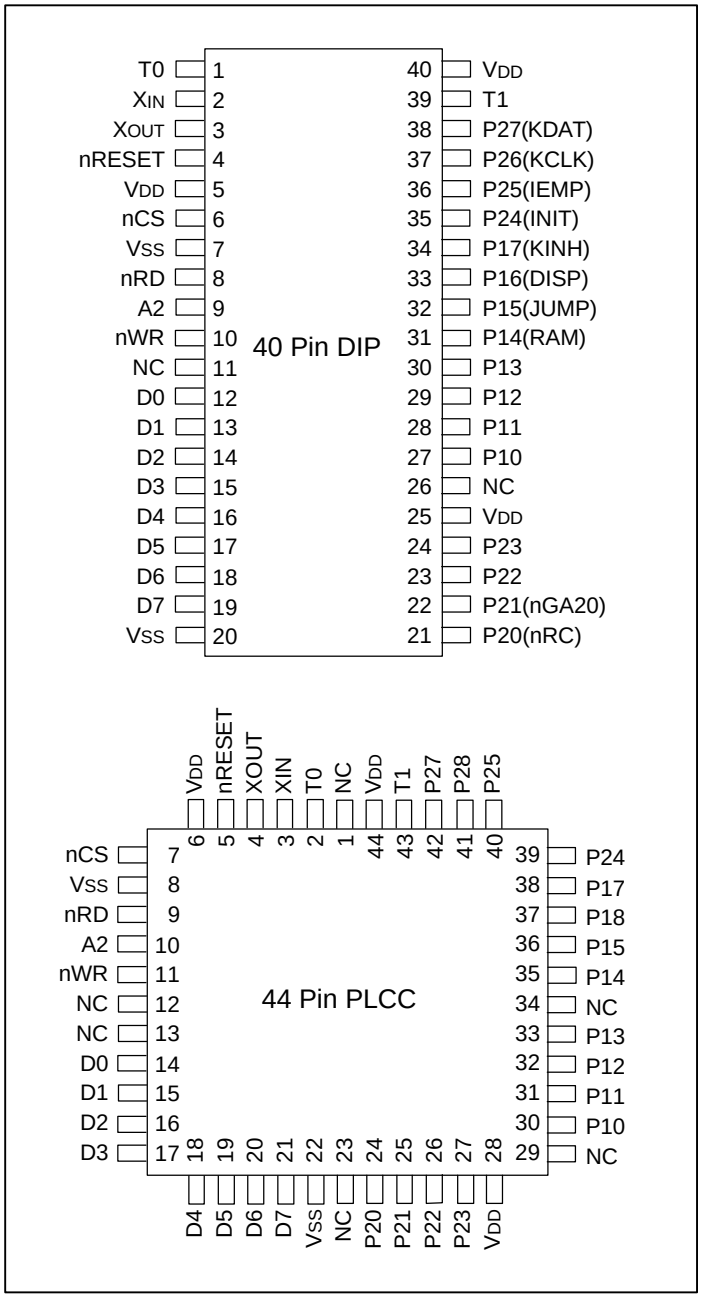
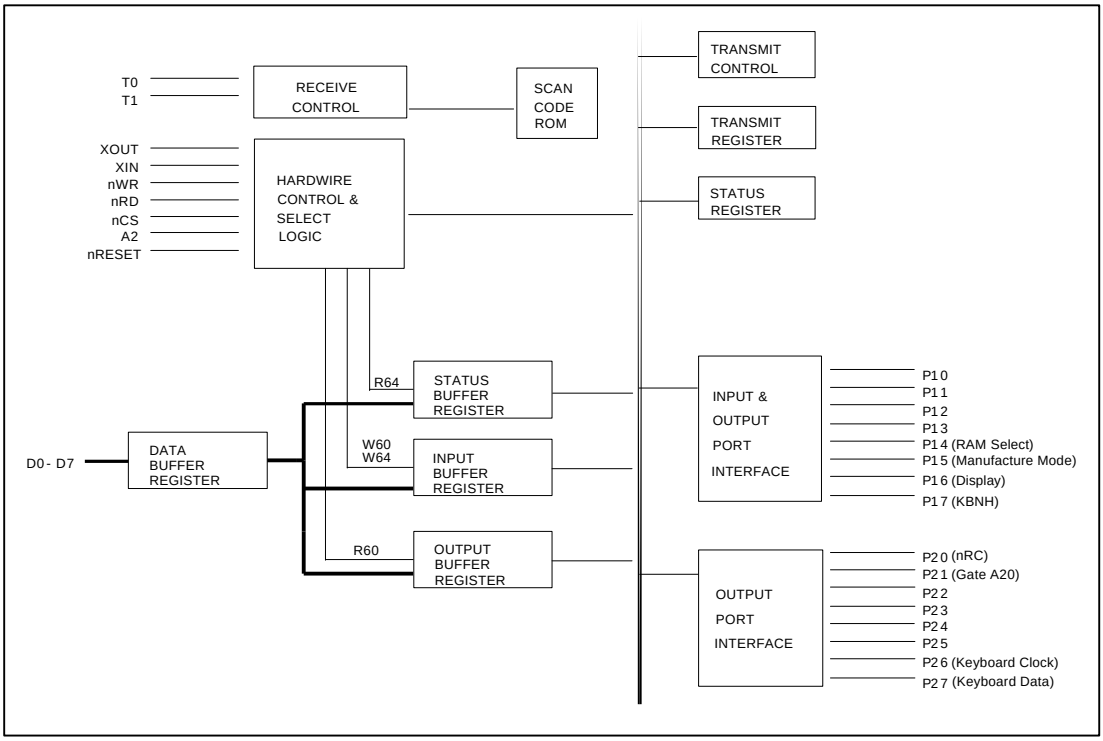
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO. (40 Pin DIP)	PIN NO. (44 Pin PLCC)	I/O	NAME	FUNCTION
1	2	I	T0	K/B Clock Input
2	3	I	XIN	Crystal Clock I/P
3	4	O	XOUT	Crystal Clock O/P
4	5	I	nRESET	Chip Reset
5	6	-	VDD	Optional +5V Power Supply
6	7	I	nCS	Chip Select
7	8	-	VSS	Optional Ground Power
8	9	I	nRD	I/O Read
9	10	I	A2	Connect to Address A2
10	11	I	nWR	I/O Write
11,26	1,12,13,23,29, 34	-	NC	Reserved
12,13,14, 15,16,17, 18, 19	14,15,16,17,18, 19,20,21	I/O	D0-D7	Data Bus D0 - D7
20	22	-	VSS	Ground Power Supply
21	24	O	P20	Bit 0 of Port 2 (RCB: System Reset)
22	25	O	P21	Bit 1 of Port 2 (GA20: GATE A20)
23	26	I/O	P22	Bit 2 of Port 2
24	27	I/O	P23	Bit 3 of Port 2
25	28	-	VDD	Optional +5V Power Supply
27	30	I/O	P10	Bit 0 of Port 1
28	31	I/O	P11	Bit 1 of Port 1
29	32	I/O	P12	Bit 2 of Port 1
30	33	I/O	P13	Bit 3 of Port 1
31	35	I	P14	Bit 4 of Port 1 (RAM Jumper Select)
32	36	I	P15	Bit 5 of Port 1 (JUMP)
33	37	I	P16	Bit 6 of Port 1 (Display Select)
34	38	I	P17	Bit 7 of Port 1 (K/B Inhibit Switch)
35	39	O	P24	Bit 4 of Port 2 (OBF O/P Interrupt)
36	40	O	P25	Bit 5 of Port 2 (I/P Buffer Empty)
37	41	O	P26	Bit 6 of Port 2 (K/B Clock O/P)
38	42	O	P27	Bit 7 of Port 2 (K/B Data O/P)
39	43	I	T1	K/B Data Input
40	44	-	VDD	+5V Power Supply

BLOCK DIAGRAM

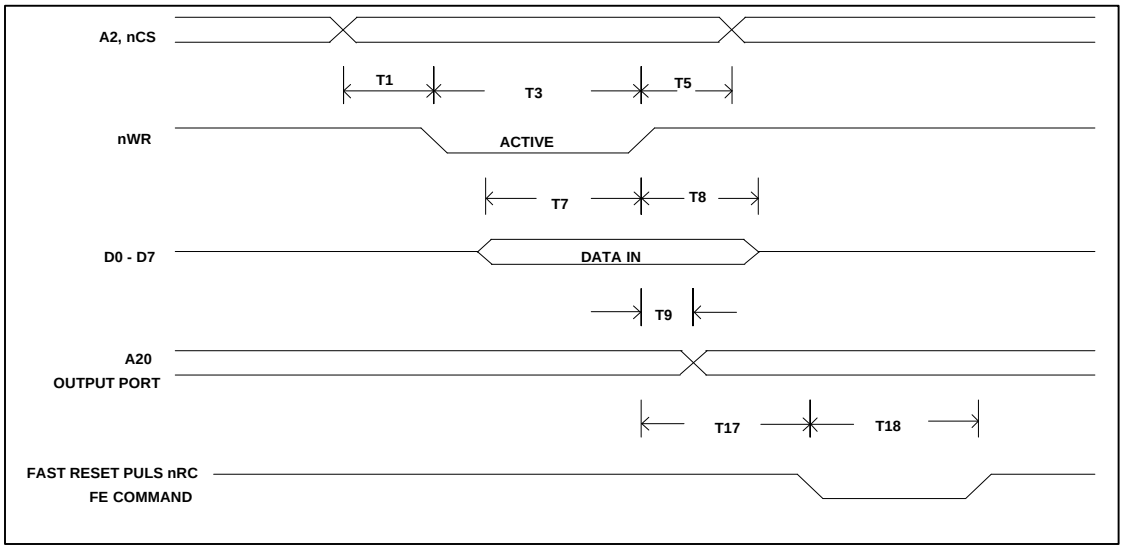


AC TIMING

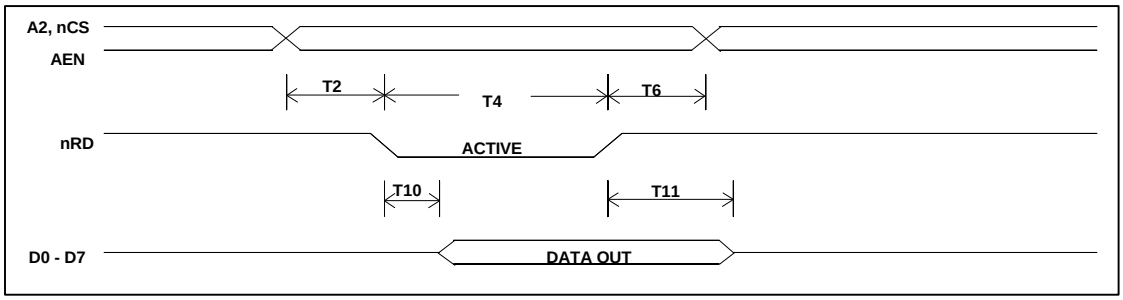
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from nWR	0		nS
T2	Address Setup Time from nRD	0		nS
T3	nWR Strobe Width	20		nS
T4	nRD Strobe Width	20		nS
T5	Address Hold Time from nWR	0		nS
T6	Address Hold Time from nRD	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from nWR	10		nS
T10	nRD to Drive Data Delay		20	nS
T11	nRD to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T17	nRC Fast Reset Pulse Delay (8 MHz)	2	3	µS
T18	nRC Pulse Width (8 MHz)	6		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	XIN/XOUT Period (6-12 MHz)	83	167	nS

TIMING WAVEFORMS

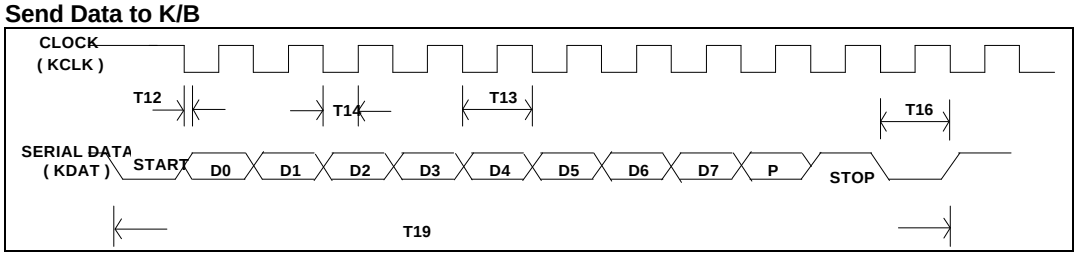
Write Cycle Timing



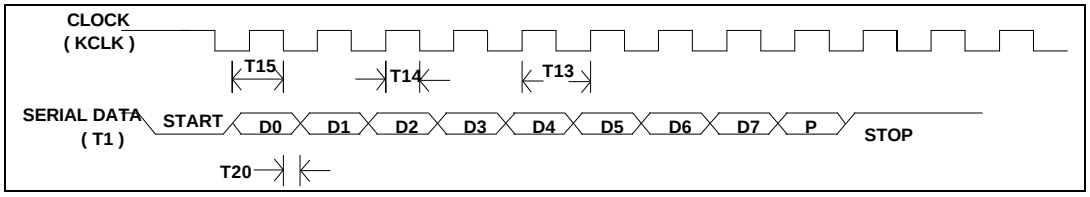
Read Cycle Timing



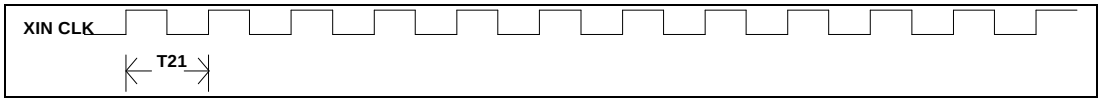
Send Data to K/B



Receive Data from K/B



XIN/XOUT Clock



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Operating Temperature	-0 to +85	°C
Storage Temperature	-65 to +150	°C
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	50	mW

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta = 0° C to +70° C, VDD = +5V ±5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
VDD	Power Supply	4.75	5.0	5.25	V
TA	Operating Temperature	0	25	70	V
VIH	High Level Voltage for TTL Min. I/P	2.0		VDD	V
VIL	Low Level Voltage for TTL Max. I/P	-0.3		0.8	V
VOH	High Level Voltage for TTL Min. O/P	VDD-0.5			V
VOL	Low Level Voltage for TTL Max. O/P			0.5	V
RIP	Min. I/P Resist	10K			Ω
ILI	I/P Leakage Current	-10		10	µA
ILO	O/P Leakage Current	-10		10	µA
IOL	O/P Sink Current	4			mA
CL	O/P Load Capacity	15		50	pF

STATUS REGISTER

The status register is an 8-bit read-only register at I/O address hex 64 that holds information about the state of the keyboard controller and interface. It may be read at any time.

BIT	BIT DESCRIPTION	FUNCTION
0	Output Buffer Full	0: Output Buffer Empty 1: Output Buffer Full
1	Input Buffer Full	0: Input Buffer Empty 1: Input Buffer Full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It is set to 0 after a power-on reset
3	Command/data	0: Data Byte 1: Command Byte
4	Inhibit Switch	0: Keyboard is Inhibited 1: Keyboard is Not Inhibited
5	Transmit Time Out	0: No Transmit Time Out Error 1: Transmit Time Out Error
6	Receive Time Out	0: No Receive Time Out Error 1: Receive Time Out Error
7	Parity Error	0: Odd Parity (No Error) 1: Even Parity (Error)

OUTPUT BUFFER

The output buffer is an 8-bit read-only register at I/O address hex 60. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by command to the system. The output buffer should be read only when the output buffer full bit in the register is 1.

INPUT BUFFER

The input buffer is an 8-bit write-only register at I/O address hex 60 or 64. Writing to address hex 60 sets a flag that indicates a data write; writing to address hex 64 sets a flag that indicates a command write. Data written to I/O address hex 60 are sent to the keyboard (unless the keyboard controller is expecting a data byte) following the controller's input buffer only if the input buffer full bit in the status register is set to 0.

I/O PORTS

The keyboard controller has two 8-bit I/O ports and two test inputs. One of the ports is assigned for input and the other for output. The controller uses the test inputs to read the state of the keyboard's clock line and data line.

The following figures show bit definitions for the input, output, and test-input ports.

(A) Input Port Definitions

BIT	FUNCTION
0	Undefined
1	Undefined
2	Undefined
3	Undefined
4	RAM on System Board 0: Disable 2nd 256 KB of System Board RAM 1: Enable 2nd 256 KB of System Board RAM
5	Manufacturing Jumper Installed 0: Manufacturing Jumper 1: Jumper Not Installed
6	Display Type Switch 0: Primary Display Attached to Color/graphics 0: Primary Display Attached to Monochrome
7	Keyboard Inhibit Switch 0: Keyboard Inhibited 1: Keyboard Not Inhibited

(B) Output Port Definitions

BIT	FUNCTION
0	System Reset
1	Gate A20
2	Undefined
3	Undefined
4	Output Buffer Full
5	Input Buffer Empty
6	Keyboard Clock (Output)
7	Keyboard Data (Output)

(C) Test-Input Definitions

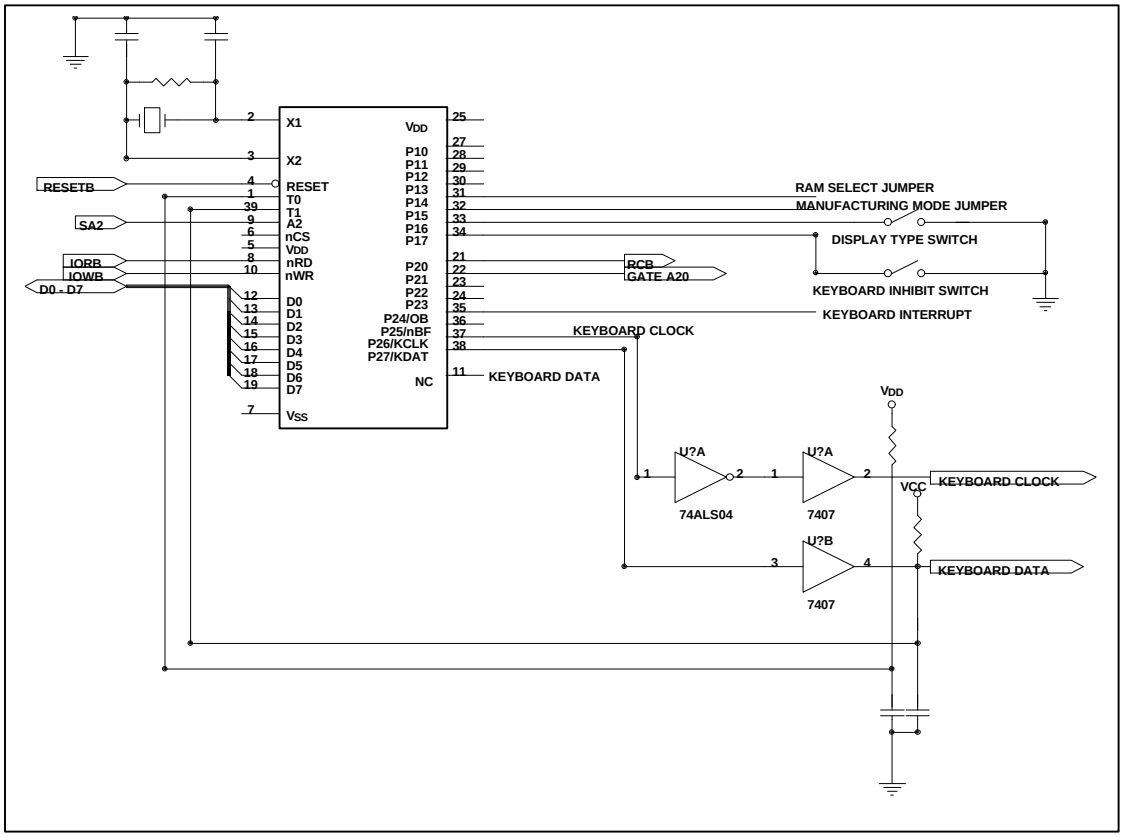
BIT	FUNCTION
0	Keyboard Clock (Input)
1	Keyboard Data (Input)

COMMANDS (I/O ADDRESS HEX 64)

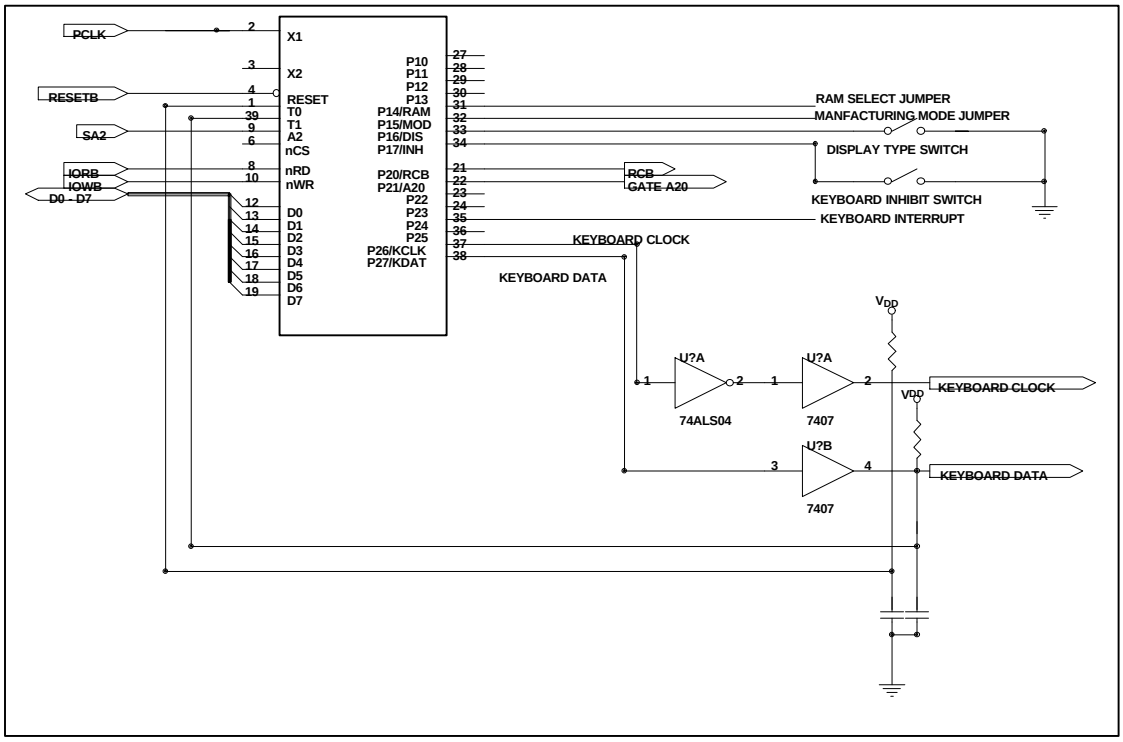
COMMAND	FUNCTION
20	Read Command Byte of Keyboard Controller
60	Write Command Byte of Keyboard Controller **BIT** **BIT DEFINITIONS** 7 Reserved 6 IBM PC Compatible Mode 5 IBM PC Mode 4 Disable Keyboard 3 Inhibit Override 2 System Flag 1 Reserved 0 Enable Output Buffer Full Interrupt
AA	Self-test **BIT** **BIT DEFINITIONS** 00 No Error Detected 01 K/B Clock Line is Stuck Low 02 K/B Clock Line is Stuck High 03 K/B Data Line is Stuck Low 04 K/B Data Line is Stuck High
AB	Interface Test
AD	Disable Keyboard Feature
AE	Enable Keyboard Interface
C0	Read Input Port
D0	Read Output Port
D1	Write Output Port
E0	Read Test Inputs
F0-FF	Pulse Output Port

APPLICATION CIRCUIT

Asynchronous

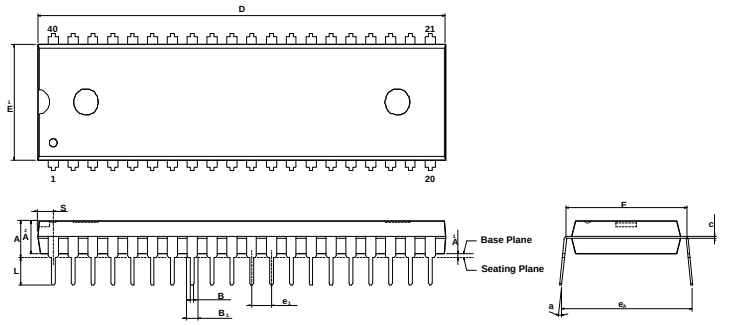


Synchronous



PACKAGE DIMENSIONS

40 Pin PDIP

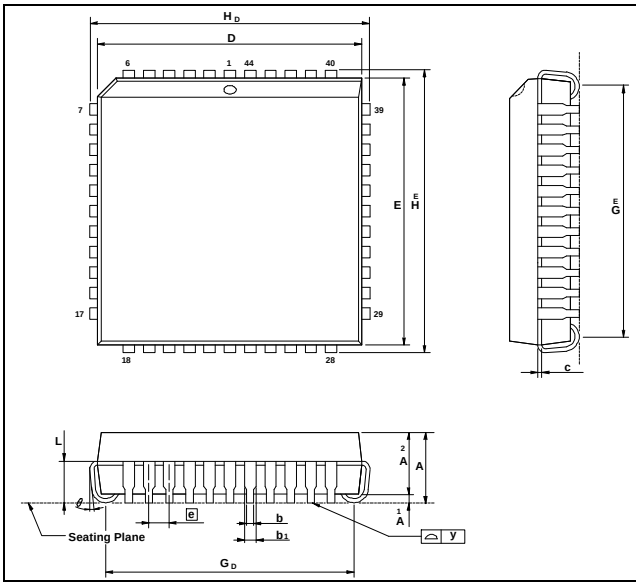


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:

1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44 Pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

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