KS8723 – Single Port 10/100 PHY / MAC / PCI

Introduction

The KS8723 is a single-chip, full duplex, 10/100Mbps Ethernet MAC + PHY incorporating a 32-bit PCI with bus master support. The KS8723 is designed for use in a variety of applications including workstation NICs, PC motherboards, and other systems utilizing a PCI bus that require network connectivity to an Ethernet or Fast Ethernet LAN.

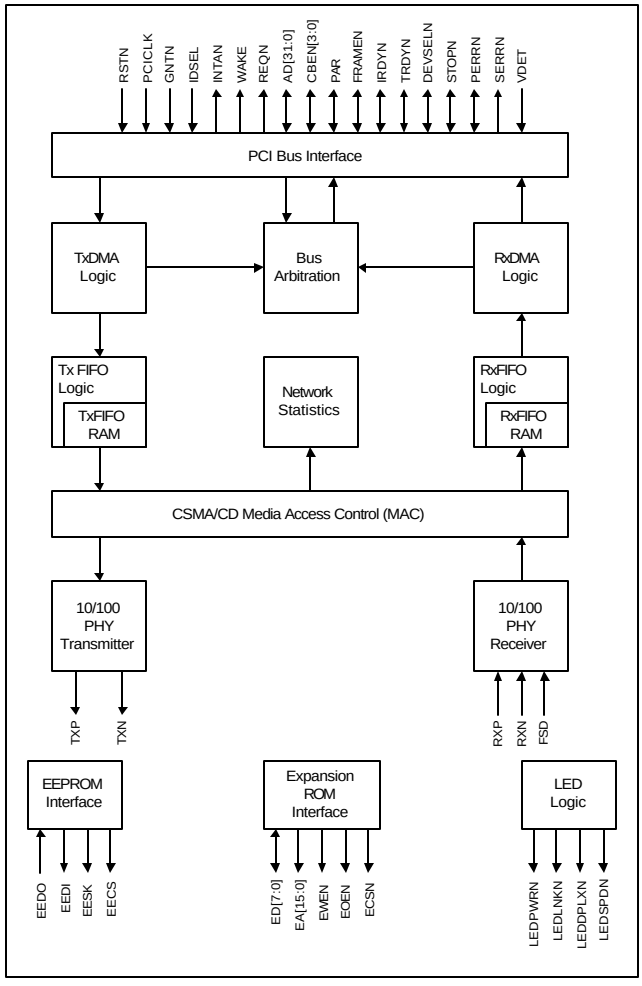
The KS8723 includes a PCI bus interface unit, IEEE 802.3 compliant MAC, transmit and receive FIFO buffers, IEEE 802.3 compliant 100BASE-TX and 100BASE-FX PHY, serial EEPROM interface, expansion ROM interface, and LED drivers.

The KS8723 implements a rich set of control and status registers. Accessible via the PCI interface, these registers provide a host system vis ibility into the features and operating state of the KS8723. Network management statistics are also recorded, and host access to registers of the PHY device are facilitated through the KS8723's PCI interface.

The KS8723 supports features for use in "Green PCs" or systems where control over system power consumption is desired. The KS8723 supports several power down states, and the ability to issue a system "wake event" via reception of unique, user defined Ethernet frames. In addition, the KS8723 can assert a wake event in response to changes in the Ethernet link status.

Highlights

- Single chip 10/100BASE, half or full duplex Ethernet Media Access Controller
- IEEE 802.3 compliant 100BASE-TX PHY
- IEEE 802.3 full duplex flow control
- IEEE 802.3 compliant 100BASE-FX PCS and PMA
- PCI Bus master scatter/gather DMA on any byte boundary
- Full operation with PCI Clock from 12.5 MHz to 33 MHz
- On-chip transmit and receive FIFO buffers
- On-chip LED drivers
- Power management capabilities for ACPI 1.0 compliant systems
- WakeOnLA N support
- Management statistics gathering
- IP multicast receive and filter support using 64 bit hash table
- Receive early interrupt
- Transmit polling
- Auto pad insertion for short packets
- Programmable minimum Inter Packet Gap
- Programmable transmit and receive FIFO watermarks
- On-chip crystal oscillator
- 2.5V CMOS with 3.3V tolerant I/O
- On-chip voltage regulator for 2.5V supply
- 0.25mm technology
- 128-pin PQFP
- Typical 120mA (0.3W) including transmit driver current



KS8723 Block Diagram

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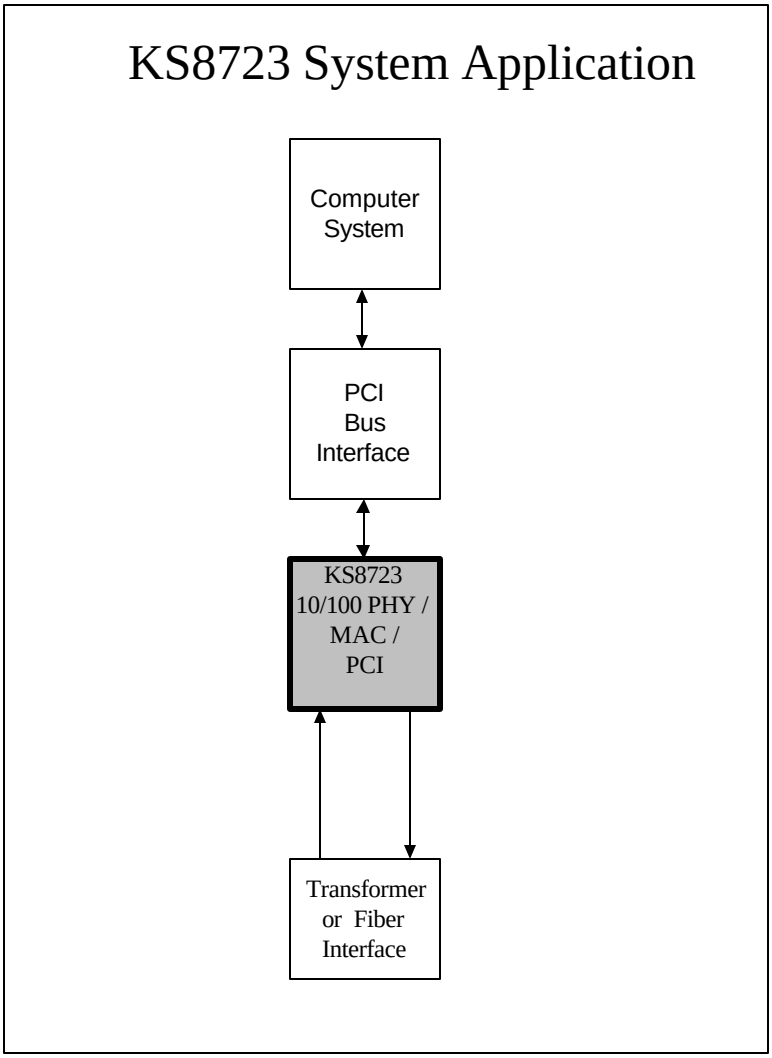
System Level Applications

The KS8723 is designed to easily terminate a 10/100 Ethernet network connection. System access is through a standard PCI interface with transmit and receive DMA engines for added convenience. Also on chip is the physical layer transceiver that helps reduce BOM concerns as well as increasing reliability. As with all Kendin components, the KS8723 exhibits very low power due to advanced physical layer technology.

Drivers are available for Windows 2000/98/95/NT and Linux. The PCI interface is used to program registers, read statistics, transfer receive and transmit data and collect interrupt information. Ample information is supplied for network management and monitoring agents for network wide performance and maintenance functions.

The diagram below illustrates a typical usage of the KS8723 as utilized in a computing device.



Request full datasheet.