

K7A163609A
K7A163209A
K7A161809A

PRELIMINARY

512Kx36/x32 & 1Mx18 Synchronous SRAM

Document Title

512Kx36/x32 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft</u>	<u>Date</u>	<u>Remark</u>
0.0	1. Initial draft		Feb. 23. 2001	Preliminary
0.1	1. Add JTAG Scan Order		May. 10. 2001	Preliminary
0.2	1. Add x32 org and industrial temperature . 2. Add 165FBGA package		Aug. 30. 2001	Preliminary

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512Kx36/x32 & 1Mx18 Synchronous SRAM

16Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7B161825A-Q(H/F)C(I)65/75/85	SB	3.3	6.5/7.5/8.5ns	Q : 100TQFP H : 119BGA F : 165FBGA	C (Commercial Temperature Range)
	K7A161800A-Q(H/F)C(I)16/14	SPB(2E1D)	3.3	167/138MHz		
	K7A161809A-Q(H/F)C(I)25/22/20	SPB(2E1D)	3.3	250/225/200MHz		
	K7A161801A-QC(I)16/14	SPB(2E2D)	3.3	167/138MHz		
	K7A161808A-QC(I)25/22/20	SPB(2E2D)	3.3	250/225/200MHz		
512Kx32	K7B163225A-QC(I)65/75/85	SB	3.3	6.5/7.5/8.5ns		
	K7A163200A-QC(I)16/14	SPB(2E1D)	3.3	167/138MHz		
	K7A163209A-QC(I)25/22/20	SPB(2E1D)	3.3	250/225/200MHz		
	K7A163201A-QC(I)16/14	SPB(2E2D)	3.3	167/138MHz		
	K7A163208A-QC(I)25/22/20	SPB(2E2D)	3.3	250/225/200MHz		
512Kx36	K7B163625A-Q(H/F)C(I)65/75/85	SB	3.3	6.5/7.5/8.5ns		I (Industrial Temperature Range)
	K7A163600A-Q(H/F)C(I)16/14	SPB(2E1D)	3.3	167/138MHz		
	K7A163609A-Q(H/F)C(I)25/22/20	SPB(2E1D)	3.3	250/225/200MHz		
	K7A163601A-QC(I)16/14	SPB(2E2D)	3.3	167/138MHz		
	K7A163608A-QC(I)25/22/20	SPB(2E2D)	3.3	250/225/200MHz		

512Kx36/x32 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V \pm 0.165V / -0.165V$ Power Supply.
- I/O Supply Voltage $3.3V \pm 0.165V / -0.165V$ for 3.3V I/O or $2.5V \pm 0.4V / -0.125V$ for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package)
- 165FBGA(11x15 ball array) with body size of 13mmx15mm.
- Operating in commercial and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.1	ns
Output Enable Access Time	tOE	2.6	2.8	3.1	ns

GENERAL DESCRIPTION

The K7A163609A, K7A163209A and K7A161809A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(32/18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, $\overline{ZZ}$. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

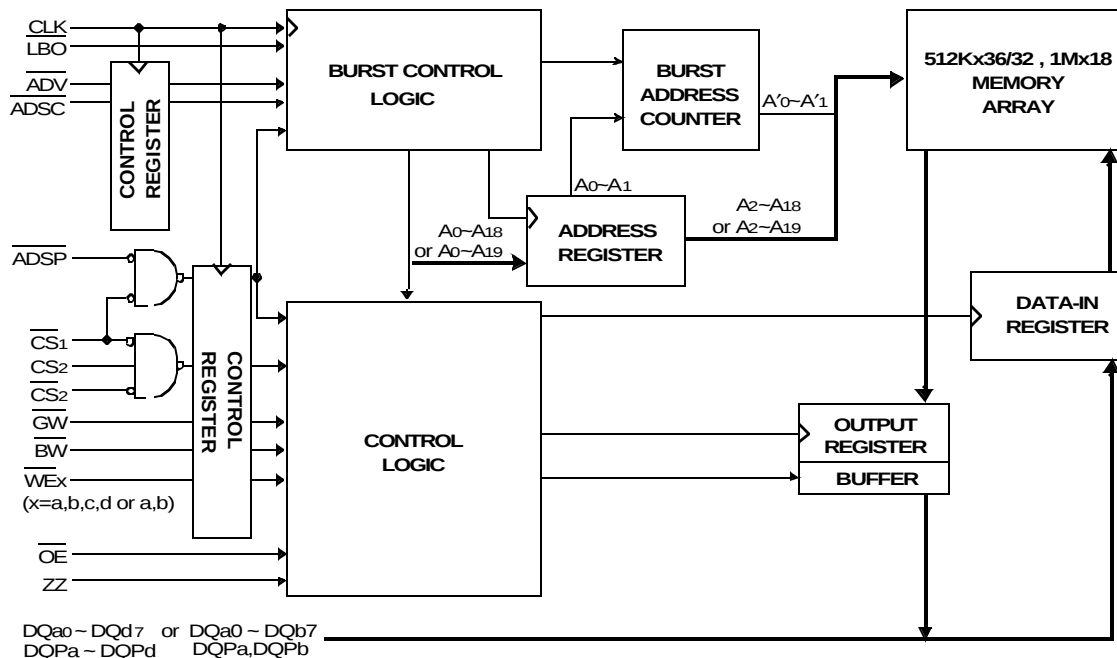
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

$\overline{ZZ}$ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163609A, K7A163209A and K7A161809A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP, 119BGA and 165FBGA package. Multiple power and ground pins are utilized to minimize ground bounce.

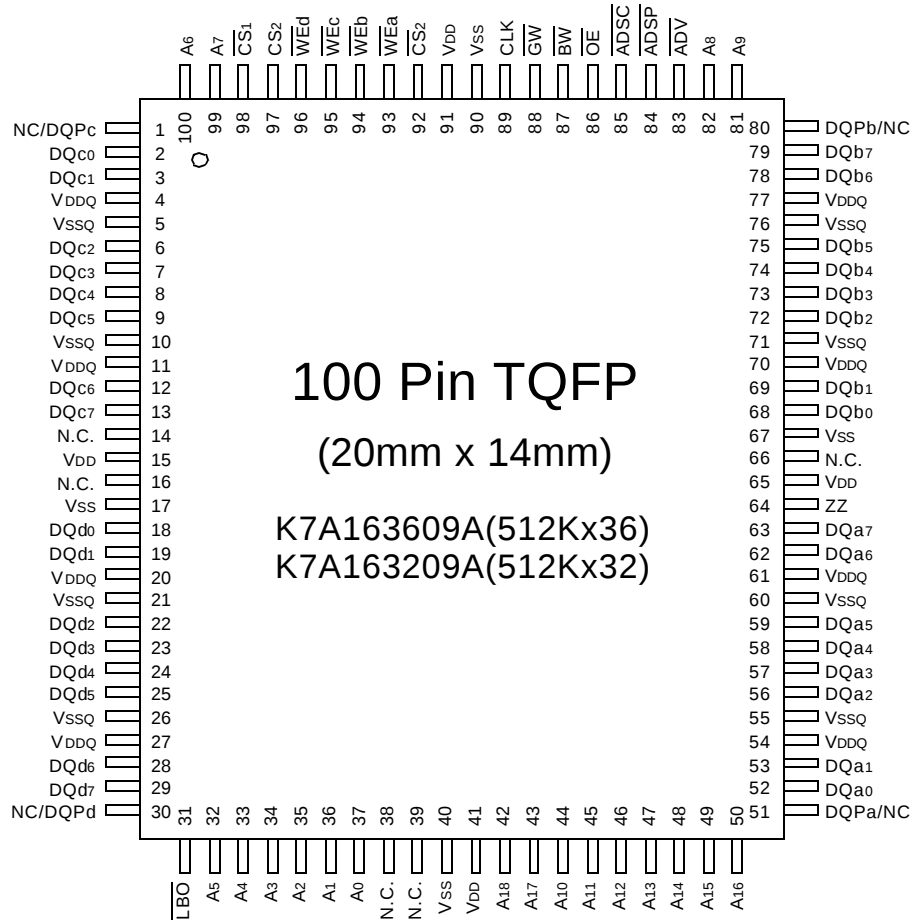
LOGIC BLOCK DIAGRAM



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PIN CONFIGURATION(TOP VIEW)



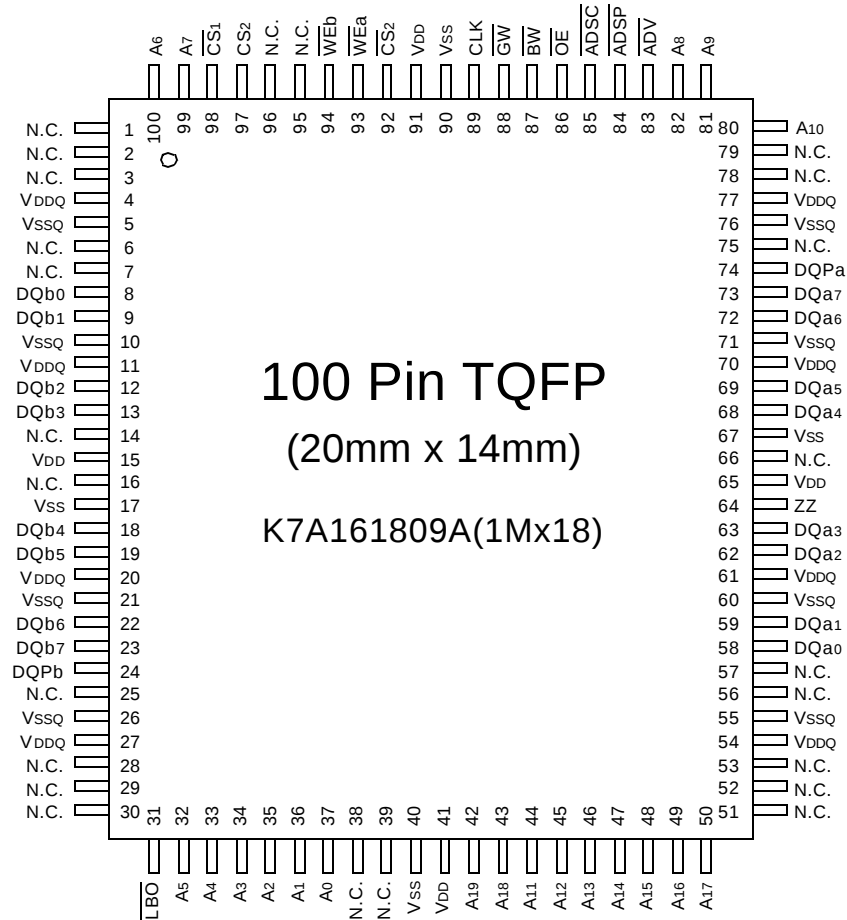
PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42,43,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa0-a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0-b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0-c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0-d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa-Pd or NC		51,80,1,30
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

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PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29 30,38,39,51,52,53,56,57 66,75,78,79,95,96
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85			
CLK	Clock	89			
CS1	Chip Select	98	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73 8,9,12,13,18,19,22,23 74,24
CS2	Chip Select	97	DQb0 ~ b7		
CS2	Chip Select	92	DQPa, Pb		
WEx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A163609A(512Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	ADSP	A	A	VDDQ
B	NC	A	A	ADSC	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	VSS	NC	VSS	DQPb	DQb
E	DQc	DQc	VSS	CS1	VSS	DQb	DQb
F	VDDQ	DQc	VSS	OE	VSS	DQb	VDDQ
G	DQc	DQc	WEc	ADV	WEb	DQb	DQb
H	DQc	DQc	VSS	GW	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	WE d	NC	WEa	DQa	DQa
M	VDDQ	DQd	VSS	BW	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1*	VSS	DQa	DQa
P	DQd	DQPd	VSS	A0*	VSS	DQPa	DQa
R	NC	A	LBO	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ , A ₁	Burst Count Address	VSS	Ground
ADV	Burst Address Advance	N.C.	No Connect
ADSP	Address Status Processor		
ADSC	Address Status Controller		
CLK	Clock	DQa	Data Inputs/Outputs
CS ₁	Chip Select	DQb	Data Inputs/Outputs
WEx	Byte Write Inputs	DQc	Data Inputs/Outputs
(x=a,b,c,d)		DQd	Data Inputs/Outputs
		DQPa~Pd	Data Inputs/Outputs
OE	Output Enable	VDDQ	Output Power Supply
GW	Global Write Enable		(2.5V or 3.3V)
BW	Byte Write Enable		
ZZ	Power Down Input		
LBO	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

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512Kx36/x32 & 1Mx18 Synchronous SRAM

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A161809A(1Mx18)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	$\overline{\text{CS}}_1$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{WE}}_b$	$\overline{\text{ADV}}$	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{\text{GW}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{\text{WE}}_a$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{BW}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A ₁ *	VSS	DQa	NC
P	NC	DQPb	VSS	A ₀ *	VSS	NC	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{\text{CS}}_1$	Chip Select	DQb	Data Inputs/Outputs
$\overline{\text{WE}}_x$	Byte Write Inputs	DQPa-Pb	Data Inputs/Output
(x=a,b)		VDDQ	Output Power Supply (2.5V or 3.3V)
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable		
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

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165-PIN FGPA PACKAGE CONFIGURATIONS(TOP VIEW)

K7A163609A(512Kx36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CS1}}$	$\overline{\text{WEc}}$	$\overline{\text{WEb}}$	$\overline{\text{CS2}}$	$\overline{\text{BW}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	A	NC
B	NC	A	CS2	$\overline{\text{WEd}}$	$\overline{\text{WEa}}$	CLK	$\overline{\text{GW}}$	$\overline{\text{OE}}$	$\overline{\text{ADSP}}$	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	A	VSS	VSS	VDDQ	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	$\overline{\text{LBO}}$	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note : * A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A0, A1	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller		
CLK	Clock	DQa	Data Inputs/Outputs
CS1	Chip Select	DQb	Data Inputs/Outputs
WE _x	Byte Write Inputs	DQc	Data Inputs/Outputs
(x=a,b,c,d)		DQd	Data Inputs/Outputs
		DQPa~Pd	Data Inputs/Output
$\overline{\text{OE}}$	Output Enable	VDDQ	Output Power Supply
$\overline{\text{GW}}$	Global Write Enable		(2.5V or 3.3V)
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

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512Kx36/x32 & 1Mx18 Synchronous SRAM

165-PIN FGPA PACKAGE CONFIGURATIONS(TOP VIEW)

K7A161809A(1Mx18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS}1$	$\overline{WE}b$	NC	$\overline{CS}2$	$\overline{BW}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CS2	NC	$\overline{WE}a$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPa	NC	VDDQ	VSS	NC	A	VSS	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	$\overline{LBO}$	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note : * A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A0,A1	Burst Count Address	VSS	Ground
$\overline{ADV}$	Burst Address Advance	N.C.	No Connect
$\overline{ADSP}$	Address Status Processor		
$\overline{ADSC}$	Address Status Controller		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{CS}1$	Chip Select	DQb	Data Inputs/Outputs
$\overline{WE}x$	Byte Write Inputs	DQPa-Pb	Data Inputs/Output
(x=a,b)			
$\overline{OE}$	Output Enable	VDDQ	Output Power Supply
$\overline{GW}$	Global Write Enable		(2.5V or 3.3V)
$\overline{BW}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7A163609A, K7A163209A and K7A161809A are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When $\overline{ZZ}$ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2cycles of wake up time. $\overline{ZZ}$ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WEx}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of $\overline{CLK}$, are carried to the Data-out buffer by the next positive edge of $\overline{CLK}$. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WEx}$ are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$ (regardless of $\overline{BW}$ and $\overline{WEx}$), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WEx}$ when $\overline{GW}$ is high.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WEx}$. $\overline{WEx}$ are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WEx}$ are sampled Low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WEx}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WEx}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals ($\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$ or $\overline{WEd}$) sampled low. The $\overline{WEa}$ control $\overline{DQa0} \sim \overline{DQa7}$ and $\overline{DQPa}$, $\overline{WEb}$ controls $\overline{DQb0} \sim \overline{DQb7}$ and $\overline{DQPb}$, $\overline{WEc}$ controls $\overline{DQc0} \sim \overline{DQc7}$ and $\overline{DQPC}$, and $\overline{WEd}$ control $\overline{DQd0} \sim \overline{DQd7}$ and $\overline{DQPD}$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.

$\overline{WEx}$ are sampled on the same clock edge that sampled $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{\text{LBO}}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

ASYNCHRONOUS TRUTH TABLE

Operation	$\overline{ZZ}$	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. $\overline{ZZ}$ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE(x36 / x32)

$\overline{GW}$	$\overline{BW}$	$\overline{WE}_a$	$\overline{WE}_b$	$\overline{WE}_c$	$\overline{WE}_d$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WE}_a$	$\overline{WE}_b$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V _{DD} Supply Relative to V _{SS}		V _{DD}	-0.3 to 4.6	V
Voltage on V _{DDQ} Supply Relative to V _{SS}		V _{DDQ}	V _{DD}	V
Voltage on Input Pin Relative to V _{SS}		V _{IN}	-0.3 to V _{DD} +0.3	V
Voltage on I/O Pin Relative to V _{SS}		V _{IO}	-0.3 to V _{DDQ} +0.3	V
Power Dissipation		P _D	1.6	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _{OPR}	0 to 70	°C
	Industrial	T _{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T _{BIAS}	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	3.135	3.3	3.465	V
Ground	V _{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	2.375	2.5	2.9	V
Ground	V _{SS}	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

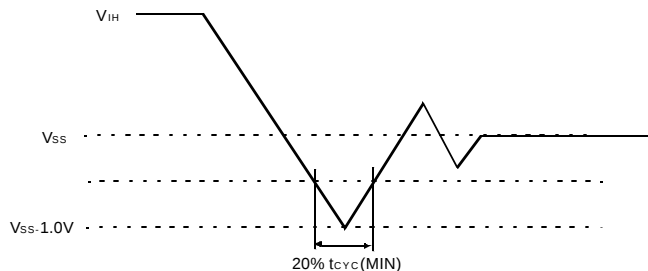
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I _{IL}	$V_{DD} = \text{Max}$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	I _{OL}	Output Disabled, $V_{OUT}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ≤V _{IL} , Cycle Time ≥ t _{CYC} Min	-25	-	440	mA 1,2
			-22	-	400	
			-20	-	370	
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ≤V _{IL} , f=Max, All Inputs≤0.2V or ≥ V _{DD} -0.2V	-25	-	120	mA
			-22	-	110	
			-20	-	100	
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	70	mA	
	I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ≥V _{DD} -0.2V, f=Max, All Inputs≤V _{IL} or ≥V _{IH}	-	60	mA	
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V	
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V	
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V	
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V	
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V _{IH}		2.0	V _{DD} +0.3**	V	3
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V _{IH}		1.7	V _{DD} +0.3**	V	3

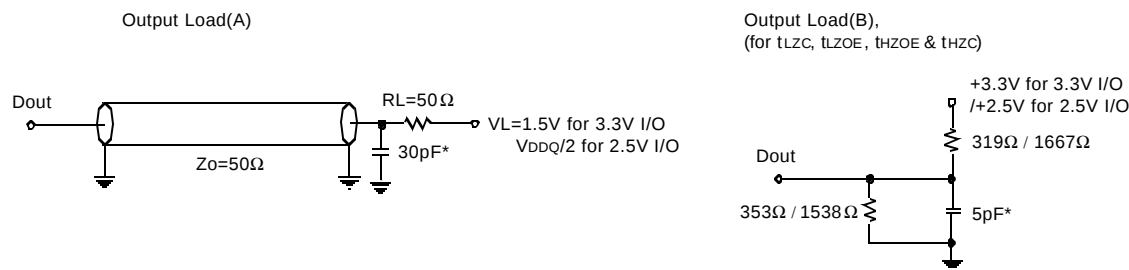
Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.



TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V _{DDQ} /2
Output Load	See Fig. 1



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS (VDD=3.3V+0.165V/-0.165V, TA=0°C to +70°C)

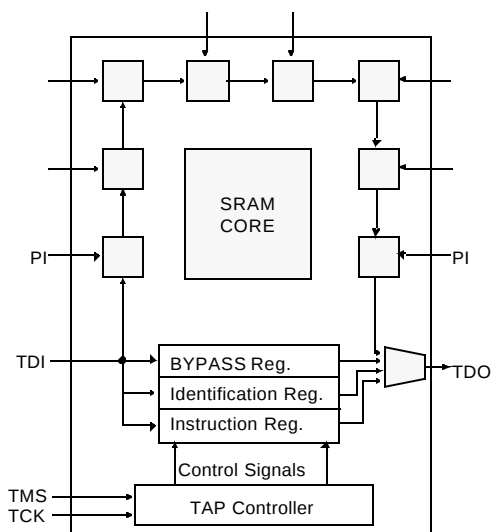
PARAMETER	Symbol	-25		-22		-20		UNIT
		MIN	MAX	Min	Max	MIN	MAX	
Cycle Time	t _{CYC}	4.0	-	4.4	-	5.0	-	ns
Clock Access Time	t _{CD}	-	2.6	-	2.8	-	3.1	ns
Output Enable to Data Valid	t _{OE}	-	2.6	-	2.8	-	3.1	ns
Clock High to Output Low-Z	t _{LZC}	0	-	0	-	0	-	ns
Output Hold from Clock High	t _{OH}	0.8	-	1.0	-	1.0	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	2.6	-	2.8	-	3.0	ns
Clock High to Output High-Z	t _{HZC}	0.8	2.6	1.0	2.8	1.0	3.0	ns
Clock High Pulse Width	t _{CH}	1.7	-	1.8	-	2.0	-	ns
Clock Low Pulse Width	t _{CL}	1.7	-	1.8	-	2.0	-	ns
Address Setup to Clock High	t _{AS}	1.2	-	1.4	-	1.4	-	ns
Address Status Setup to Clock High	t _{SS}	1.2	-	1.4	-	1.4	-	ns
Data Setup to Clock High	t _{DS}	1.2	-	1.4	-	1.4	-	ns
Write Setup to Clock High (GW, BW, WE _x)	t _{WS}	1.2	-	1.4	-	1.4	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.2	-	1.4	-	1.4	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.2	-	1.4	-	1.4	-	ns
Address Hold from Clock High	t _{AH}	0.3	-	0.4	-	0.4	-	ns
Address Status Hold from Clock High	t _{SH}	0.3	-	0.4	-	0.4	-	ns
Data Hold from Clock High	t _{DH}	0.3	-	0.4	-	0.4	-	ns
Write Hold from Clock High (GW, BW, WE _x)	t _{WH}	0.3	-	0.4	-	0.4	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.3	-	0.4	-	0.4	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.3	-	0.4	-	0.4	-	ns
ZZ High to Power Down	t _{PDS}	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{ss} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



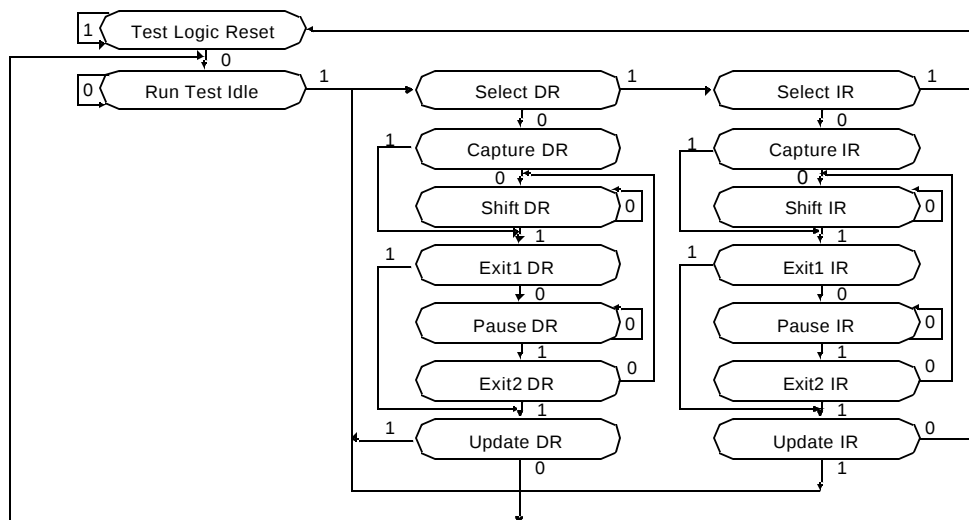
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{ss} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512Kx36	3 bits	1 bits	32 bits	75 bits
1Mx18	3 bits	1 bits	32 bits	75 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
512Kx36	0000	00111 00100	XXXXXX	00001001110	1
1Mx18	0000	01000 00011	XXXXXX	00001001110	1

119BGA BOUNDARY SCAN EXIT ORDER(x36)

1	2T	NC		CLK	4K	39
2	1R	NC		ADV	4G	40
3	4T	A		ADSC	4B	41
4	4H	GW		ADSP	4A	42
5	5R	NC		BW	4M	43
6	5T	A		WE _c	3G	44
7	5L	WE _a		A	3B	45
8	7R	NC		A	3A	46
9	6R	A		A	2B	47
10	7T	ZZ		CS ₁	4E	48
11	6P	DQPa		A	3C	49
12	7N	DQa		A	2C	50
13	6M	DQa		A	2A	51
14	7L	DQa		DQPc	2D	52
15	6K	DQa		DQc	1E	53
16	7P	DQa		DQc	2F	54
17	6N	DQa		DQc	1G	55
18	6L	DQa		DQc	2H	56
19	7K	DQa		DQc	1D	57
20	5J	NC		DQc	2E	58
21	6H	DQb		DQc	2G	59
22	7G	DQb		DQc	1H	60
23	6F	DQb		DQd	2K	61
24	7E	DQb		DQd	1L	62
25	7D	DQb		DQd	2M	63
26	7H	DQb		DQd	1N	64
27	6G	DQb		DQd	1P	65
28	6E	DQb		DQd	1K	66
29	6D	DQPb		DQd	2L	67
30	7B	NC		DQd	2N	68
31	6C	A		DQPd	2P	69
32	5C	A		WE _d	3L	70
33	6A	A		LBO	3R	71
34	5B	A		A	2R	72
35	5A	A		A	3T	73
36	4F	OE		A1	4N	74
37	5G	WE _b		A0	4P	75
38	6B	A				

119BGA BOUNDARY SCAN EXIT ORDER(x18)

1	2T	A		CLK	4K	39
2	1R	NC		ADV	4G	40
3	6T	A		ADSC	4B	41
4	4H	GW		ADSP	4A	42
5	5R	NC		BW	4M	43
6	5T	A		WE _b	3G	44
7	5L	WE _a		A	3B	45
8	7R	NC		A	3A	46
9	6R	A		A	2B	47
10	7T	ZZ		CS ₁	4E	48
11	6P	NC		A	3C	49
12	7N	NC		A	2C	50
13	6M	NC		A	2A	51
14	7L	NC		NC	2D	52
15	6K	NC		NC	1E	53
16	7P	DQa		NC	2F	54
17	6N	DQa		NC	1G	55
18	6L	DQa		NC	2H	56
19	7K	DQa		DQb	1D	57
20	5J	NC		DQb	2E	58
21	6H	DQa		DQb	2G	59
22	7G	DQa		DQb	1H	60
23	6F	DQa		DQb	2K	61
24	7E	DQa		DQb	1L	62
25	6D	DQPa		DQb	2M	63
26	7H	NC		DQb	1N	64
27	6G	NC		DQPb	2P	65
28	6E	NC		NC	1K	66
29	7D	NC		NC	2L	67
30	7B	NC		NC	2N	68
31	6C	A		NC	1P	69
32	5C	A		NC	3L	70
33	6A	A		LBO	3R	71
34	5B	A		A	2R	72
35	5A	A		A	3T	73
36	4F	OE		A1	4N	74
37	5G	NC		A0	4P	75
38	6B	A				

NOTE. NC ; Don't Care

K7A163609A
K7A163209A
K7A161809A

PRELIMINARY

512Kx36/x32 & 1Mx18 Synchronous SRAM

165FBGA BOUNDARY SCAN EXIT ORDER(x36)

1	1R	LBO		CLK	6B	39
2	6N	A		NC	11B	40
3	11P	A		NC	1A	41
4	8P	A		CS2	6A	42
5	8R	A		WEa	5B	43
6	9R	A		WEb	5A	44
7	9P	A		WEc	4A	45
8	10P	A		WEd	4B	46
9	10R	A		CS2	3B	47
10	11R	A		CS1	3A	48
11	11H	ZZ		A	2A	49
12	11N	DQa		A	2B	50
13	11M	DQa		NC	1B	51
14	11L	DQa		DQc	1C	52
15	11K	DQa		DQc	1D	53
16	11J	DQa		DQc	1E	54
17	10M	DQa		DQc	1F	55
18	10L	DQa		DQc	1G	56
19	10K	DQa		DQc	2D	57
20	10J	DQa		DQc	2E	58
21	11G	DQb		DQc	2F	59
22	11F	DQb		DQc	2G	60
23	11E	DQb		DQd	1J	61
24	11D	DQb		DQd	1K	62
25	10G	DQb		DQd	1L	63
26	10F	DQb		DQd	1M	64
27	10E	DQb		DQd	2J	65
28	10D	DQb		DQd	2K	66
29	11C	DQb		DQd	2L	67
30	11A	NC		DQd	2M	68
31	10A	A		DQd	1N	69
32	10B	A		A	3P	70
33	9A	ADV		A	3R	71
34	9B	ADSP		A	4R	72
35	8A	ADSC		A	4P	73
36	8B	OE		A1	6P	74
37	7A	BW		A0	6R	75
38	7B	GW				

165FBGA BOUNDARY SCAN EXIT ORDER(x18)

1	1R	LBO		CLK	6B	39
2	6N	A		NC	11B	40
3	11P	A		NC	1A	41
4	8P	A		CS2	6A	42
5	8R	A		WEa	5B	43
6	9R	A		NC	5A	44
7	9P	A		WEb	4A	45
8	10P	A		NC	4B	46
9	10R	A		CS2	3B	47
10	11R	A		CS1	3A	48
11	11H	ZZ		A	2A	49
12	11N	NC		A	2B	50
13	11M	NC		NC	1B	51
14	11L	NC		NC	1C	52
15	11K	NC		NC	1D	53
16	11J	NC		NC	1E	54
17	10M	DQa		NC	1F	55
18	10L	DQa		NC	1G	56
19	10K	DQa		DQb	2D	57
20	10J	DQa		DQb	2E	58
21	11G	DQa		DQb	2F	59
22	11F	DQa		DQb	2G	60
23	11E	DQa		DQb	1J	61
24	11D	DQa		DQb	1K	62
25	11C	DQa		DQb	1L	63
26	10F	NC		DQb	1M	64
27	10E	NC		DQb	1N	65
28	10D	NC		NC	2K	66
29	10G	NC		NC	2L	67
30	11A	A		NC	2M	68
31	10A	A		NC	2J	69
32	10B	A		A	3P	70
33	9A	ADV		A	3R	71
34	9B	ADSP		A	4R	72
35	8A	ADSC		A	4P	73
36	8B	OE		A1	6P	74
37	7A	BW		A0	6R	75
38	7B	GW				

NOTE, NC ; Don't Care

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O / 2.5V I/O)	V _{IH}	2.0 / 1.7	-	V _{DD} +0.3	V	1
Input Low Level (3.3V I/O / 2.5V I/O)	V _{IL}	-0.3	-	0.8 / 0.7	V	
Output High Voltage(3.3V I/O / 2.5V I/O)	V _{OH}	2.4 / 2.0	-	-	V	
Output Low Voltage(3.3V I/O / 2.5V I/O)	V _{OL}	-	-	0.4 / 0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.

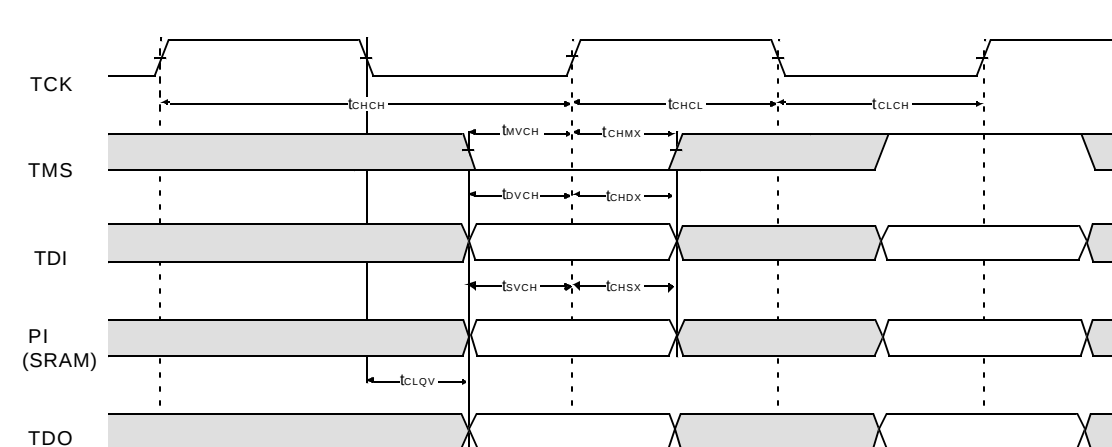
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level(3.3V I/O , 2.5V I/O)	V _{IH} /V _{IL}	3.0/0 , 2.5/0	V	
Input Rise/Fall Time(3.3V I/O , 2.5V I/O)	TR/TF	1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

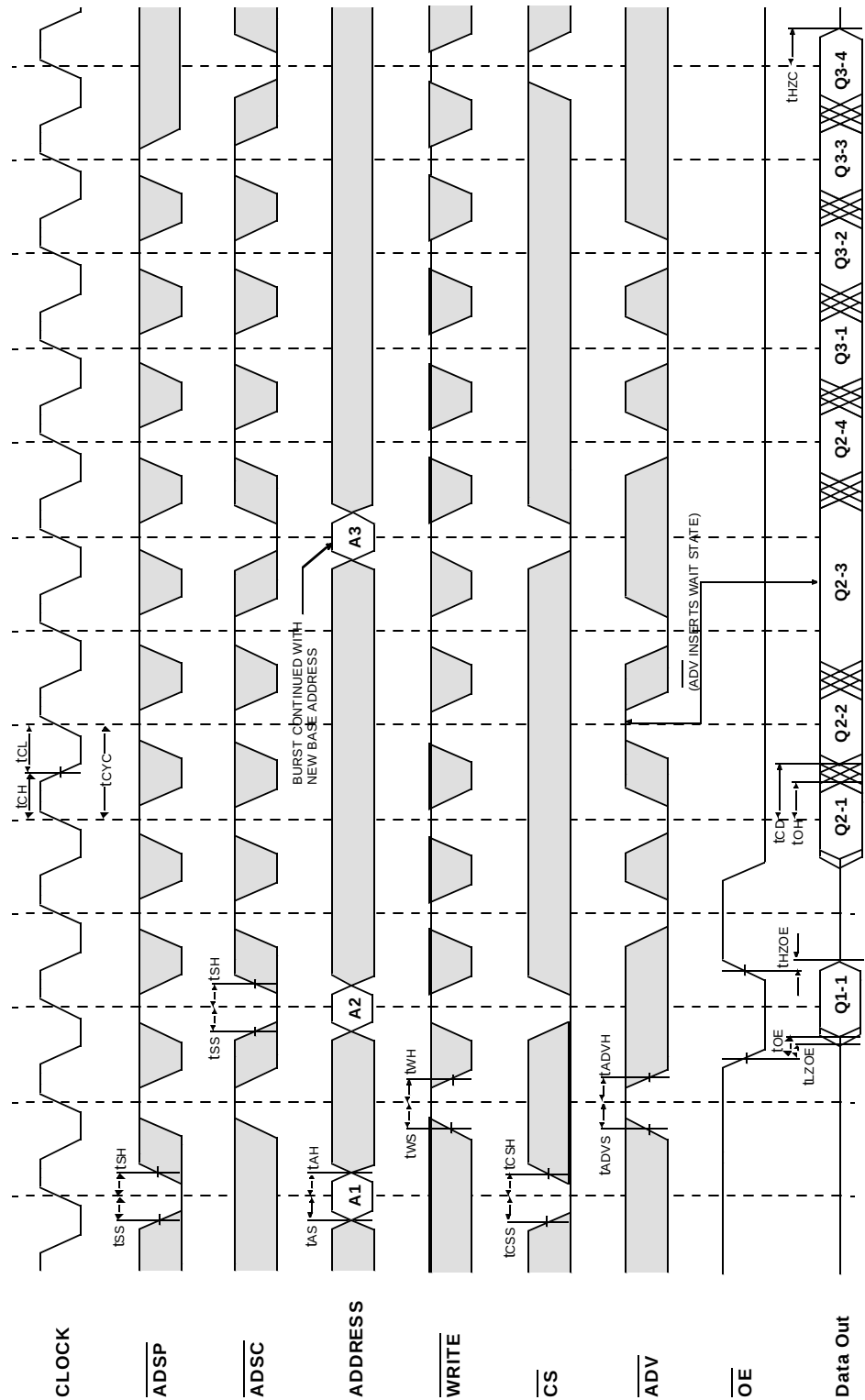
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



TIMING WAVEFORM OF READ CYCLE



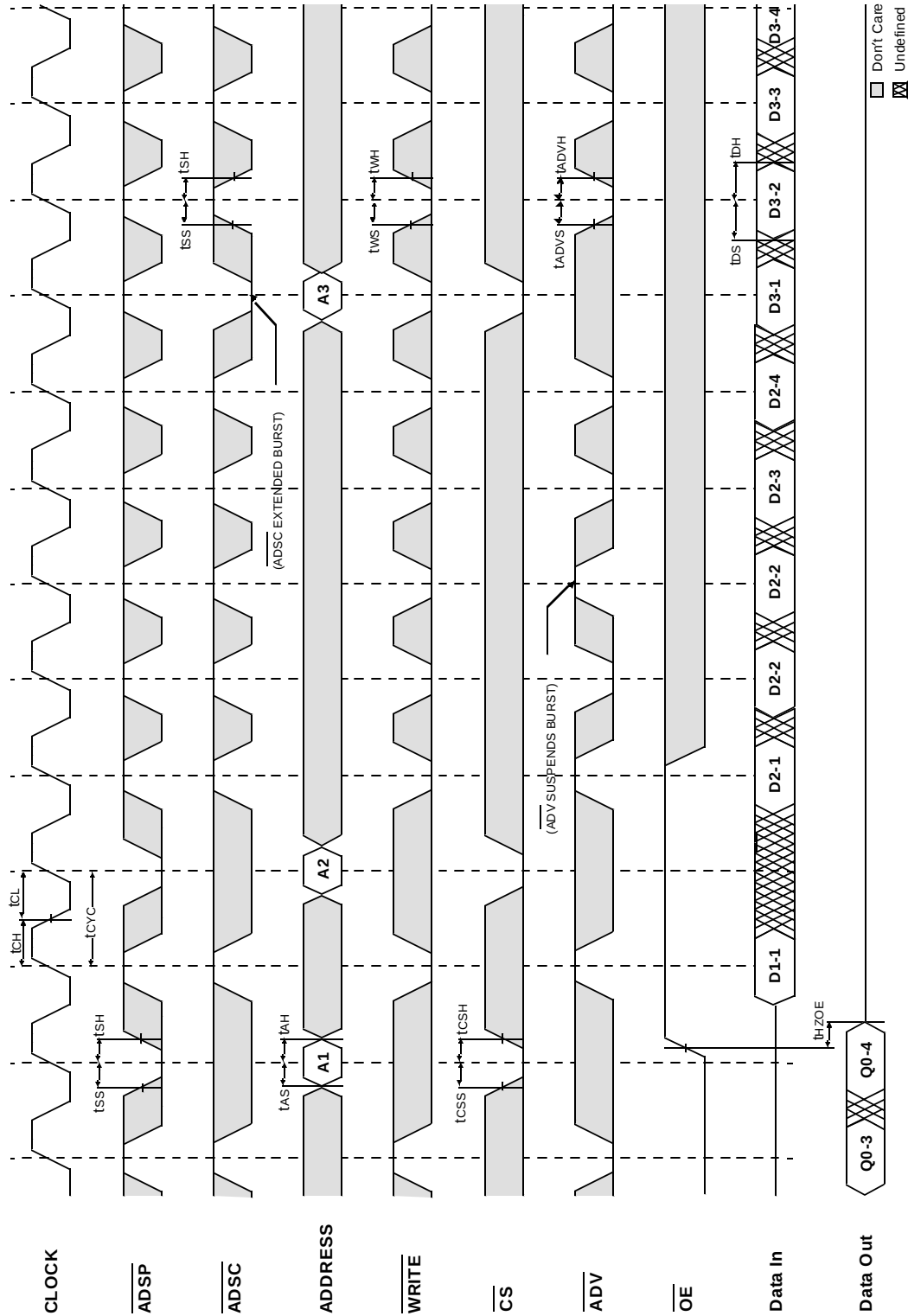
NOTES : $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{GW}} = \text{L}$, or $\overline{\text{GW}} = \text{H}$, $\overline{\text{BW}} = \text{L}$, $\overline{\text{WEX}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{L}$

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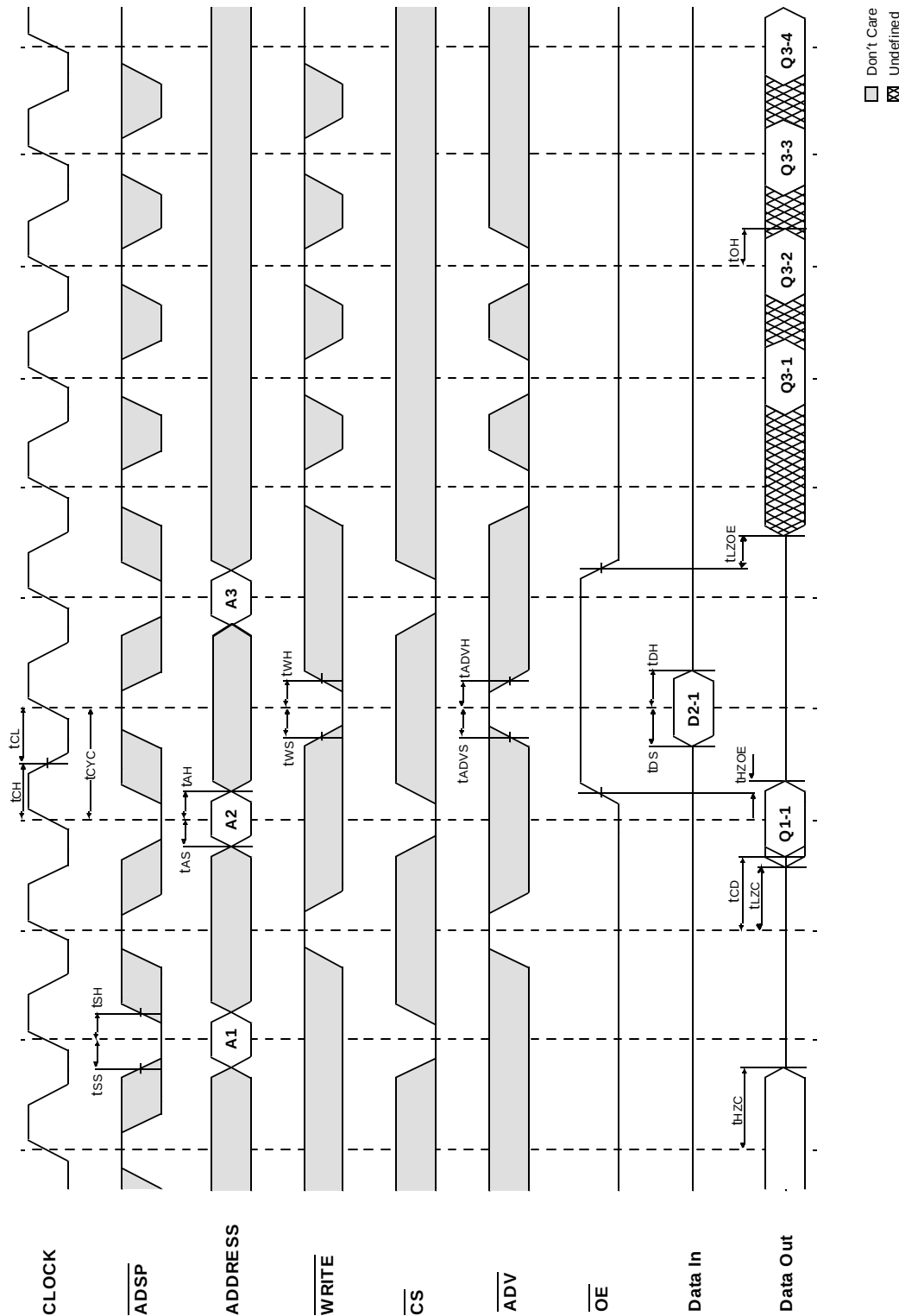
512Kx36/x32 & 1Mx18 Synchronous SRAM

PRELIMINARY

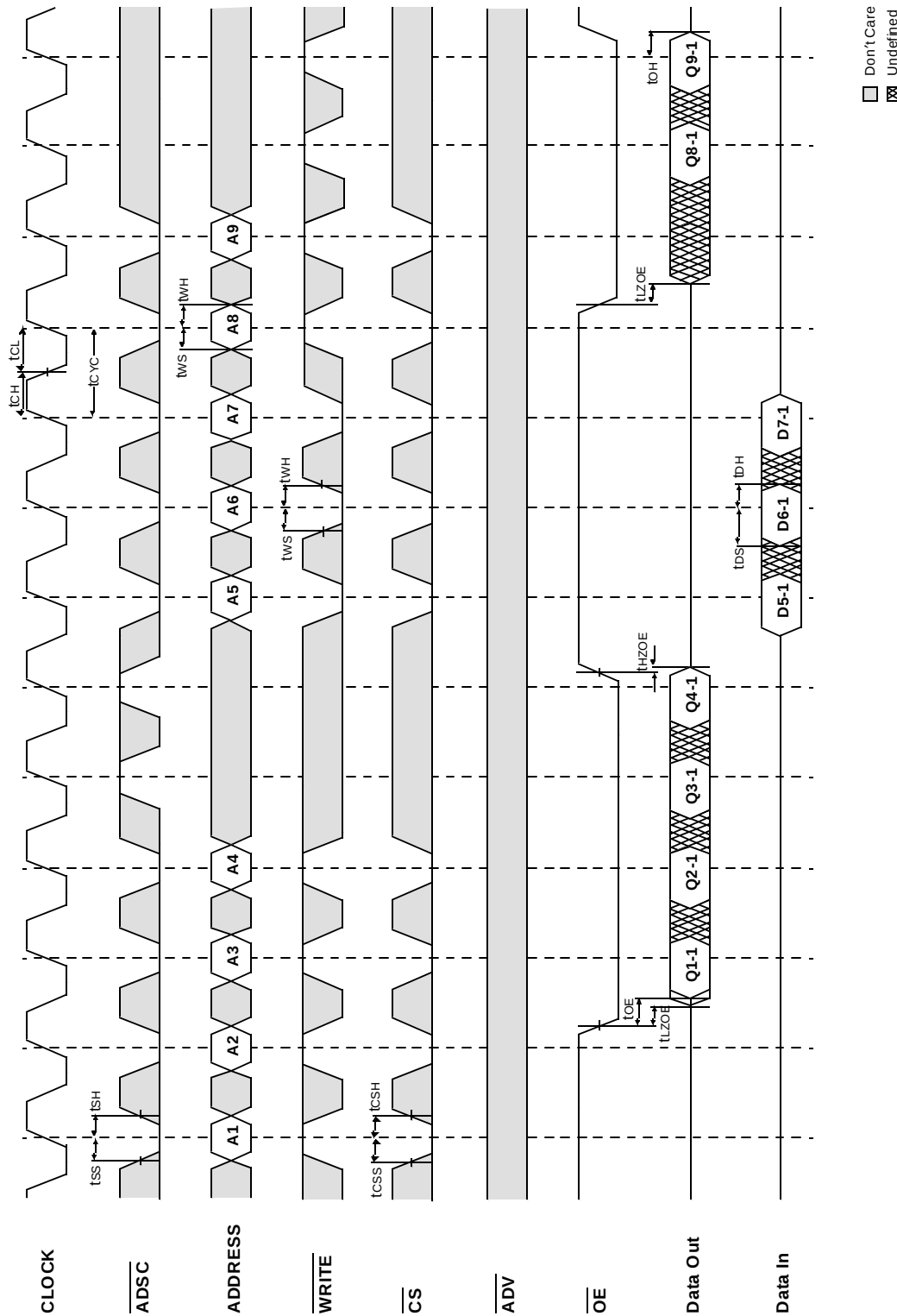
TIMING WAVEFORM OF WRTE CYCLE



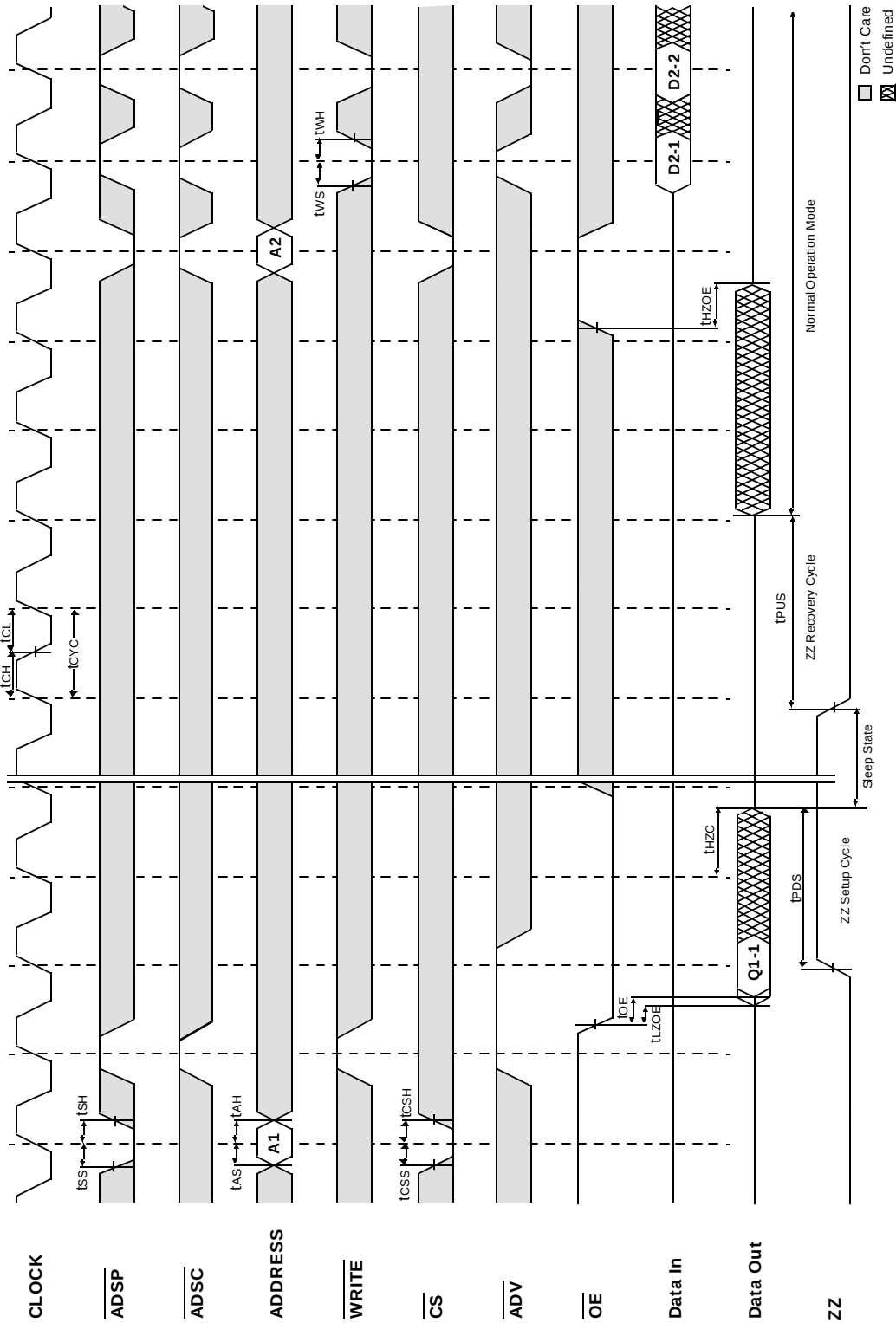
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED , ADSC=HIGH)



TIMING WAVEFORM OF SINGLE READWRITE CYCLE(ADSC CONTROLLED , ADSP=HIGH)



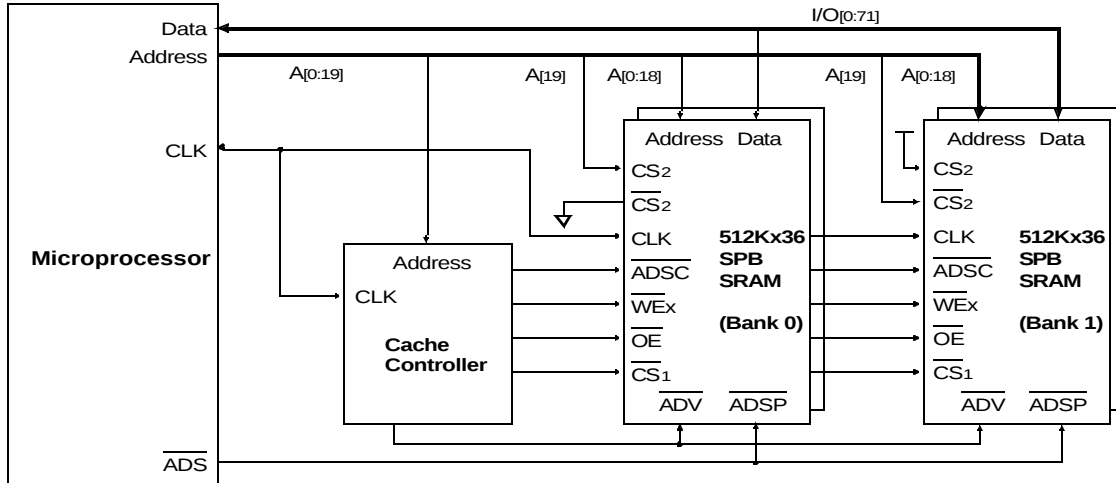
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

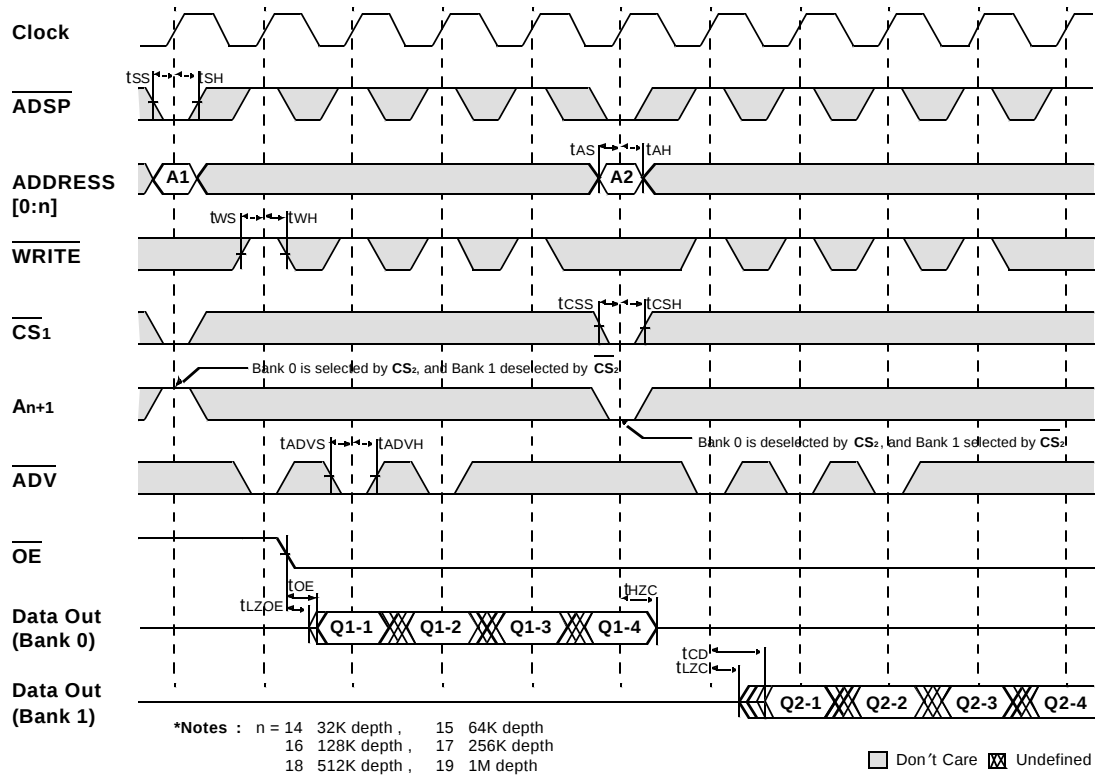
DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

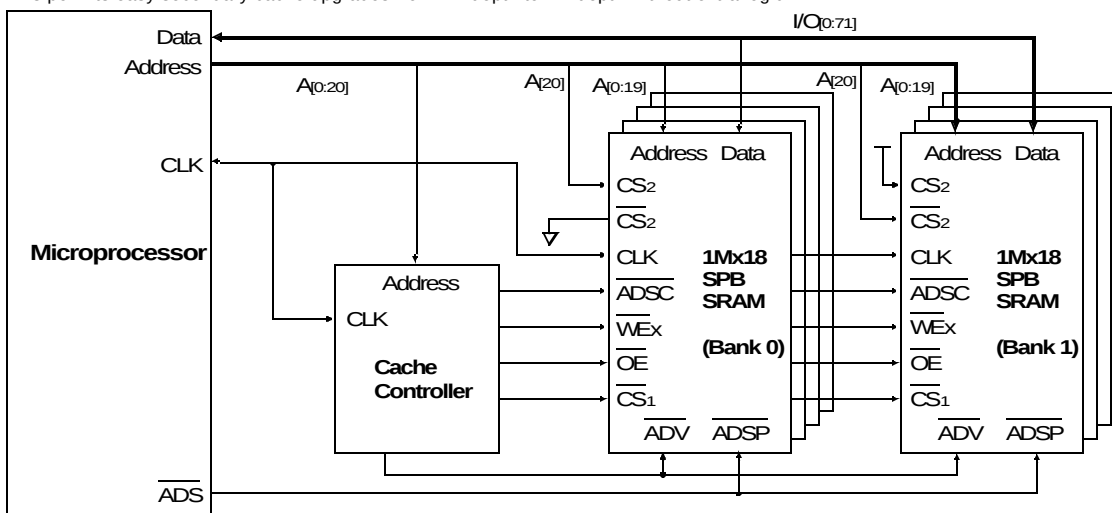
(ADSP CONTROLLED, ADSC=HIGH)



APPLICATION INFORMATION

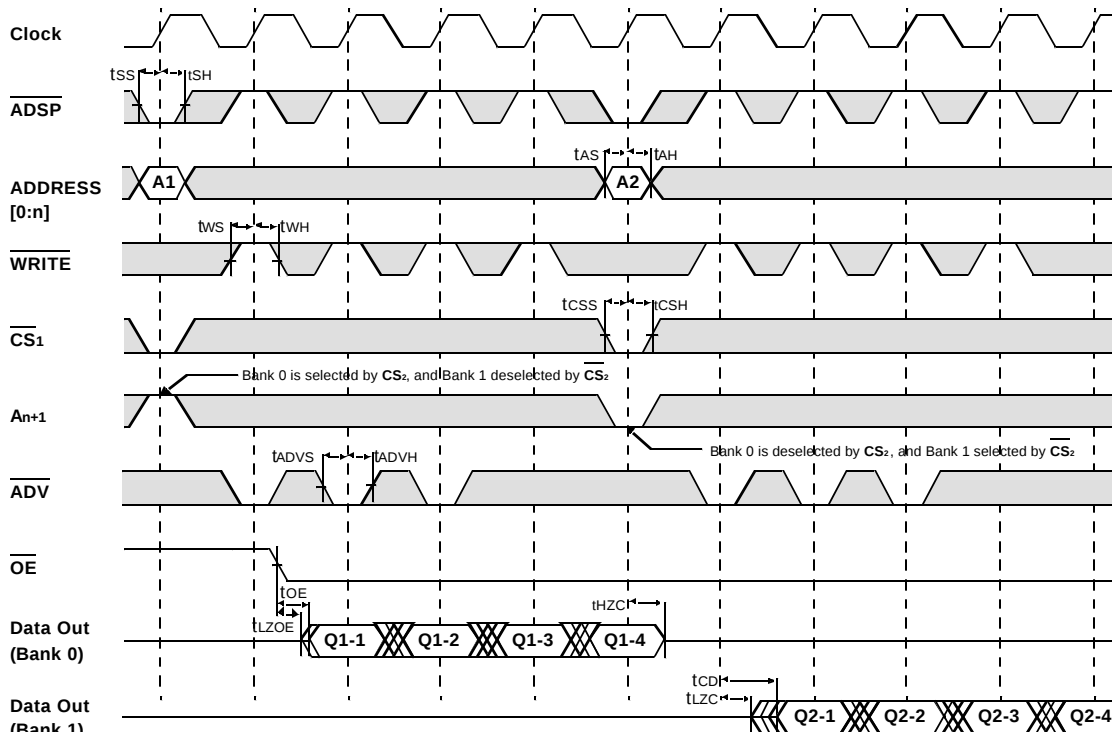
DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



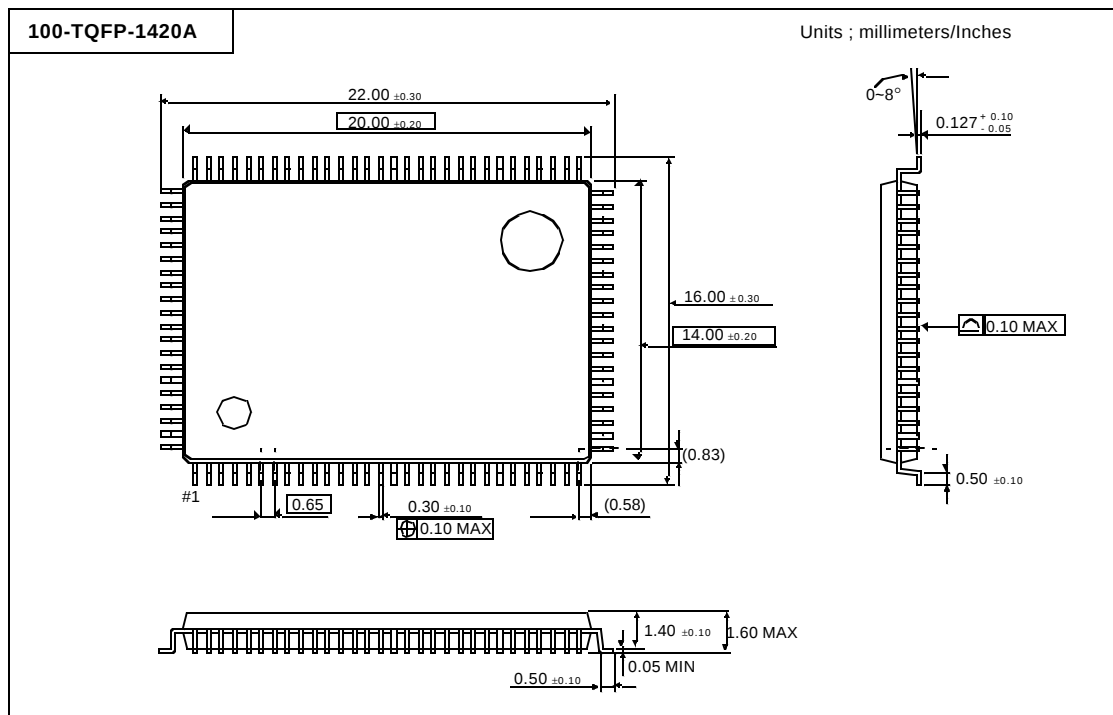
*Notes : n = 14 32K depth, 15 64K depth
16 128K depth, 17 256K depth
18 512K depth, 19 1M depth
20 2M depth

⊗ Undefined □ Don't Care

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PRELIMINARY
512Kx36/x32 & 1Mx18 Synchronous SRAM

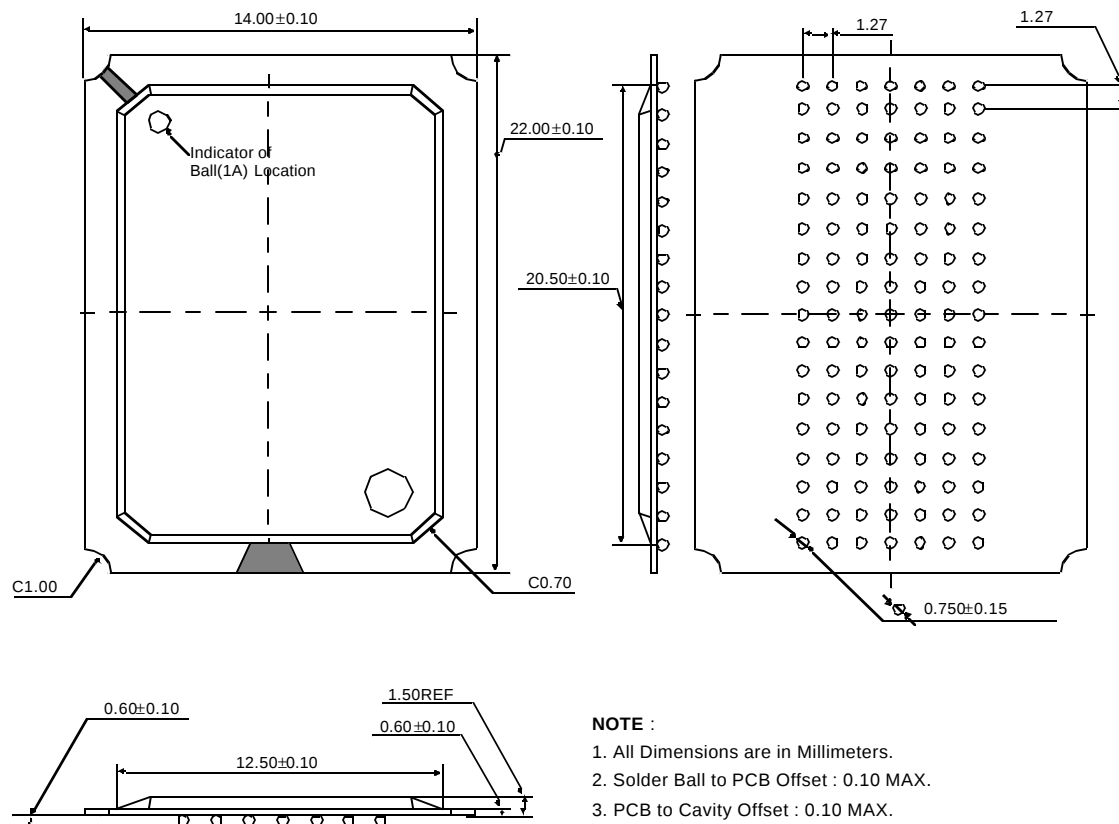
PACKAGE DIMENSIONS



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PRELIMINARY
512Kx36/x32 & 1Mx18 Synchronous SRAM

119 BGA PACKAGE DIMENSIONS

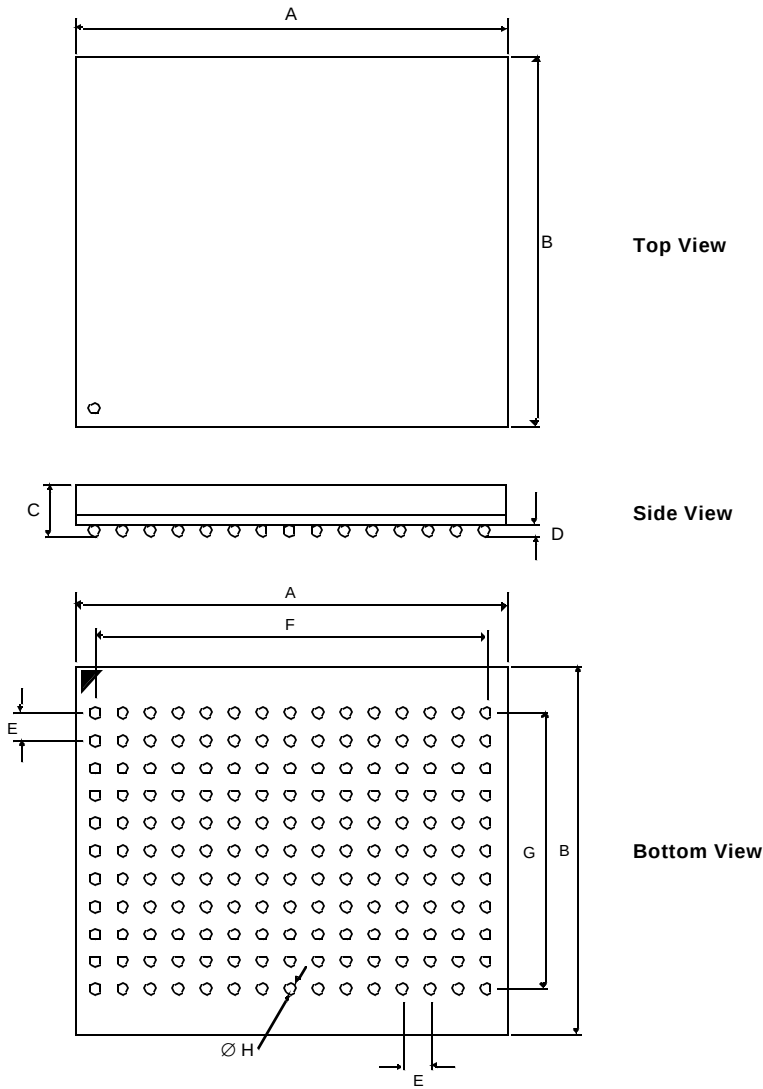


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PRELIMINARY
512Kx36/x32 & 1Mx18 Synchronous SRAM

165 FBGA PACKAGE DIMENSIONS

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	15 ± 0.1	mm		E	1.0	mm	
B	13 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.45 ± 0.05	mm	