1 PRODUCT OVERVIEW

SAM87 PRODUCT FAMILY

Samsung's SAM87 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture
— Selectable CPU clock sources
— Release by interrupt of Idle and Stop power-down modes
— Built-in basic timer circuit with watchdog function

KS88C9408 MICROCONTROLLER

The KS88C9408 single-chip CMOS microcontroller is specially designed and packaged for “smart card” applications.

The SAM87 CPU architecture supports Stop and Idle power-down modes for reduced power consumption. To increase the general-purpose register space, the physical internal register file is logically expanded.

The KS88C9408 has 16-Kbyte of program memory (ROM), 8-Kbyte of data memory (EEPROM), 272-byte general-purpose register file and 256 bytes data buffer (SRAM). The following peripherals are integrated on-chip:

- One 8-bit basic timer for internal reset and watchdog functions
- One 16-bit random number generator
- Asynchronous serial I/O interface (half-duplex) with selectable transmission baud rates
- EEPROM write inhibit features for data security

Data can be loaded into the EEPROM in units ranging from one byte to 32 bytes. A typical EEPROM erase or write operation takes 1.5 milliseconds.

An up to 32 bytes area of the EEPROM can be used as chip and card information area.

A simple yet effective hardware-level security feature based on voltage and frequency range detection circuits keeps data stored in EEPROM.

The KS88C9408’s 8-pin COB package and its serial I/O interface are fully compliant with ISO standards 7816, respectively.

FEATURES

CPU

- 8-bit architecture CPU in CMOS technology (SAM87 core)
- 78 instructions including multiply and divide
- 1 interrupt source
- Power down modes control

Memory

- 15-Kbyte for user application program and 1-Kbyte for built-in subroutine (kernel)
- 256-byte Static RAM
- 272-byte for general-purpose register file

EEPROM

- 8-Kbyte EEPROM as data memory
- 1 to 32 bytes multi-byte write and erase
- 1.5 ms fast erase or write time
- More than 100,000 erase/write cycles
- Greater than 10 years data retention

Serial I/O Interface (hardware)

- Asynchronous half-duplex character transmission serial interface (conforms to ISO standards 7816-3)
- Data transfer rates:
  external 9.6, 19.2, or 38.4-Kbps at 3.57MHz external clock
- Software(kernel) control

Security

- Secure (non-visible) ROM coding
- 32-Byte security PROM
- Unique serial number for each chip
- Reset operation is selective if abnormal voltage or frequency is detected

Random Number Generator

- One 16-bit random number generator for security key generation
- Start and Stop control

Basic Timer

- One 8-bit basic timer for internal reset release and watchdog timer functions

Reset

- Power-on reset and external reset operation

Others

- Single Power Supply : 2.7 V to 5.5 V
- Operating Frequency range : 1 – 5 MHz
- Operating Temperature range : -25°C to +70°C

BLOCK DIAGRAM

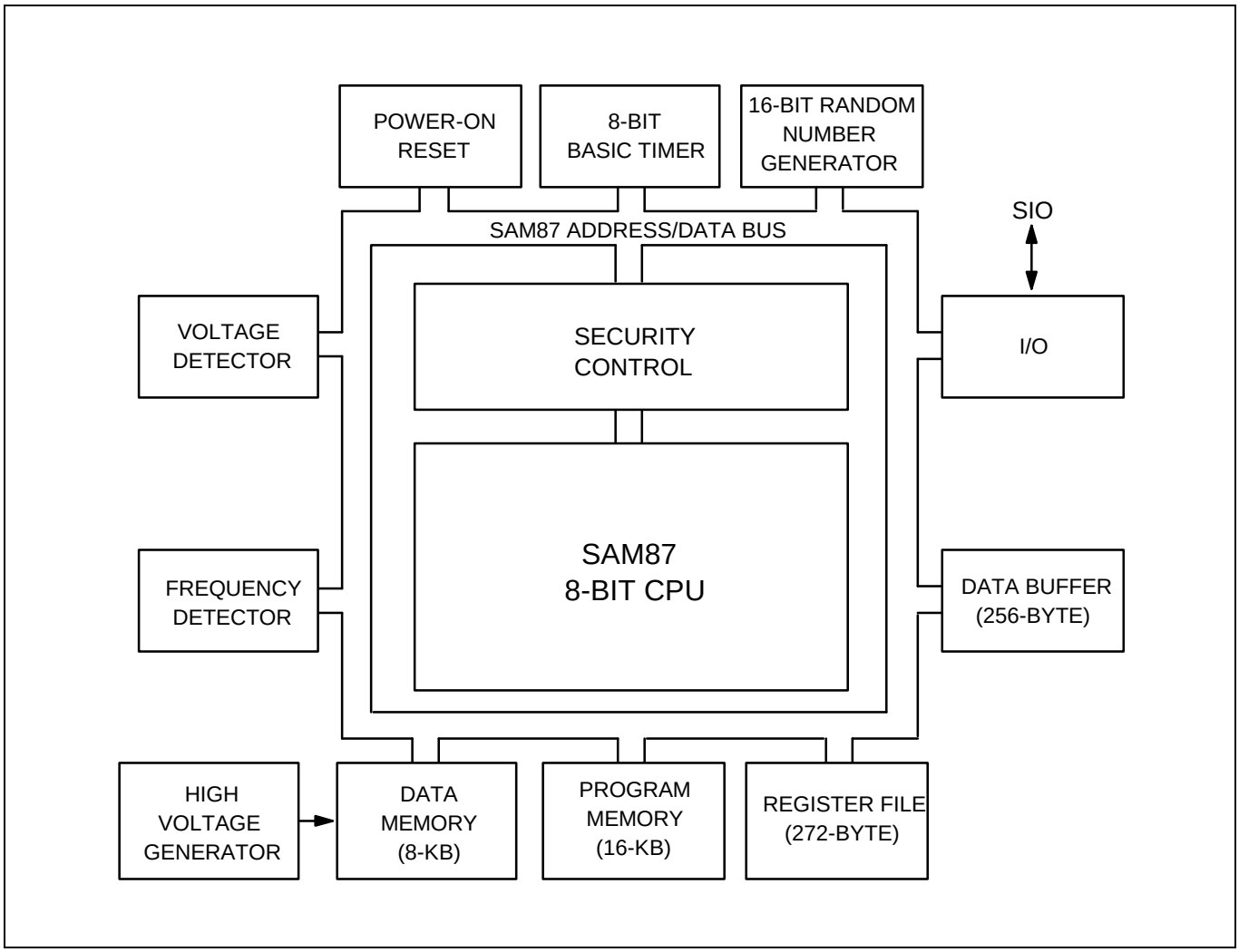


Figure 1–1. Block Diagram

PIN ASSIGNMENTS

Table 1–1. KS88C9408 Pin Descriptions

Pin Number	Pin Name	Function Description	Pin Type	Circuit Type
C1	V_{DD}	Power input	–	–
C2	RST	System reset input	Input	1
C3	CLK	External clock input	Input	2
C4	NC	No connection	–	–
C5	GND	Ground	–	–
C6	NC	No connection	–	–
C7	SIO	Serial data input and output; A pull up resistor should be connected to VDD	Input/output	3
C8	NC	No connection	–	–

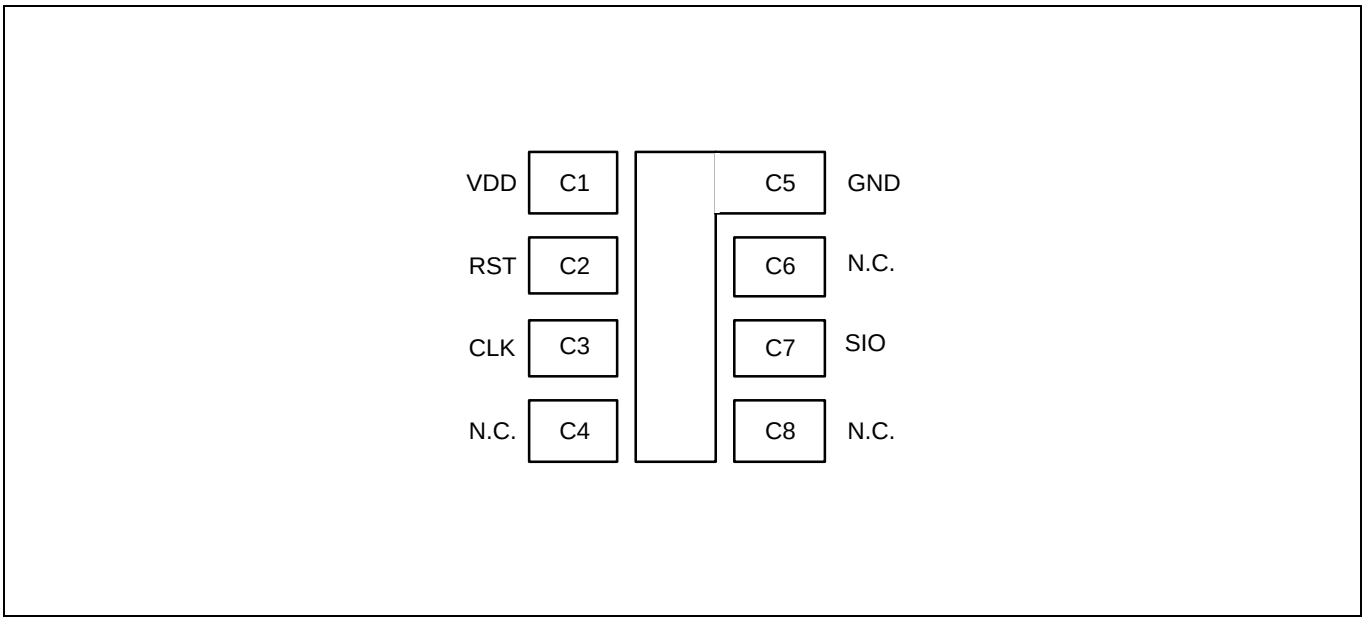


Figure 1–2. KS88C9408 COB Package Pin Arrangement

PIN CIRCUITS

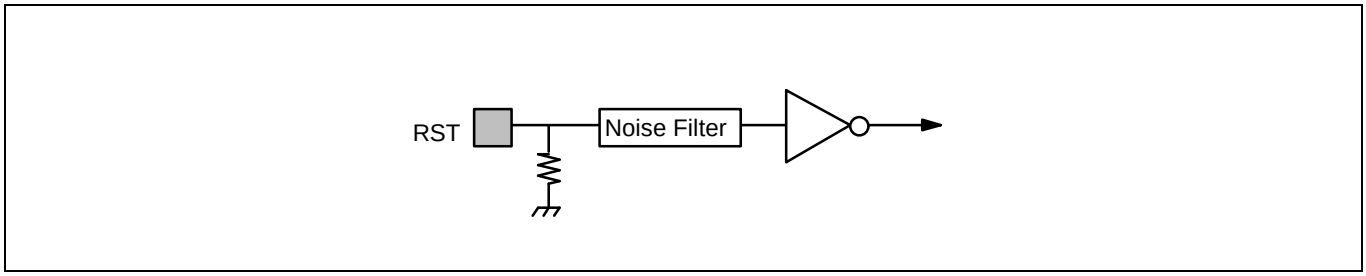


Figure 1–3. Pin Circuit Type 1 (RST)

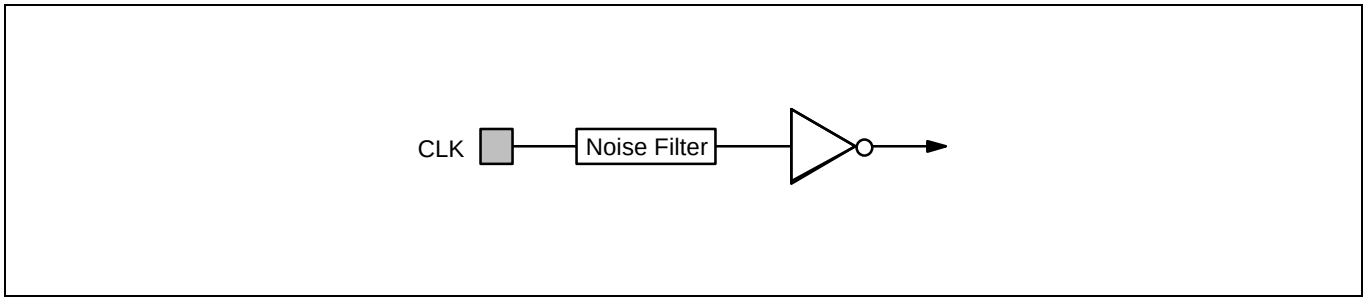


Figure 1–4. Pin Circuit Type 2 (CLK)

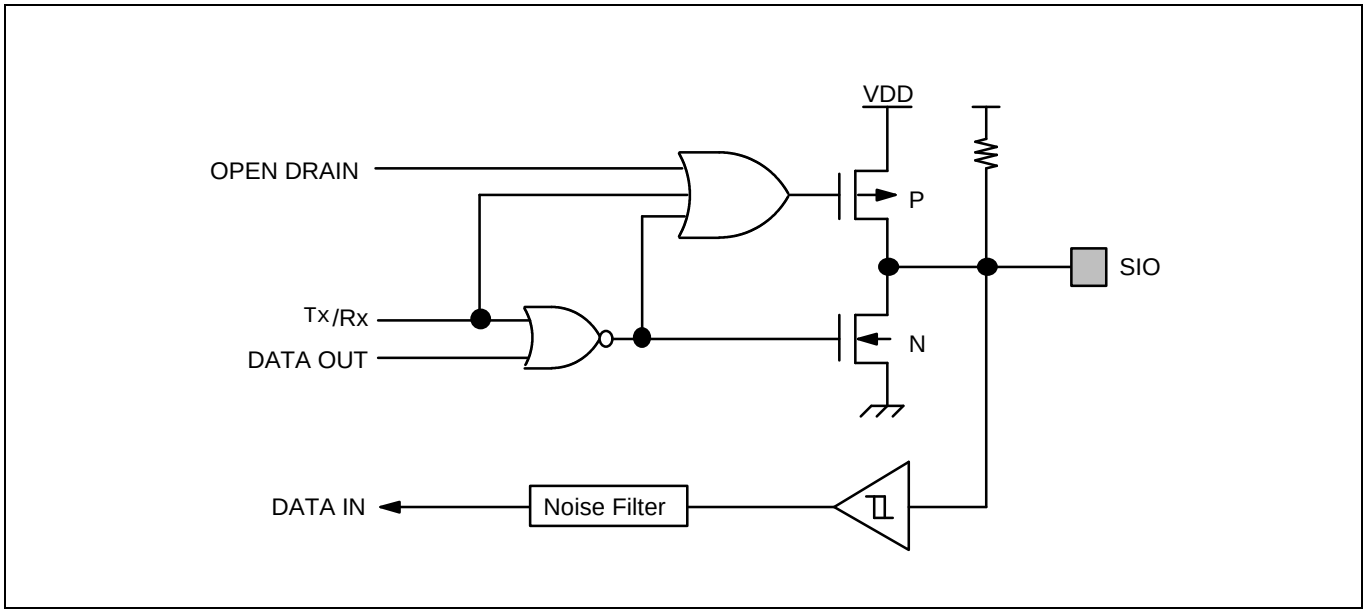


Figure 1–5. Pin Circuit Type 3 (SIO)

NOTES

15 ELECTRICAL DATA

Table 15–1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Operating temperature	T_A	–	– 25 to + 70	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	–	5000	V

Table 15–2. D.C. Electrical Characteristics

(T_A = – 25°C to + 70°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	SIO	–	–	0.2 V_{DD}	V
		CLK			0.12 V_{DD}	
		RST			0.15 V_{DD}	
Input Low Current	I_{IL}	SIO	– 1000	–	+ 20	µA
		CLK	– 100			
		RST	– 200			
Input High Voltage	V_{IH}	SIO	0.7 VDD	–	V_{DD}	V
		CLK	0.7 VDD			
		RST	0.8 VDD			
Input High Current	IIH	SIO	– 300	–	+ 20	µA
		CLK	– 20		+ 100	
		RST	– 20		+ 150	
Output Low Voltage	V_{OL}	I_{OL} = 500 µA, SIO	0	–	0.15 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = –20 µA, SIO	0.7 VDD	–	V_{DD}	V
Supply Current	I_{DD1}	f_{CLK} = 3.57 MHz, 5 V	–	3.5	10	mA
		f_{CLK} = 3.57 MHz, 3 V		1.0	5	
Idle Current	IDD2	f_{CLK} = 3.57 MHz, 5 V	–	1.0	2.0	mA
Stop Current	IDD3	f_{CLK} = GND, 3 V	–	–	10	µA

Table 15–2. D.C. Electrical Characteristics (Continued)

(T_A = – 25°C to + 70°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-voltage detection	V_{LVD}	f_{CLK} = 3.57MHz	–	2.6	–	V
High-voltage detection	V_{HVD}	f_{CLK} = 3.57MHz	–	7.0	–	V
Low-frequency detection	F_{LFD}	VDD = 5V, 25°C	200	500	800	kHz
High-frequency detection	F_{HFD}	VDD = 5V, 25°C	7	10	12	MHz

Table 15–3. A.C. Electrical Characteristics

(T_A = – 25°C to + 70°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External clock	f_{CPU}	CPU clock	1	3.57	5.0	MHz
External clock duty	t_{CW}	Clock width	45	50	55	%
RESET Low level width	t_{RSW}	–	5	–	–	µA
EEPROM erase cycle time	t_{EC}	–	–	1.5	–	ms
EEPROM write cycle time	t_{WC}	–	–	1.5	–	ms
EEPROM data retention	t_{DR}	–	10	–	–	years
EEPROM endurance	T_{EN}	–	100,000	–	–	cycles
Rise/Fall time (Cin = 30 pF)	t_R, t_F	SIO, RESET	0	–	1	µs
		CLOCK			0.5×9%	

NOTE: The rise time, fall time data for CLK assumes 9% of the period with a maximum time of 0.5 µs. This condition is represented by the formula, 0.09 × 1 / f_{CLK} .

SIO TIMING DIAGRAM

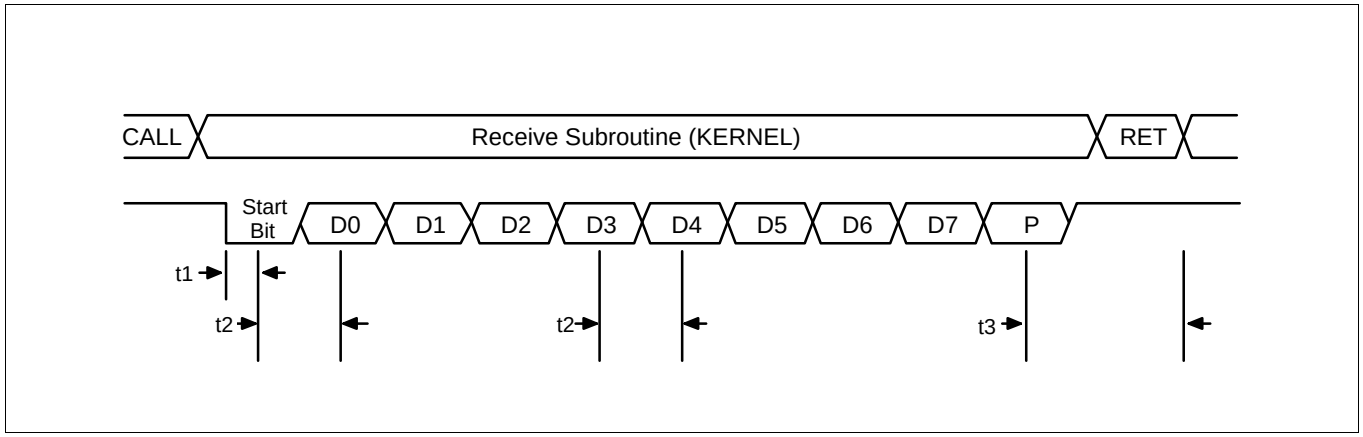


Figure 15–1. Data Receive

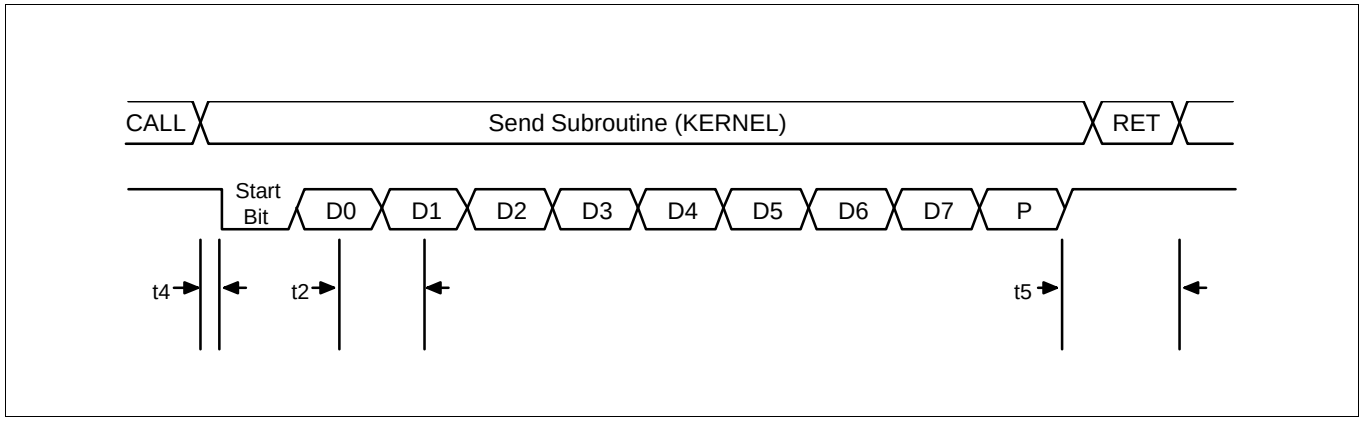


Figure 15–2. Data Send

Table 15–4. Number of Clock for Sampling at 3.57 MHz

bps	t1	t2	t3	t4	t5
9600	178–196	372	305	115	17
19200	86–104	186	161	115	17
38400	38–56	92	127	115	17

ELECTRICAL DATA (Continued)

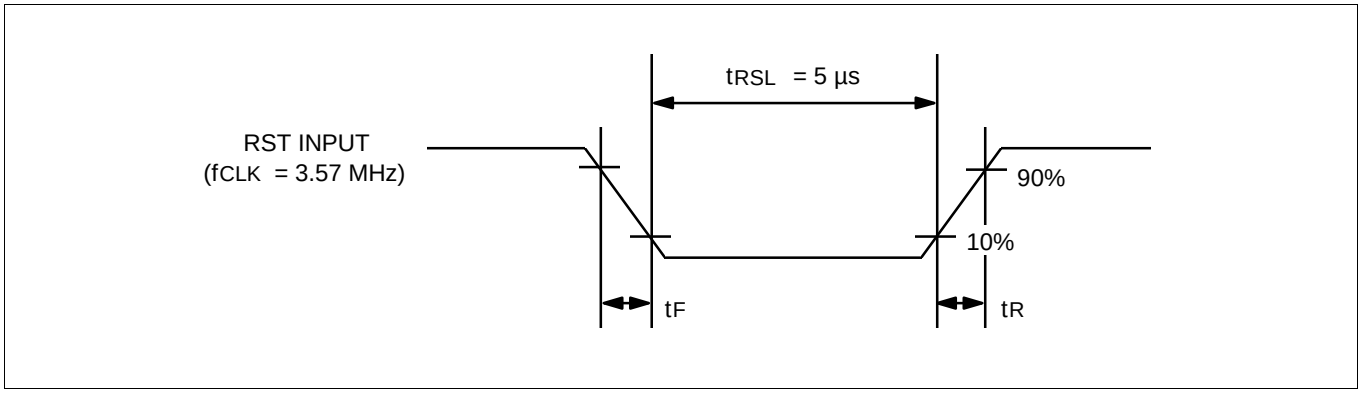


Figure 15–3. RST Input Wave Form

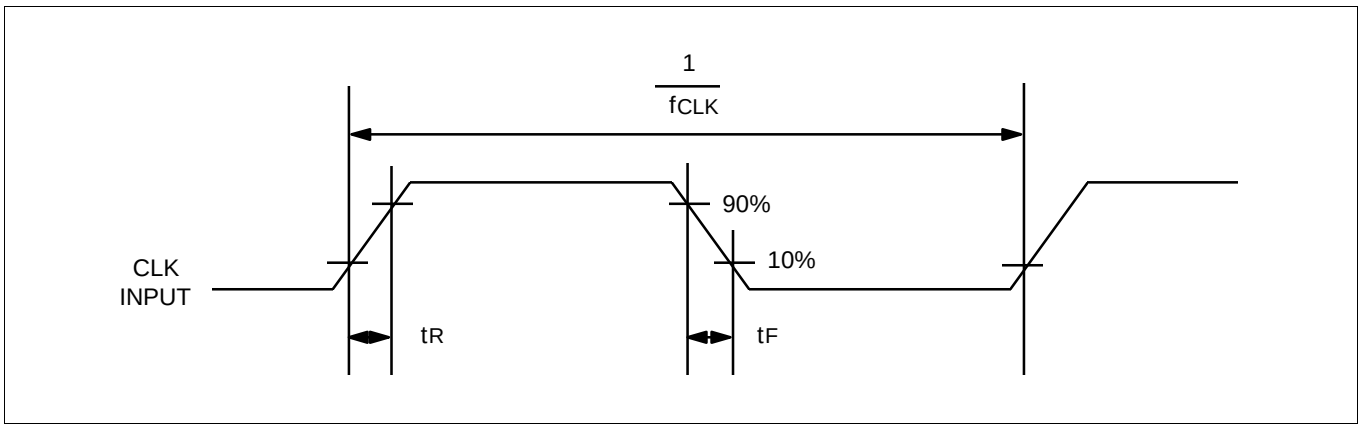


Figure 15–4. CLK Input Wave Form

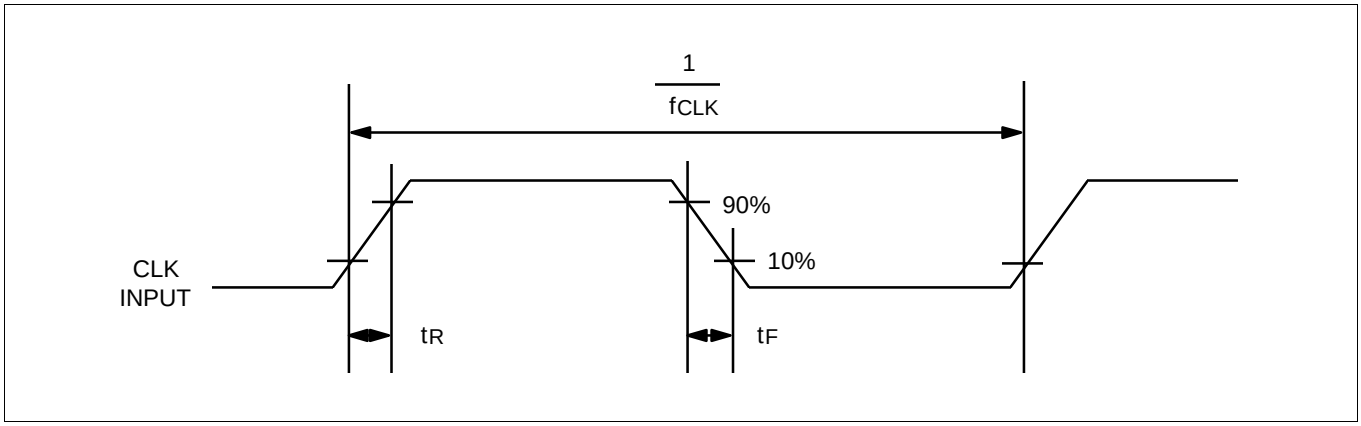


Figure 15–5. SIO Input Wave Form

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

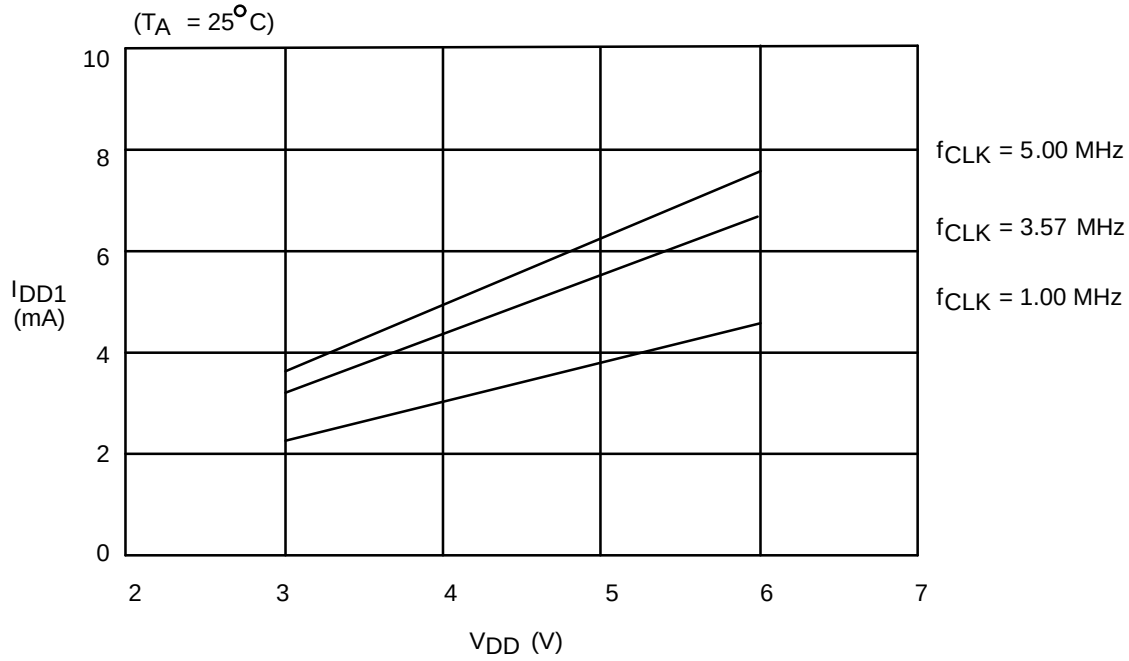


Figure 15–6. I_{DD1} vs. V_{DD}

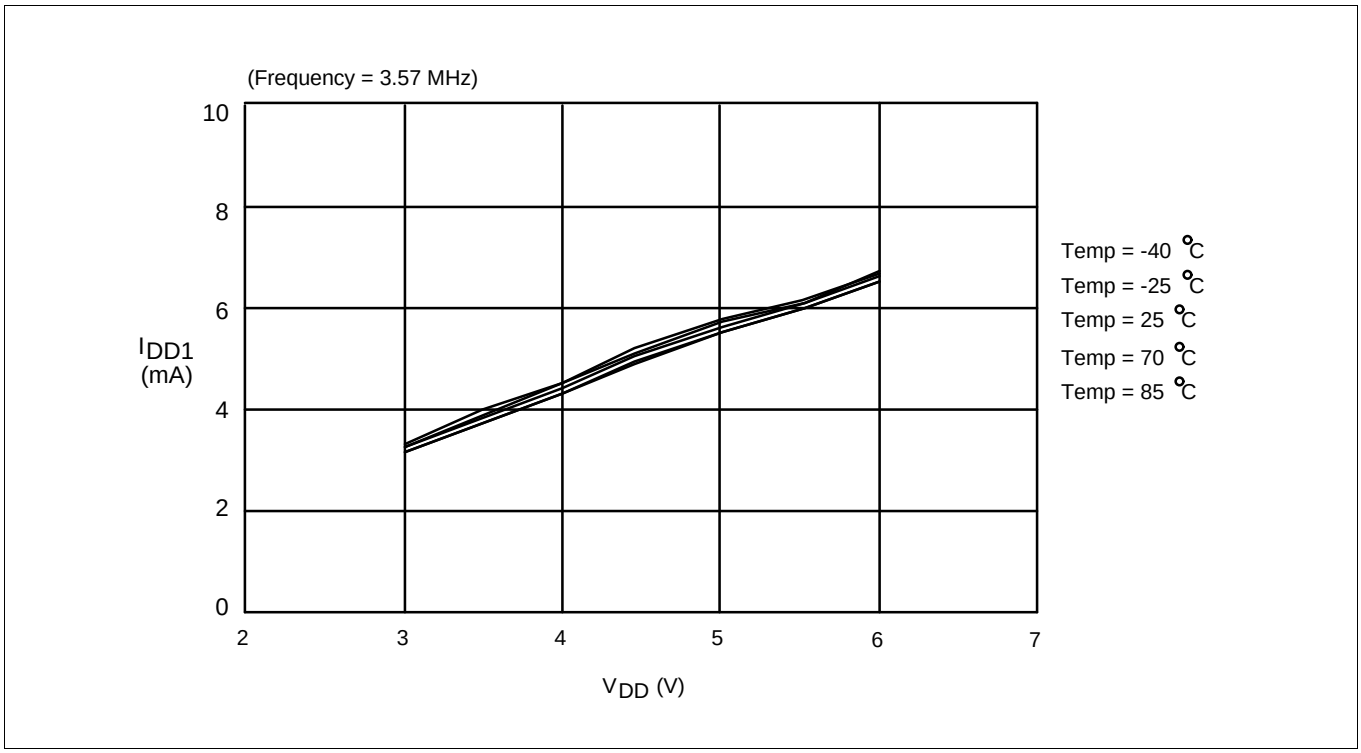


Figure 15–7. I_{DD1} vs. TEMP

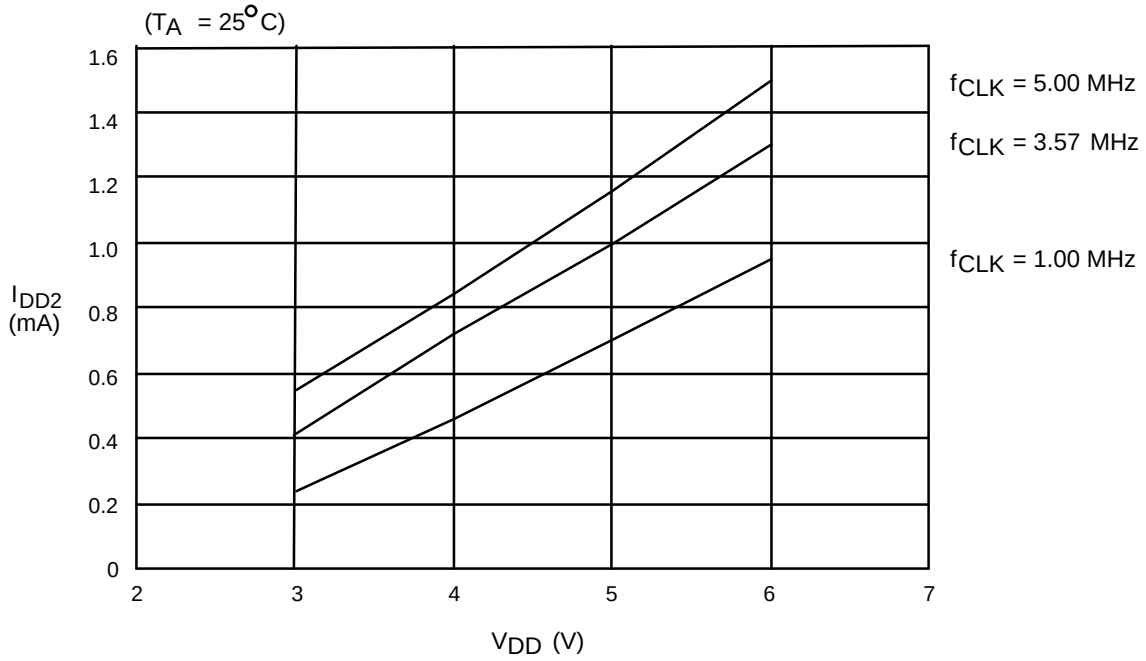


Figure 15–8. I_{DD2} (Idle) vs. V_{DD}

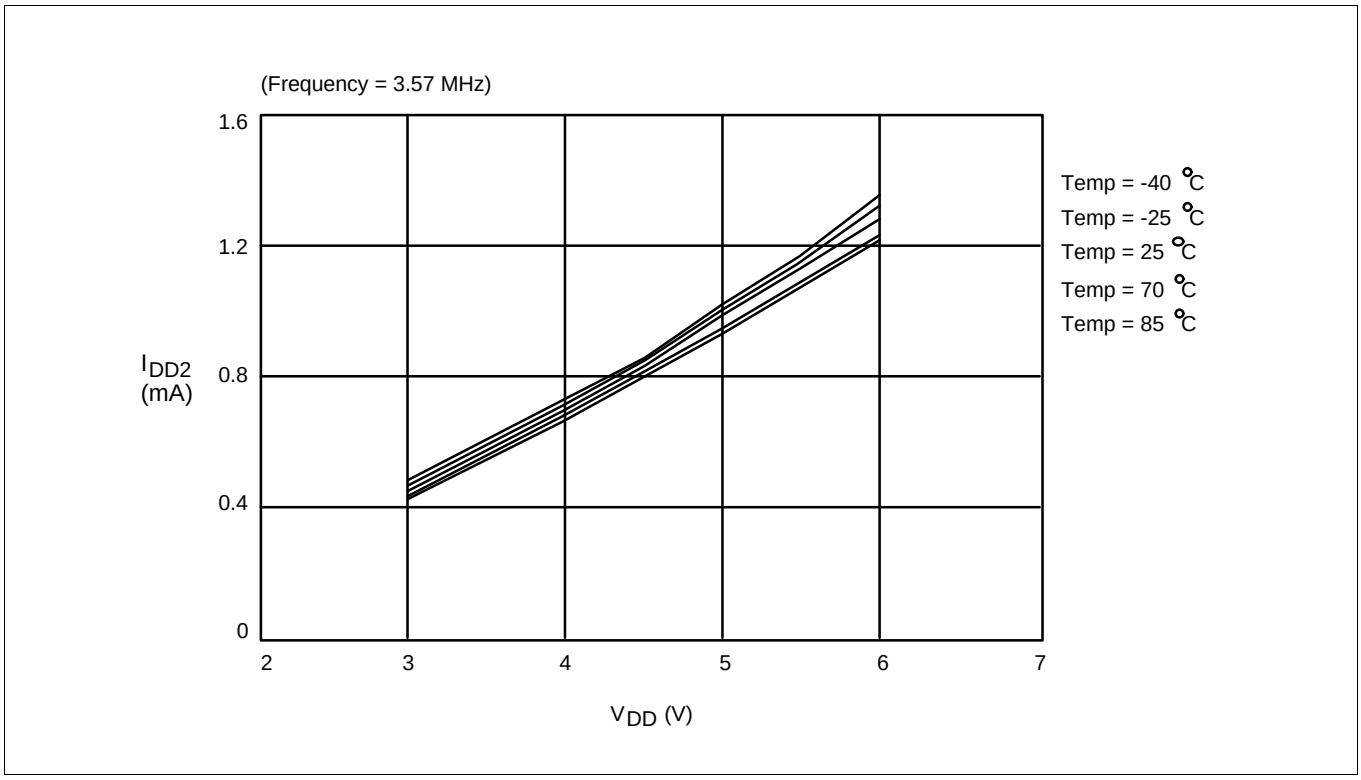


Figure 15–9. $I_{DD2\ (Idle)}$ vs. TEMP

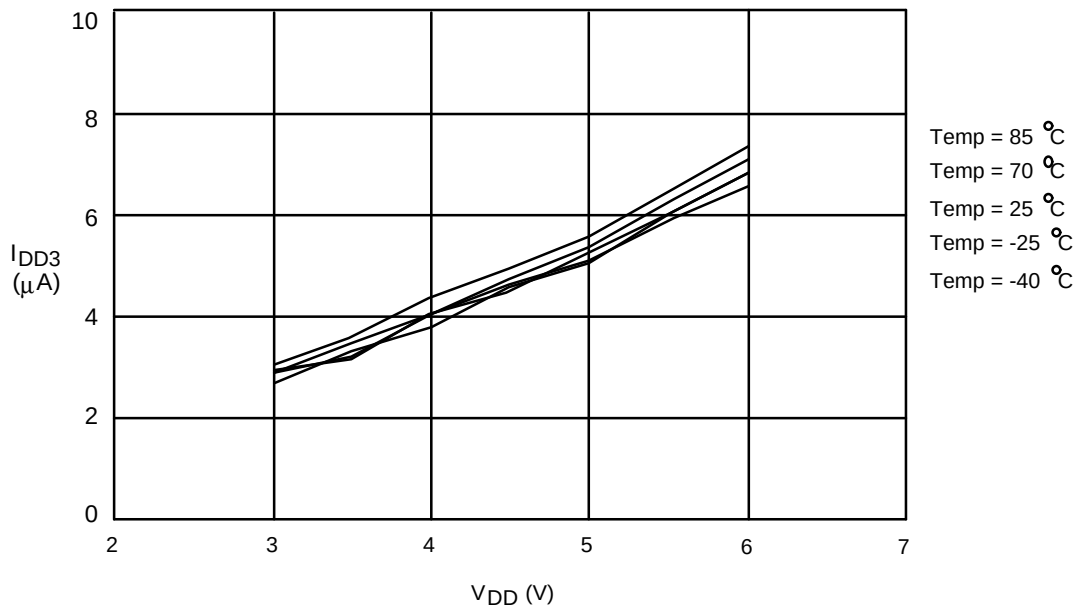


Figure 15–10. $I_{DD3\ (stop)}$ vs. V_{DD}

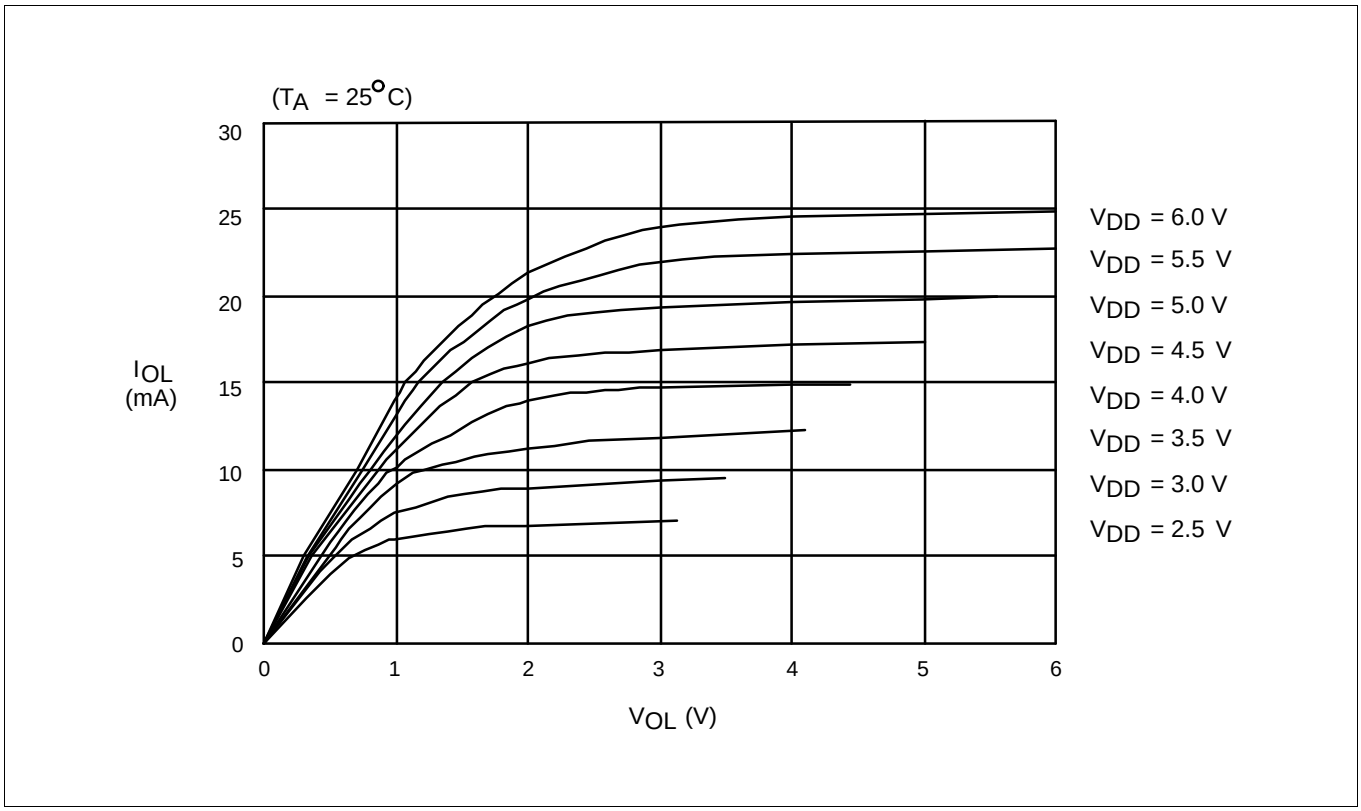


Figure 15–11. V_{OL} vs. I_{OL} (SIO Pin Output Low Voltage)

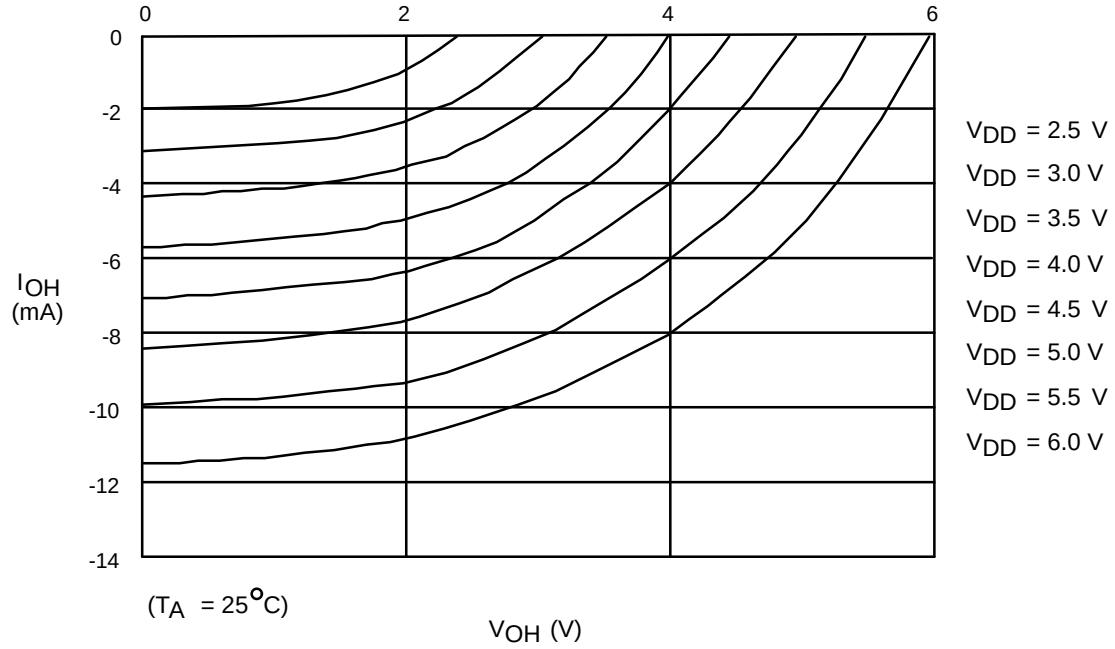
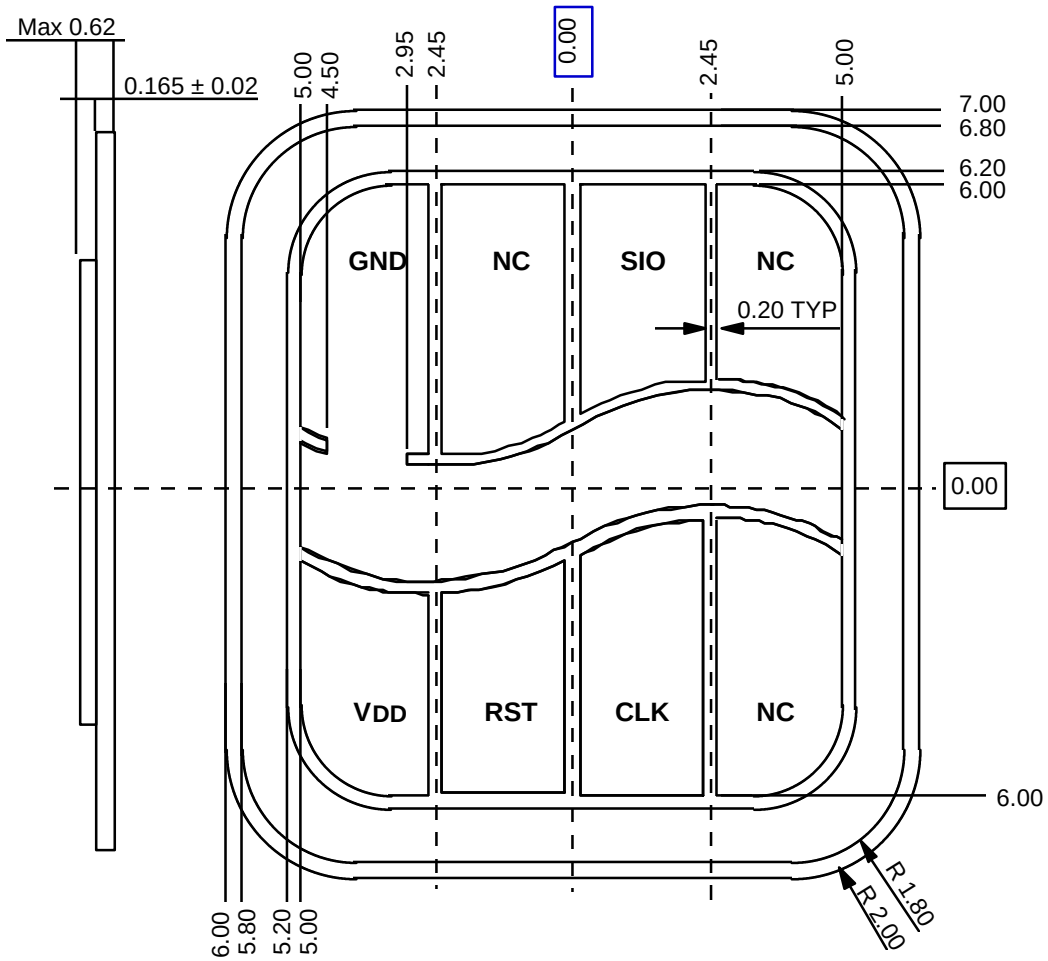


Figure 15–12. V_{OH} vs. I_{OH} (SIO Pin Output High Voltage)

NOTES

16 MECHANICAL DATA



NOTES:
1. Dimensions are in millimeters.
2. The 8-pad COB package dimensions shown above are only approximate. Actual dimensions are adapted to customer specifications.

Figure 16–1. Mechanical Dimensions for 8-Pad COB Package

NOTES